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► **To cite this version:**

Florent Becker, Ehsan Jamshidpour, Philippe Poure, Shahrokh Saadate. Switch Fault detection and localization for T-Type Converter. IEEE Transactions on Industry Applications, 2023, pp.1-8. 10.1109/TIA.2023.3241602 . hal-03971138

HAL Id: hal-03971138

<https://hal.science/hal-03971138>

Submitted on 4 Feb 2023

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Switch Fault detection and localization for T-Type Converter

Florent Becker*, Ehsan Jamshidpour†, Philippe Poure‡ and Shahrokh Saadate†

*Naval Academy Research Institute

†Université de Lorraine, GREEN

‡Université de Lorraine, Institut Jean Lamour (UMR7198)

Abstract—Over the past decade, multilevel converters have received considerable interest in medium voltage applications. A large number of active switches in a multilevel converter increases the probability of switch failure and decreases the reliability of the system. An open switch fault can lead to a malfunction of the whole system and should be diagnosed as soon as possible. In this paper, an open-switch fault diagnosis method for a five-level H-Bridge T-type converter is presented. The proposed fault detection method and the fault localization algorithm are based on the switching patterns and the converter output voltage level observation. This approach is capable to detect and localize an open circuit fault for all switches. First, it is validated by simulations in Matlab Simulink and Simscape toolbox environments. Experimental results are also presented and discussed to validate the simulation results.

Index Terms—Open-switch fault; Fault diagnosis; Fault detection; Fault localization; Multilevel converter; Neutral Point Piloted converter; T-type converter; H-bridge

I. INTRODUCTION

In recent years, multilevel converters (MLC) have been widely used in many different applications [1]–[5], such as transport (railway, electric vehicle, . . .), motor drive [1], [6], [7], grid-connected applications [8]–[11] and renewable energy [12]–[15]. These converters have many advantages: high power capacity, better power quality (reduced total harmonic distortion THD for AC voltage and current), reduced blocking voltage requirement for the power switches, and fault-tolerant capability [8], [16], [17]. Among the different MLC topologies, some converters such as the cascaded H-bridge inverter, the Neutral Point Clamped (NPC), the T-Type (or Neutral-Point Piloted (NPP)), and the flying capacitor converters have been used in industrial applications [4], [9], [18], [19]. The T-type converter is more attractive than other MLC structures for industrial applications thanks to its low conduction switching losses, compared to other converters [3]. The T-type converter topology is presented in Fig. 1.

Switch Open Circuit Failure (OCF) is one of the most common failures in power electronic converters. Fig. 2 shows the results of a study of more than 200 products from 80 companies. It confirms that semiconductor and solder failures are the cause of more than 30% of systems comprising power electronic converters [20]. In these converters, bond wire lift or solder cracking due to thermo-mechanical stresses and

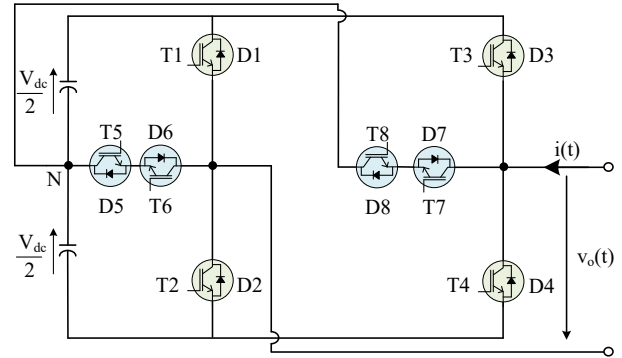


Fig. 1. Circuit of the 5-level T-Type converter.

high junction temperature variations, gate driver malfunction, and electrical disconnection can cause OCFs in the switching devices [1]. Based on another survey for faults in DC-DC converters, the failure rate for switches is 31% while for diodes is 4%. This shows that switches are more vulnerable than diodes [21]. Therefore, switch OCF diagnosis is one of the major design criteria for safety-critical applications. An OCF leads to current distortion and increased voltage stress, which can lead to a breakdown if the fault persists for a long time; thus, the switch failure must be detected and localized rapidly. Therefore, having a fast and reliable fault detection and localization method for the power electronic converters is necessary.

Several fault detection methods have been proposed in the

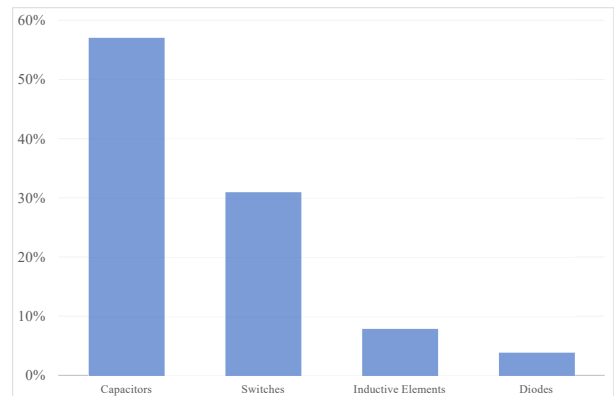


Fig. 2. Distributions of faults in power electronics converters [20].

scientific literature [1], [8], [18], [22]–[25]. In [1], a review of fault detection methods for Modular Multilevel Converters (MMC) has been presented. In this paper, diagnostic techniques for open-switch faults have been reviewed. Most of the works have been focused on the classical two-level and multilevel inverters [22], [23]. However, due to the actual importance of renewable energy resources, in the latest years, the study of fault diagnosis of MLC became very attractive. Some fault detection methods for PV grid-connected systems using MLC are proposed in [8], [24], [25]. The authors of [2] present an OCF diagnosis based on the capacitor voltage balance principle for eight IGBT-based submodules MMC applications. In [26], a fault diagnosis method based on the mass center of the voltage pattern is proposed for the T-type converter topology.

In [27], an OCF diagnosis strategy is proposed for a four-wire T-type converter. This method is based on decomposing the circuit model into positive, negative, and zero sequence models, and locating the OCF by the law of the voltage error offsets of the sequence models.

In [28] a data-driven fault diagnosis method of a five-level nested neutral point piloted (NNPP) converter is proposed. The authors of this paper have used, an affine-invariant Riemannian metric autoencoder (AIRMAE) for fault diagnosis of multilevel converters.

In [29], [30], the authors present OCF diagnosis approaches for multilevel inverters using the current distortion calculation of each phase and the variation in the DC link voltage as the fault diagnosis signature. The proposed method is applied on an hybrid active neutral point converter (HANPC) in these papers. In [31] an OCF diagnosis method for a four-level active neutral-point-clamped (4L-ANPC) inverter is presented. This method is based on the appeared distortions on two measured voltage waveforms (output phase voltages and the inter-half-bridge voltages) and output current.

This paper is an extended version of the conference paper [32] that first introduced the fault diagnosis method for a five-level H-Bridge T-Type (5L HB T-Type) converter. Because of the numerous switches that are used in this topology, it is particularly vulnerable to switch faults. The proposed fault diagnosis is composed of two parts: Fault Detection Method (FDM) and Fault Localization Algorithm (FLA). The proposed FDM is based on the output voltage observation. This FDM compares the measured output voltage (V_o) with the desired (estimated) value of the output voltage (V_{oe}), according to the applied switching patterns. The estimated voltage is computed from the switching pattern and from the converter states for each possible combination of switches (see Fig.3). If any mismatch appears, it means that a switch fault has occurred. When an OCF is declared, the proposed FLA activates the localization process, as well as the identification of the faulty switch, which will be detailed in the following. In [32] the principle parts of the proposed method are presented and validated only with simulation results. In this paper, the OCF diagnosis method is verified and validated by selected experimental results.

In the next section, the 5L HB-T-type and the different states are presented. Then, in section III, the principle of

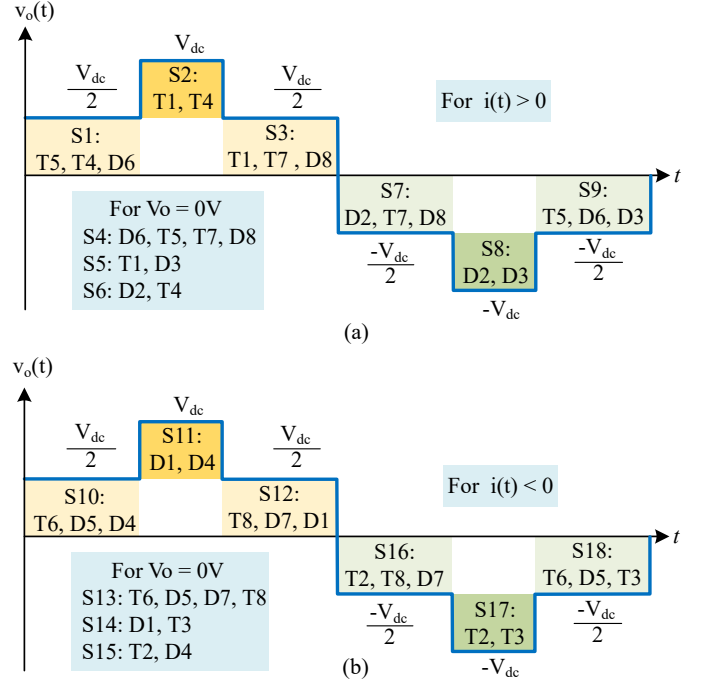


Fig. 3. (a) Output voltage levels and corresponding states for positive output current (b) Output voltage levels and corresponding states for negative output current.

the proposed fault diagnosis method for the 5L HB-T-type is detailed. In section IV, the proposed approach is validated by simulation. Section V presents some selected experimental results, and finally, some conclusions are provided.

II. FIVE LEVEL H-BRIDGE T-TYPE TOPOLOGY

Fig. 1 shows the 5L HB-T-Type converter. This converter has 8 switches (that can be IGBT or MOSFET) with antiparallel diodes. The 5L HB-T-Type converter is supplied by a DC voltage source (V_{dc}) with a central neutral point, called N. Depending on the switching pattern (control orders) and the sign of the output current, the converter can generate 5 different voltage levels: $V_{dc}/2$, V_{dc} , 0 , $-V_{dc}/2$, and $-V_{dc}$. In this paper, for each voltage level that depends on a specific switching pattern and for positive and negative output current, a state (S1 to S19) is introduced. The states, voltage levels, and the switches that are constructing the current path for each state are depicted in Fig. 3(a) for positive current (S1 to S9) and in Fig. 3(b) for negative current (S10 to S18). In the next section, the fault diagnosis approach is detailed.

III. FAULT DIAGNOSIS METHOD

A. Fault detection method

Fig. 4 shows the fault diagnosis algorithm. As mentioned before, the proposed fault detection method is based on the switching pattern and the output voltage value observation. For the studied 5L HB-T-Type converter, the 18 states must be considered. The switching patterns ($\delta 1$ to $\delta 8$) are produced by the “current and voltage control” block by measuring the output voltage (v_o) and current $i(t)$. The “voltage estimation” block estimates the value of the desired output voltage v_{oe}

by using the switching patterns and the states shown in Fig. 3, considering the current direction. After that, “the Fault Detection Method” (FD:) block compares the measured and desired output voltage (v_o and v_{oe}). If $v_o = v_{oe}$, it means that the converter works in healthy condition. Otherwise, the error signal “err” is not null.

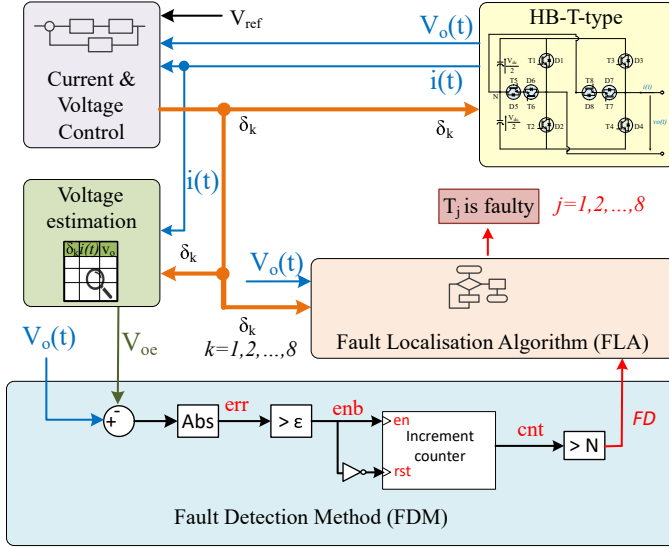


Fig. 4. Fault diagnosis approach.

To avoid false detection, two criteria are considered. The first one compares the error value with an accepted tolerance (ϵ). If the error is larger than ϵ , the “enb” signal switches to ‘1’ level. The second criterion is the time criterion. When “enb” becomes equal to ‘1’, the increment counter is activated and the “cnt” value increases. If “cnt” passes the selected threshold value “N” and the “enb” is always equal to ‘1’, the fault detection method declares a fault occurrence and the signal “FD” steps up to ‘1’.

B. Fault localization method

As mentioned before, the proposed fault diagnosis method has two steps:

- 1) fault detection,
- 2) fault localization.

In the previous fault detection step, a switch fault is declared by the FDM, but the faulty switch is not localized yet. The T-type converter has 8 semiconductor switches (IGBT, MOSFET, ...). Therefore identifying the faulty switch is not simple and needs an efficient and fast algorithm.

As depicted in Fig. 4, the fault localization algorithm (FLA) is activated by the “FD” signal generated by the FDM bloc. The FLA principle is summarized in Fig. 5 and Fig.6 for the positive and negative current respectively. The output voltage values for each possible OCF case have been previously calculated and registered in a Table. This FLA recognizes the states by encoding the switching commands (δ_1 to δ_8) and then compares the measured output voltage with the value of the voltage table, considering the current direction, to identify the faulty switch. For some states, two switches can

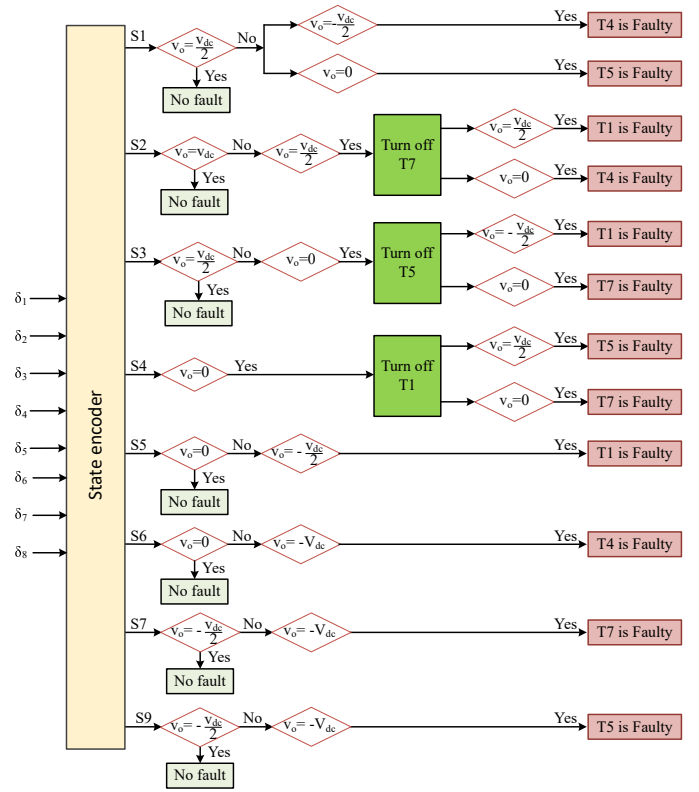


Fig. 5. Fault localization algorithm when output current is positive.

be potentially faulty. To explain and detail the localization algorithm, the states can be arranged into three groups:

- S8 and S11, no switch is conducting the current (group 1).
- S5, S6, S7, S9, S12, S14, and S15: a single switch is active (group 2).
- S1, S2, S3, S4, S10, S13, S16, S17, and S18: 2 switches are forming the current path (group 3).

For the group 1 (S8 and S11), there are just 2 passing diodes in the circuit, therefore any switch (IGBT or transistor) is concerned. Thus, fault localization is not necessary for this group. For the group 2, the algorithm can localize the faulty switch in a single step by comparing the measured output voltage with the predefined value for output voltage, in case of a switch fault, as illustrated in Fig.5 and Fig. 6.

But, for the group 3, there are two passing switches in each state, and thus, the faulty one cannot be localized in a single comparison step. As Fig. 5 and 6 show, the proposed algorithm needs to do an additional operation to identify the faulty switch. For example, Fig. 7 shows an OCF detection in state S3. In a healthy case of S3, the current passes through T1, T7, and D8 (see Fig. 3(a) and Fig. 8(a)). According to FDA (Fig. 5), in a healthy condition of S3, the output voltage is $V_o = V_{dc}/2$. But when an OCF has occurred in one of the switches (T1 or T7), the output voltage is $V_o = 0$ (see Fig. 8 (b) and (c)). Therefore, the FDM declared an OCF but the faulty switch can not be localized. To identify the faulty switch, the FLA turns off the switch T5 and observes the output voltage(Fig. 8 (d)). If the output voltage remains

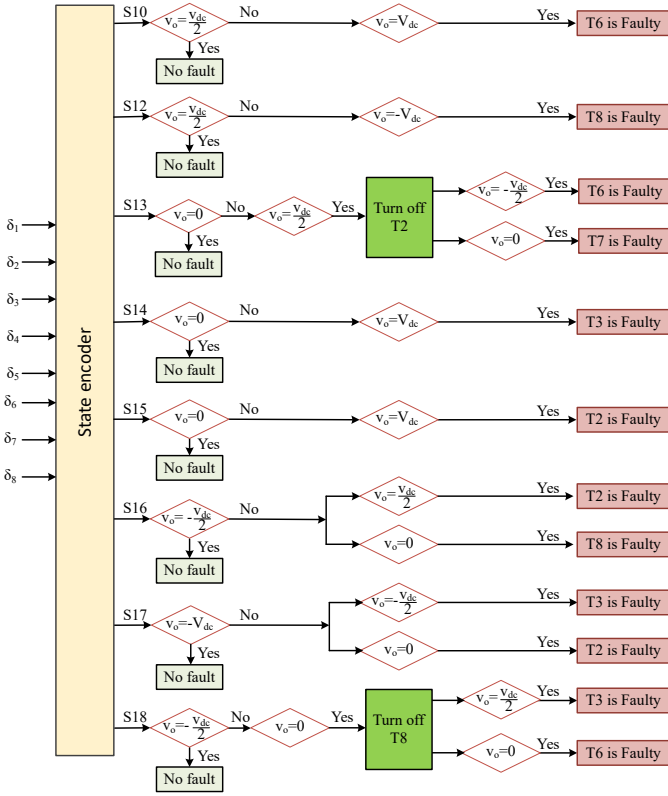


Fig. 6. Fault localization algorithm when output current is negative.

$V_o = 0$, T7 is the faulty switch. If the output voltage steps down to $V_o = -V_{dc}/2$, the fault has occurred in T1 (Fig.8(d)). For the other three states, the same additional operation must be done to localize the faulty switch. Fig. 5 and Fig. 6 summarize the fault localization approach for the other states of this group.

IV. SIMULATION RESULTS

To validate the performance of the proposed switch fault detection method applied to the 5L HB-T-Type, some simulations are performed in the Matlab/Simulink environment using the Simscape library. This converter supplies a load (R, L) with $R = 30\Omega$ and $L = 10mH$. The value of V_{dc} is equal to 1200V. The five possible output voltage levels of the converter have already been recorded in Fig. 3, according to the associated switching states.

For the first simulation test, the case of an OCF in T2 in state S17 is considered. As it can be seen in Fig. 6, this state is in group 2. There are two possible faulty switches (T2 and T3). Fig. 7 presents the simulation results when an OCF is artificially imposed in T2 at $t_1 = 14.2$ ms and is turned off. To view more details about fault detection, a zoom around the time of the fault occurrence (t_1) is shown in Fig. 7(b). This figure shows that at t_1 the voltage V_o and V_{oe} are not equal. Thus, the counter turns on and starts counting. Once $Cnt = 20\mu s$ ($N=20$ with simulation sample time = $1\mu s$ see Fig. 4), the switch T2 is declared as faulty at t_2 because ($V_o = V_{dc}) \neq (V_{oe} = 0)$.

Let's now study a case of the group 3. Fig. 8 shows the circuit in state S3. When an OCF occurs in T1 or T7, the

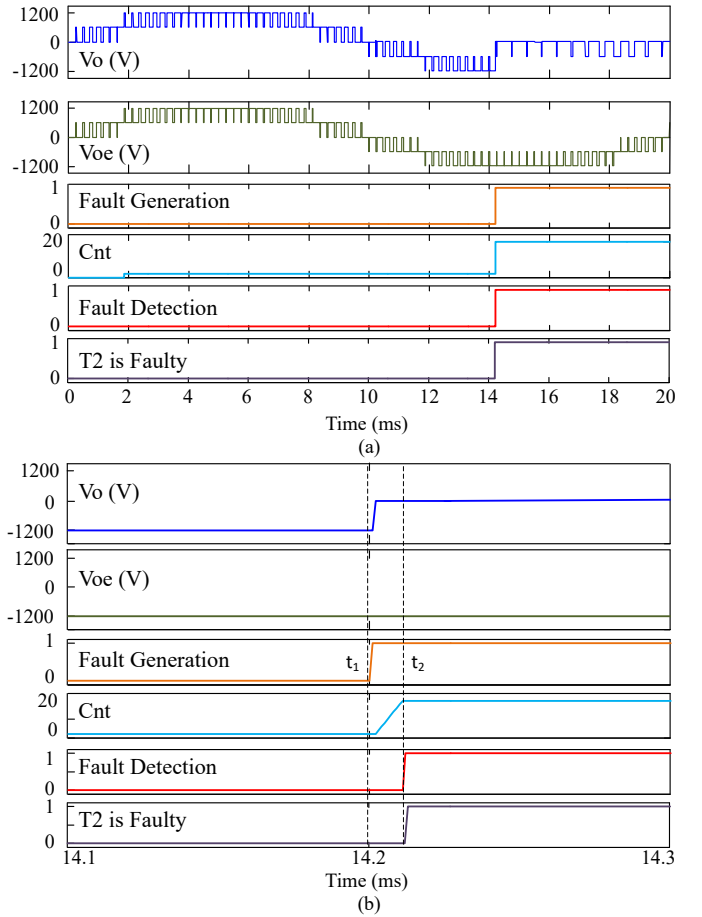


Fig. 7. (a) Simulation results for an OCF in T2 in state S17 (b) zoom during the fault detection.

output voltage V_o is equal to 0 and two steps are needed to detect and localize the fault. The simulation results are shown in Fig. 9 and Fig. 10. First, the case of an OCF in T7 is studied. As it is shown in Fig. 9(a), an OCF is artificially imposed in T7 at $t_1 = 8.94ms$. Therefore, the output voltage V_o steps down to 0 volt. The FDM detects the fault by comparing $V_{oe} = V_{dc}/2$ and $V_o = 0$, and thus FT signal goes to '1'. To know which switch is faulty (T1 or T7) the switch T5 is turned off by the FLA. As the value of V_o remains equal to '0', the FLA declares that T7 is faulty. Fig. 9(b) is a zoom of Fig. 9 around the fault occurrence time. Let's now study the OCF case in T1 during S3 state. Fig. 10 shows the corresponding simulation results. The fault is artificially generated at $t_1 = 8.7ms$ (Fig. 10). But, $\delta_1 = '0'$ for the time interval of $[t_1, t_2]$ and the switch T1 is not forming the current path during this interval. Therefore the converter works in healthy conditions, and no fault is detected until t_2 . At t_2 , the control system sets the switching command of T1 to '1' ($\delta_1 = '1'$). In healthy conditions, the output voltage V_o should be equal to $V_{dc}/2$, but as it can be seen in Fig 10, V_o remains zero. At this time, the FDA correctly declared an OCF by comparing the values of V_o with V_{oe} . Thus the "FD" signal goes to '1'. Until now, the fault is detected but the faulty switch is not determined yet. As is shown in Fig. 5, to discern the faulty switch between T1 and T7, the switch T5 must be turned off ($\delta_5 = '0'$) at

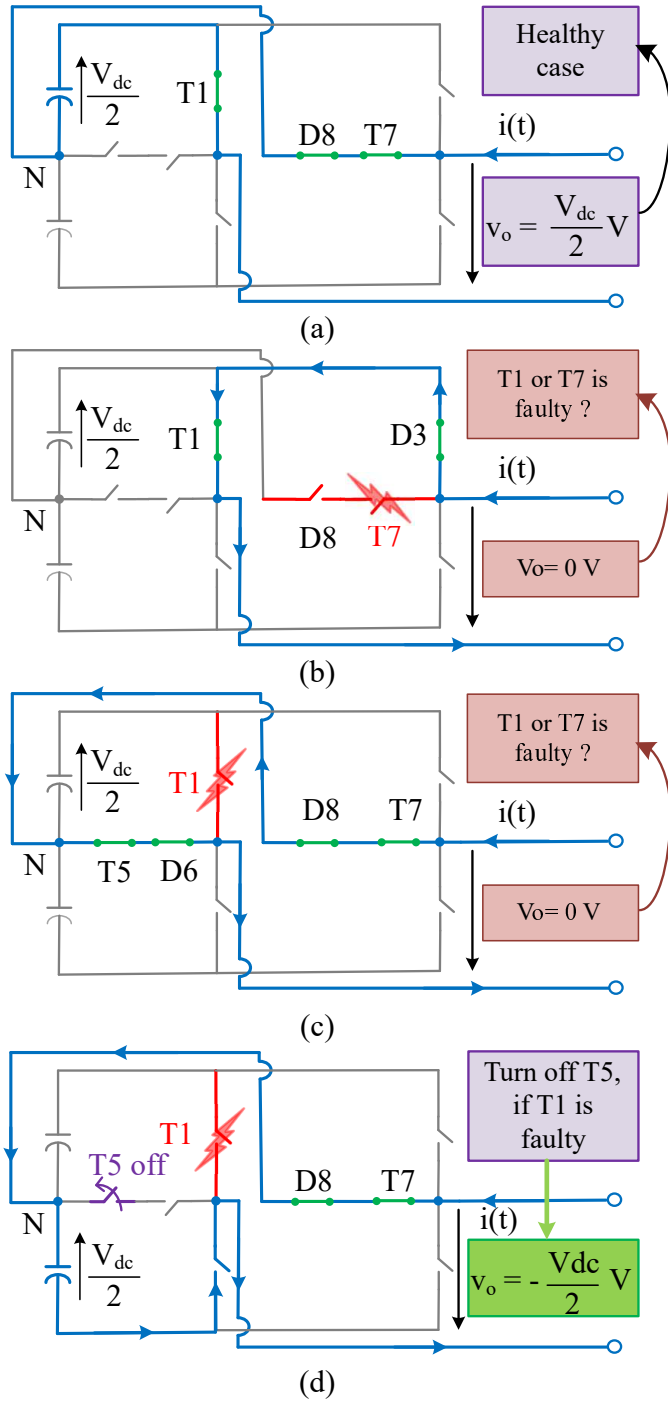


Fig. 8. The 5L-HB converter current path during state S3.

t_4 . At this time, the output voltage V_o steps down from zero to $-V_{dc}/2$ and the FLA, declares “T1 is faulty”. In the next section the experimental results will be presented.

V. EXPERIMENTAL RESULTS

To verify the validity of the proposed switch fault diagnosis applied to the 5L-HB T-Type, several experimental tests are carried out.

Fig. 11 shows the test bench. SEMIKRON IGBTs (SKM50GB123D) are used for the converter. They are driven

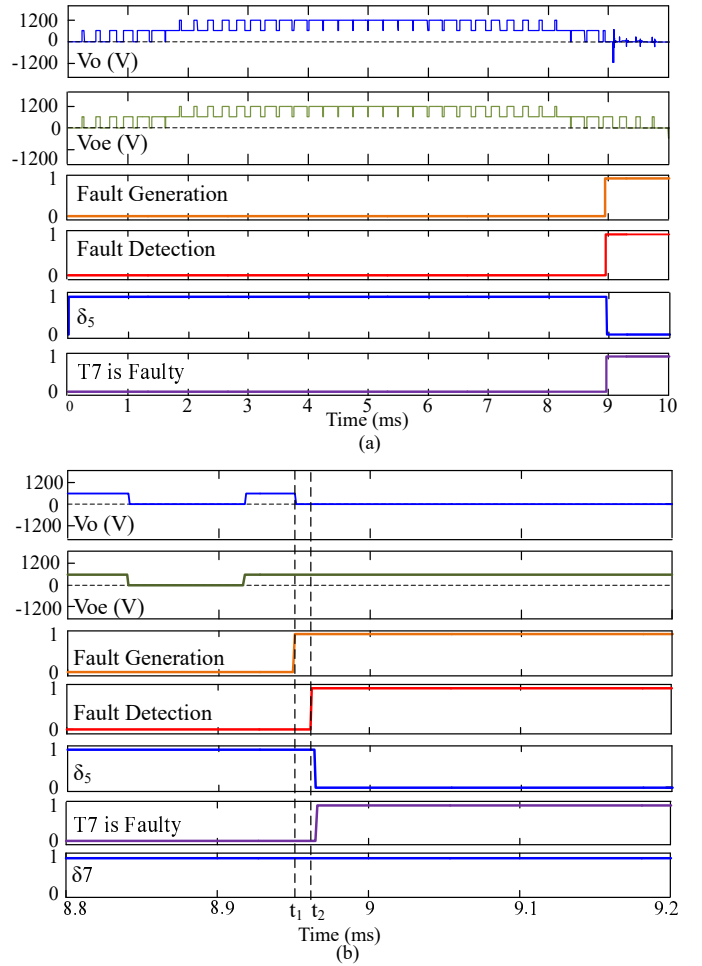


Fig. 9. (a) Simulation results for an OCF in T7 in state S3 (b) Zoom around the fault occurrence.

by drivers SKHI 22A. The DC bus capacity is $2200\mu\text{F}$ and $V_{dc} = 100\text{V}$. A RL load with a resistance of $R = 27.7\Omega$ and an inductance $L = 9\text{mH}$ is used. The frequency of the PWM is equal to 2000Hz .

In order to avoid any potential problems in the power system, the OCF diagnosis must be carried out quickly and in parallel with the other control tasks of the system. Fig. 12 shows the schematic of the proposed test bench. The control method is applied by using a dSPACE system containing a control card DS1005 as well as a DS2004 for high-resolution analog conversion (16 bit- $0.8\mu\text{s}$) and a PWM card DS5101 with 12 outputs. As the dSPACE is not a sufficiently fast calculation system, therefore it is not suitable to realize the switch OCF diagnosis. Thus, an FPGA from the ALTERA family is also used (Stratix S80B956C6). Thanks to its fast calculation capacity, the FPGA card ensures the detection of the fault, and its location. In this case, the dSPACE system will always perform the healthy mode control of the converter; the FPGA will perform the main functions dedicated to switch OCF detection and localization of the converter. The FPGA operation frequency is chosen to equal 1MHz , corresponding to a sample time (T_c) equal to $1\mu\text{s}$. For this test bench, maximum total system delay including delay of IGBT and

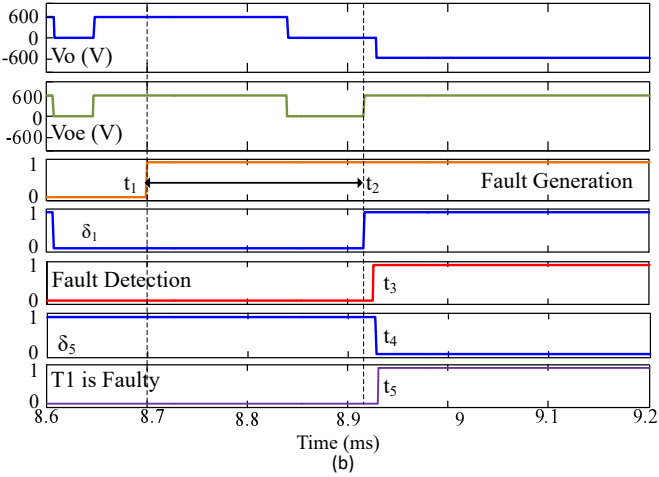
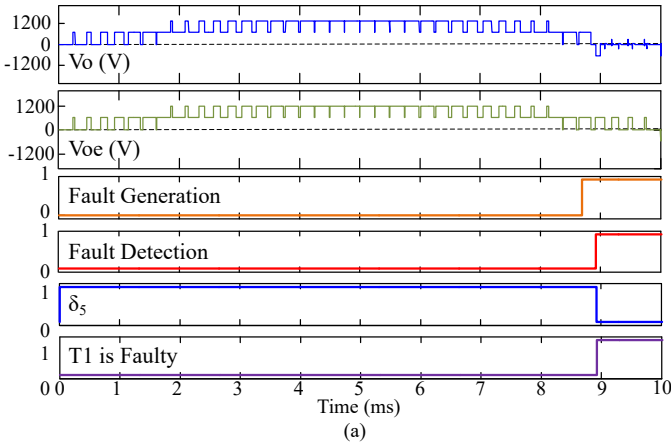


Fig. 10. (a) Simulation results for an OCF in T1 in state S3 (b) Zoom around the fault occurrence.

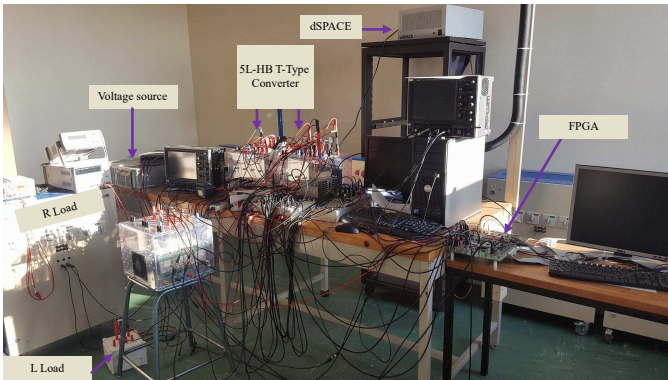


Fig. 11. Experimental test bench.

driver, A/D converter, sensors, interface circuit, etc. is less than $10\mu s$, therefore to avoid false FD, observation time (NT_c) is chosen to equal $20\mu s$ ($N = 20$).

In this section, we will present three cases of fault diagnosis for the 5L-HB T-Type converter: one case of group 2, and two cases of group 3. According to the test bench characteristics existing in our laboratory, the experimental tests are performed in a reduced voltage range for the DC bus voltage ($V_{dc} = 200V$) compared to the simulation results ($V_{dc} = 1200V$). Knowing that the open-switch fault detection

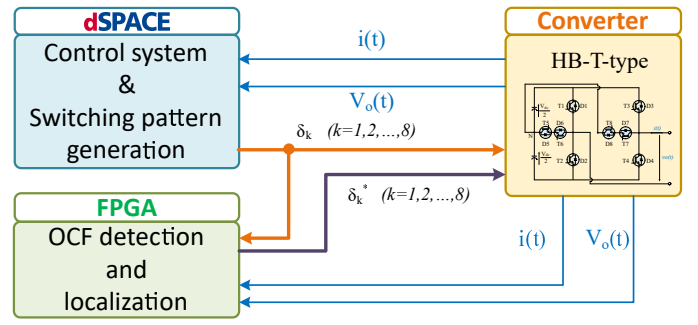


Fig. 12. Schematic of the experimental test bench control system.

for lower voltages is more difficult than for higher ones. In other words, if the proposed method works correctly for $V_{dc} = 200V$, it will also be able to guarantee fault diagnosis for $V_{dc} = 1200V$. Therefore, in the experimental results, v_o and v_{oe} waveforms have a voltage scale of $200V/div$, and the other signals are “binary” signals.

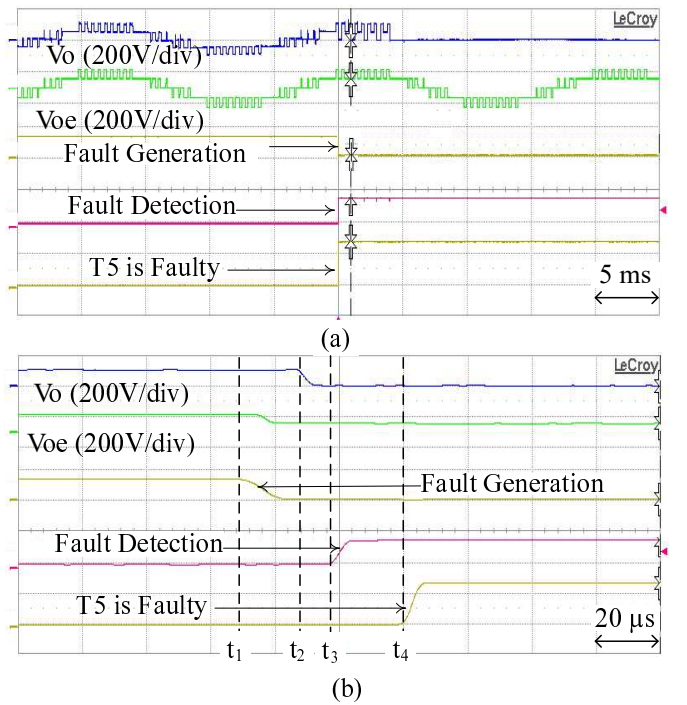
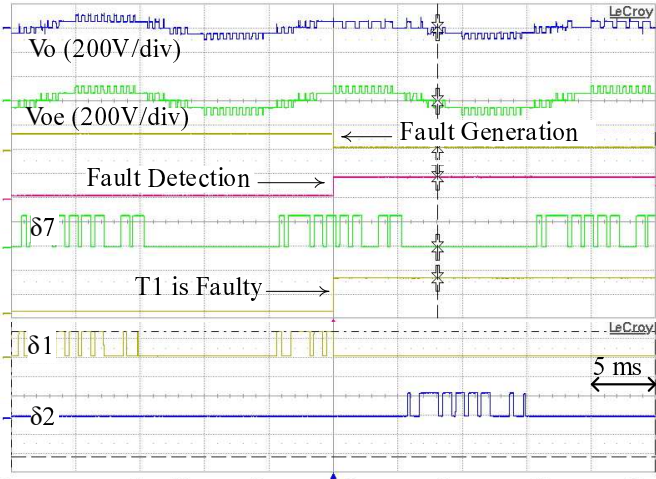
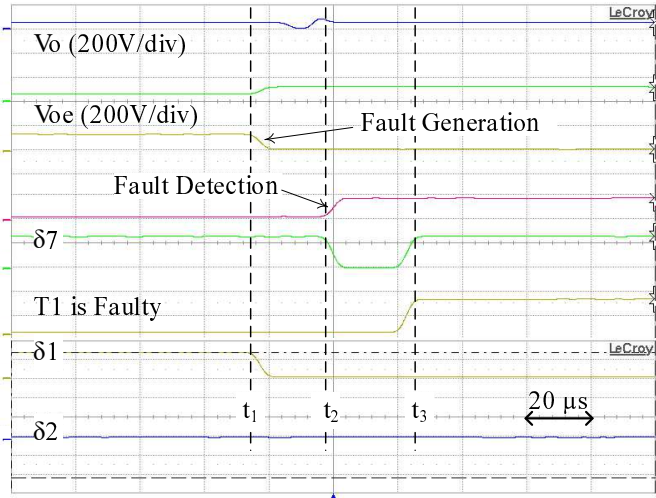


Fig. 13. (a) Experimental results for an OCF in T5 in state S1 (b) Zoom around the fault occurrence.

Fig. 13 (a) illustrates the case of an OCF in T5 during the state S1 and Fig. 13 (b) is a zoom around the time of appearance of the fault. At $t = t_1$ the OCF is artificially generated when the “Fault Generation” signal passes from ‘0’ to ‘1’. Therefore, T5 is open from the falling edge of this signal, regardless of the control command computed by the control system (see Fig. 13(b)). At $t = t_2$, the measured output voltage ($v_o = 0$) and the estimated output voltage ($v_{oe} = V_{dc}/2$) are not equal. Thus, the incremental counter (Fig. 4) will be enabled. When its output “Cnr” signal will be greater than the predefined time threshold that is equal to $20\mu s$, the fault can be declared. Therefore, the signal “Fault



(a)



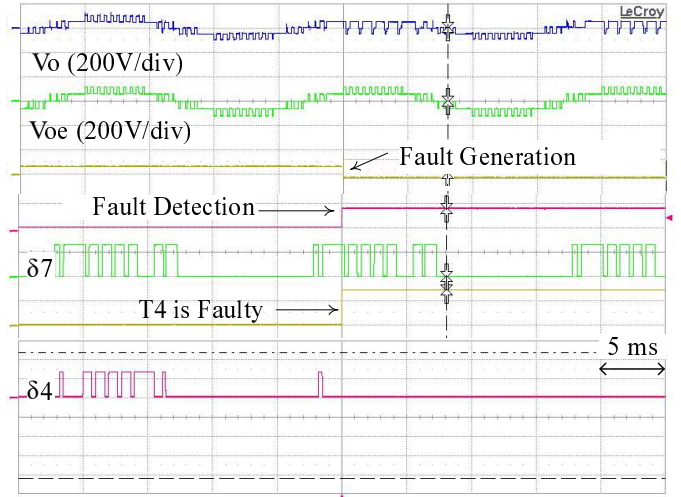
(b)

Fig. 14. (a) Experimental results for an OCF in T1 in state S2 (b) Zoom around the fault occurrence.

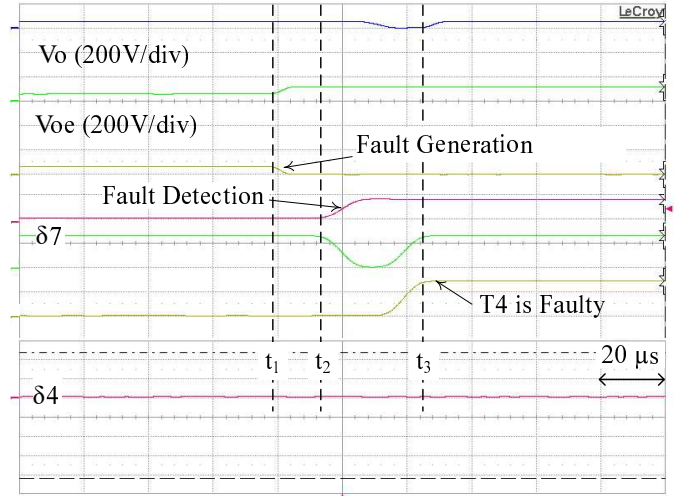
detection” goes to ‘1’. According to Fig.5, the FLA must compare the v_o and v_{oe} to find the faulty switch. In this case $v_o = 0$ that announces an OCF fault in T5 (see Fig.5). At $t = t_4$ the signal “T5 is faulty” is activated.

Fig. 14 and Fig. 15 respectively show the cases of an OCF in T1 and T4, consequently during state S2. This state is classified into group 3 which needs an additional action for fault localization. First, the case of an OCF in T1 is studied (Fig. 14), the fault is generated at $t = t_1$. At $t = t_2$, the measured output voltage ($v_o = V_{dc}$) and the estimated output voltage ($v_{oe} = V_{dc}/2$) are not equal. Therefore, the FDM activates the counter and when the time criterion is satisfied ($N = 20$ and $T_c = 1\mu s \rightarrow (NT_c = Cnt) > 20\mu s$) the signal “Fault detection” goes to ‘1’ and the OCF is declared. However, the faulty switch (T1 or T4) cannot be directly identified. Thus, the FLA forces $\delta 7$ to ‘0’ during the fault localization period ($[t_2, t_3]$ on Fig. 14(b)). As it can be seen in Fig. 14(b) in this time interval, the output voltage remains constant ($v_o = V_{dc}$) which means that “T1 is faulty”.

Now, the case of an OCF in T4 during state S2 is pre-



(a)



(b)

Fig. 15. (a) Experimental results for an OCF in T4 in state S2 (b) Zoom around the fault occurrence.

sented (Fig. 15). The OCF in T4 is generated artificially at $t = t_1$, thus the measured output voltage ($v_o = V_{dc}$) and the estimated output voltage ($v_{oe} = V_{dc}/2$) are not equal. Same as the fault in T1, the fault is detected when the time criteria ($Cnt > 20\mu s$) is validated. However, the faulty switch cannot be directly identified. Discrimination between the two potentially faulty switches (T1 or T4) must be realized. Thus, the control command of T7 is forced to ‘0’ during the fault localization period $[t_2, t_3]$. In these cases, the output voltage v_o goes to 0 volt and “T4 is faulty” goes to ‘1’ and thus the fault is correctly localized (Fig. 15 (b)).

VI. CONCLUSION

The Multilevel converters have been widely used in various applications. These converters have a considerable number of semiconductor switches that can cause faults and decrease the reliability of the converter hardware. Therefore, fault diagnosis is one of the most important challenges for systems that include a multilevel converter.

This paper proposes a switch open circuit fault diagnosis for a five-level H-bridge T-type multilevel converter. In a healthy mode of operation, depending on the direction of the output current, in some states, there is more than one switch in the current path. Therefore, in addition to the fault detection algorithm, the fault identification (location) algorithm is also required for proper diagnosis. The proposed method compares the measured output voltage and its desired value in real time to detect a switch OCF. According to the possible states (different voltage levels), there are three groups for fault detection and localization. For the faults in group 2, the fault diagnosis can be done in a single step. For the group 3 which involves two switches, the fault can be detected in the first step, and to identify the faulty switch, a second action is needed. One of the switches (chosen for possible identification purpose) must be turned off to localize the faulty switch. To avoid false FD due to the delay of the test bench components, a time criterion is also considered. Therefore, in any case, the first step is the fault detection method which is based on the observation of the output voltage value and the time criterion. The validity and performance of the proposed method are confirmed by simulations in Matlab Simulink and validated by some experimental tests. The implementation of the FD and FLA on an FPGA allows a real-time diagnosis.

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Florent Becker was born in France, in 1987. He received the M.S degree from Université de Nancy and Ph.D. Degree in Electrical Engineering from Université de Lorraine, IJL/GREEN, France in 2011 and 2017 respectively. Since 2017 he is working in French Naval Academy in Brest, France. His research interests are Fault Tolerant Control, Multi-Level Converter, multi-phase machine and Naval application.



Ehsan Jamshidpour received the Ph.D. degree in electrical engineering from the University of Lorraine, Nancy, France, in 2014 and the M.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2001. From 2003 to 2010, he was an Assistant Professor at the Institute for Energy and Hydro Technology, Iran. From 2016 to 2020, he was with "ECAM Strasbourg Europe" as a senior lecturer. In September 2020, he joined the University of Lorraine, Nancy, where he is currently an Assistant Professor. His main research interests

include electric motor drives, fault diagnosis of power electronic converters, and renewable energy.



Philippe Poure was born in 1968. He received the Engineering and Ph.D. degrees in electrical engineering from INPL-ENSEM-GREEN, Nancy, France, in 1991 and 1995, respectively. From 1995 to 2004, he was Associate Professor at the University Louis Pasteur of Strasbourg, France. In September 2004, he joined the Université de Lorraine, Nancy, France. Currently, he is Full Professor at the University of Lorraine. His research interests include fault diagnosis and fault-tolerant operation for electronic interfaces and power electronic converters, applied to

energy harvesting systems and power systems, respectively. He has authored or co-authored more than 150 international journals and conference papers.



Shahrokh Saadate Shahrokh SAADATE, born in Tehran/Iran on May 6th 1958, received his Master (Diplôme d'ingénieur/DEA) in Electrical Engineering (1982) from ENSEM/Lorraine University Nancy/France, PhD in Electrical Machines (1986) and "Habilitation à diriger les recherches" in Power Quality (1995), both in GREEN Laboratory, Lorraine University, Nancy/France. Currently he is Full Professor in "Génie Electrique", Electrical Engineering, in Lorraine University and researcher in GREEN Laboratory. His main research field is

Power Electronics and more specifically Power Quality, Renewable Energies and recently in Resiliency of the Self-Healing Multilevel Converters.