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Design and Experimentation of Inductorless Low-Pass NGD Integrated Circuit in 180-nm CMOS Technology

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Abstract—This paper introduces an innovative design of a low-pass (LP) negative group delay (NGD) integrated circuit (IC) in 180-nm CMOS technology. The LP-NGD circuit is an inductorless topology constituted by RC-network with CMOS metal-insulator-metal (MIM) capacitor and poly gate resistor. The design methodology is illustrated by considering the chip layout process. Then, the first run simulation is performed with the design rule check (DRC) and 2.5 mm × 2.2 mm layout versus schematic (LVS) approaches. The feasibility of the CMOS LP-NGD IC circuit implementation is validated with chip-on-board (CoB). The proof of concept (PoC) of the LP-NGD miniaturized circuit was tested in both S-parameter and time-domain. As expected, the calculated, simulated and experimented results of CoB showing NGD of about -10 ns over 12 MHz and -10 dB attenuation is confirmed. Moreover, time-domain investigations were also performed to show the feasibility of generating pulse and arbitrary waveform signal time-advance through the designed and fabricated LP-NGD CoB prototypes.

Index Terms— CMOS technology, Negative group delay (NGD), Low-pass (LP) NGD integrated circuit (IC), NGD miniaturized circuit, RC-network passive topology.

I. INTRODUCTION

THE performance and future of the electronic system are successfully increased with tremendous miniaturization

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thanks to the integrated circuit (IC) solution technology [1-2]. Following the traditional technology progress, recent survey reports the effectiveness of the miniaturization solution by implementation of inductorless circuit in CMOS technology [1]. Design solution directives were also stated on the effectiveness of the SiGe CMOS implementation of high-speed [2]. The CMOS design is the most promising, efficient, and good enormous trade-off solution in term of circuit miniaturization. So far, various classical electronic functions as amplifier [3-4], low-voltage signal processor [5], several aspects of filters [6-14], PLL [15], transconductors [16], were designed in CMOS technology are available in the literature. Design method of CMOS amplifier with precise and stable DC gain was introduced [3-4]. The expected advantages of CMOS technology are the low-power consumption [5-6] and compact [7] circuit design. One of most expanded circuit designs are expected for filters with different characteristics as continuous time [6,9], log-domain [7], AC-powered [8], nanometer technology [10-12], enhanced adaptive, Q-tuning scheme [13] and high dynamic range [14] filters. Despite the development of the CMOS design technology of analog circuit, the designability of certain unfamiliar analog functions as the low-pass (LP) negative group delay (NGD) circuits [17-20] remain one of open questions. Before the exploration of the solution, it is worth describing a brief state of the art on the NGD function.

The NGD function was initially experimented with negative group velocity (NGV) optical systems [21-22]. Because of its counterintuitive behavior the existence of the NGD function in electronic engineering become an attractive topic [23-31]. Accordingly, metamaterial based artificial and periodical transmission lines (TLs) operating with negative refractive index were designed to validate the NGD effect in the microwave area [22-27]. The metamaterial inspired NGD circuits were designed with resonator-based [28] and resistive left-handed circuits [29]. It was pointed out that the NGD effect enables to propagate superluminal pulse signals [30-33]. In addition, time-domain low-frequency (LF) experimentations allow to state that the NGD function is represented by the signature of output signals in time-advance compared to its input [34]. It was emphasized that such a counterintuitive effect is not in contradiction with the causality [34]. Then, the

interpretation of the unfamiliar NGD function remains a breakthrough for some electronic design researchers [35-37]. But the applications of the NGD circuits are generally limited to the circuit size. Different topologies of microwave compact circuits were proposed to overcome the challenge in terms of the miniaturization [36-37]. Following this compactness challenge, innovative design and implementation and test of 180-nm CMOS technology inductorless LP-NGD circuit are investigated.

The present paper is organized in six different sections which are technically aimed as follows: Section II focuses on the description of the low-pass (LP) NGD inductorless topology. Section III presents the design, and pre- and post-simulation processes of the LP-NGD CMOS IC proof of concept (POC). Section IV explains the design methodology of 180-nm technology CMOS IC as the POC of the inductorless LP-NGD topology. Section V focuses on the implementation technique of the chip on board (CoB) test vehicle will be described. Section VI discusses the validation results. Then, Section VII finalizes the paper with a conclusion.

II. DESCRIPTION OF THE RC-NETWORK BASED LP-NGD CIRCUIT UNDER STUDY

This section describes the LP-NGD passive circuit analytical design. After the topological description, the LP-NGD analysis is introduced. Then, the design formulas allowing to determine the resistor and capacitor in function of the expected NGD characteristics will be presented.

A. Description of the Inductorless LP-NGD Circuit and Ideal Specifications

Fig. 1 introduces the scheme of the inductorless two-port circuit under study. This passive topology is composed by RC parallel network and a shunt R_1 resistor. Acting as a two-port passive system, with the Laplace variable, $s = j\omega$ and reference impedance, $R_0 = 50 \Omega$, the circuit will be analyzed via its S-parameter equivalent model:

$$[S(s)] = \begin{bmatrix} S_{11}(s) & S_{12}(s) \\ S_{21}(s) & S_{22}(s) \end{bmatrix} \quad (1)$$

where:

$$S_{11}(s) = \frac{R_0^2 + (R + R_1)(R_0 + R_1) - [R_1(R_0 + R_1) + R_0^2]RCs}{D(s)} \quad (2)$$

$$S_{12}(s) = S_{21}(s) = \frac{2R_0R_1(1 + RCs)}{D(s)} \quad (3)$$

$$S_{22}(s) = \frac{(R_1 - R_0)(R + R_0) - R_1^2 + [R_1(R_0 - R_1) - R_0^2]RCs}{D(s)} \quad (4)$$

and:

$$D(s) = (R + R_0)(R_0 + R_1) - R_1^2 + [R_1(R_0 - R_1) + R_0^2]RCs. \quad (5)$$

To perform the LP-NGD analysis, we need the magnitudes, $S_{mn}(\omega) = |S_{mn}(j\omega)|$ ($m, n = 1, 2$), phase, $\varphi(\omega) = \arg[S_{21}(j\omega)]$ and the associated GD response versus the angular frequency, ω , defined by:

$$GD(\omega) = \frac{-\partial\varphi(\omega)}{\partial\omega}. \quad (6)$$

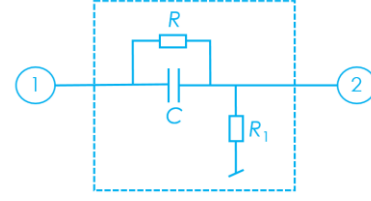


Fig. 1. Inductorless two-port circuit under study.

B. Graphical Specifications of LP-NGD Function

Fig. 2(a) highlights the ideal GD response of LP-NGD circuit. This system can be assumed as a LP-NGD function if the very low frequencies $GD, GD(\omega \approx 0) < 0$. In addition, we can find an angular frequency, ω_0 , verifying $GD(\omega_0) = 0$, $GD(\omega \leq \omega_0) \leq 0$ and $GD(\omega > \omega_0) > 0$.

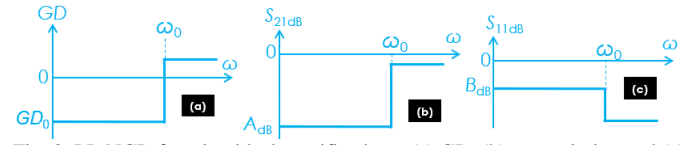


Fig. 2. LP-NGD function ideal specifications: (a) GD, (b) transmission and (c) reflection coefficients.

Then, as shown in Fig. 2(b), the transmission coefficient is non-zero, $S_{21}(\omega \approx 0) = A < 1$, and the reflection coefficient illustrated by Fig. 2(c) is higher than an expected matching level, $S_{11}(\omega \approx 0) = B < 1$ in function of the expected real parameters, A and B .

C. Design Formulas of the LP-NGD Circuit Resistors and Capacitor

The design of the RC-network LP-NGD circuit presented by Fig. 1(a) can be performed in function of the desired specifications at very LFs. The main specification and desired parameters can be attenuation, A , or reflection matching, B , and the NGD value, $GD_0 < 1$, or the NGD cut-off frequencies, $\omega_0 = 2\pi f_0$. Accordingly, with the desired values of A and B , by exploiting the input or output reflection coefficients written in equations (3) or (4) we can calculate R_1 with the following design formulas, respectively:

$$R_1 = R_0 A / (1 - A - B) \quad (7)$$

or

$$R_1 = R_0 (1 + B) / (1 - A - B). \quad (8)$$

The other resistor can be calculated from equation:

$$R = [2R_0R_1 + A(R_1^2 - R_0^2 - R_0R_1)] / [A(R_0 + R_1)] \quad (9)$$

and the capacitor:

$$C = [R_1(R_1 - R) - R_0(R + R_0 + R_1)]GD_0 / [R^2(R_0 + R_1)]. \quad (10)$$

Thanks to the established synthesis formulas, ideal circuit parameters are calculated in the following subsection from the desired NGD specifications.

D. Synthesis Result of Ideal LP-NGD Circuit

The circuit parameters were calculated by using the synthesis formulae of the LP-NGD POC given earlier in equation (7) for R_1 , equation (9) for R and equation (10) for C . The considered NGD specifications defined following the diagrams proposed

earlier by Figs. 3 are shown in Table I. Then, the ideal component parameters are calculated by considering the LP-NGD circuit synthesis formulae. From the synthesized circuit, we designed the POC of LP-NGD IC in 180-nm CMOS technology. The following sections describe the design and simulation methodology.

TABLE I
PARAMETERS OF THE LP-NGD IC POC

Parameter	Name	Chosen value
NGD cut-off frequency	f_0	20 MHz
NGD value	GD_0	-5 ns
Attenuation	A	-6.8dB
Reflection	B	-20dB
Resistor	R_0	35 Ω
	R_1	50 Ω
Capacitor	C_0	273 pF

III. CADENCE SCHEMATIC METHODOLOGICAL DESIGN, AND PRE- AND POST-SIMULATION PROCESSES

The present section describes the different steps of the design and simulation methodological processes in the environment of IC simulator commercial tool CADENCE-VIRTUOSO®. The design is aimed to the CMOS IC implementation in 180 nm technology.

A. Methodology of the Pre- and Post-Simulations, and the Layout DRC and LVS Check

The design process and simulation methodology of the LP-NGD CMOS IC POC can be summarized by the following description:

- **Process 1:** The design of lumped circuit constituted by the resistor and capacitor for library available in the environment of the CADENCE-VIRTUOSO® commercial software. The choice of components has to be made with respect to the criteria of our 180 nm technology founder and also in order to optimize the final IC prototype performance.
- **Process 2:** In the following process, the pre-simulation refers to the computational results from the schematic diagram designed in the environment of the CADENCE-VIRTUOSO® commercial software. Fig. 8 present the designed schematic corresponding to the LP-NGD topology introduced by Fig. 1. At this stage, the study does not involve the layout design. After the pre-simulation, the equivalent layout was drawn and simulated.
- **Process 3:** The post-simulation consists in considering the preliminary NGD IC layout displayed by Fig. 3. For the present case of study, the post-simulation was carried out by considering an active LP-NGD circuit.
- **Process 4:** After the preliminary drawing of the layout, the design rule check (DRC) and LVS check of the layout is needed to ensure the consistency between the layout and the schematic. The DRC is a program that uses layout database to check every design rule involved in layout. For example, the width and spacing of each wire on the layout to ensure that they do not violate the specified minimum value. The DRC ensures that the design can be manufactured within the limits of production process. We must verify the LVS check result of the considered LP-NGD layout design. After the layout drawing is completed, open calibre software and check LVS

according to the setting. The LVS inspection result must be consistently validated.

- **Process 5:** After the layout drawing is completed, open calibre software and check the DRC according to the setting must be investigated. The validity of the DRC examination except for the density of poly layer must be reported. Then, the LVS check is to compare the circuit diagram with the circuit extracted from the layout, and its method is usually to compare the netlist of the two. The result of comparison can be completely consistent or not completely consistent, and the designer shall make necessary modifications to the errors shown.

To start the process of the LP-NGD POC under study, the schematic design of our CMOS IC POC will be introduced in the next subsection.

B. Description of the Circuit Design in the Environment of CADENCE-VIRTUOSO® Simulator

Following the previously introduced methodology, the preliminary IC schematic was designed. Fig. 3 displays the schematic of the simulated LP-NGD passive circuit. The passive circuit structure is designed in the environment of the CADENCE-VIRTUOSO® simulation software. The IC model of lumped resistor and capacitor components available in the CADENCE-VIRTUOSO® library were implemented.

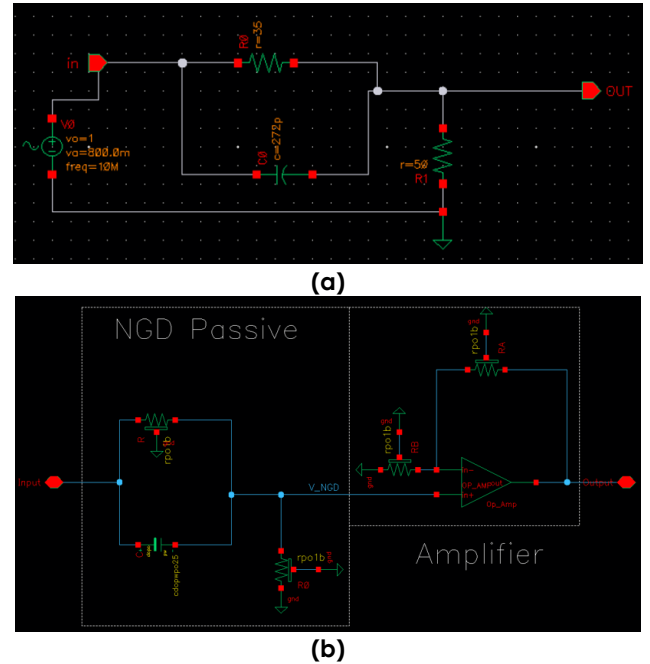


Fig. 3. VIRTUOSO® schematic of the LP-NGD circuit.

TABLE II
OPERATIONAL AMPLIFIER PERFORMANCE INDEX

Type	Name	Value
Voltage	Power supply	1.8 V
Gain-Bandwidth		119.6 MHz
Gain/Attenuation	DC gain	83.2 dB
	Common mode rejection ratio	79.1 dB
	Power supply rejection range	-26 dB @ 10 MHz
Phase	Phase margin	45°
-	Slew rate	33.99 V/ μ s
-	Noise equivalent input	89.9 nV/sqrt(Hz) @ 1 kHz

However, the passive circuit shown in Fig. 3 is naturally lossy. In order to compensate the attenuation loss, an active circuit with gain $g=1/A$ of about 10 dB was designed. The performances of the operational amplifier constituting the active IC POC were chosen with respect to the specifications given in Table II. More description about the operational amplifier and active IC design will be explained in the following section. Then, after the schematic to layout conversion, the resistor capacitor layouts to be presented in described in the following section.

IV. DESIGN METHODOLOGY OF THE INDUCTORLESS LP-NGD IC IN 180-NM CMOS TECHNOLOGY

The design methodology of the inductorless LP-NGD IC is described in the present subsection. The proof-of-concept layout design in 180-nm CMOS technology will be introduced. Hence, the implementation of each components constituting the CoB of the LP-NGD POC will be explained.

A. Description of the Layout

Fig. 4 shows the layout of CMOS-NGD circuit, which adopts 180 nm technology. The overall size of the layout is 2.5 mm \times 2.2 mm. The outside of the layout is the pad of input, output, V_{DD} , GND and other interfaces, as well as the electrostatic discharge (ESD) protection unit. The layout is divided into two parts, the upper part is the active unit, and the lower part is the passive unit. It can be seen that the area occupied by the capacitor in the layout is the largest. This is also due to the MIM capacitor used in the IC process library. Compared with MIM capacitor, poly-poly capacitor has complex fabrication process, and the capacitance value will change with the power supply V_{DD} , and the parasitic capacitance is also large, so the linearity of the MIM capacitor is better than poly-poly one.

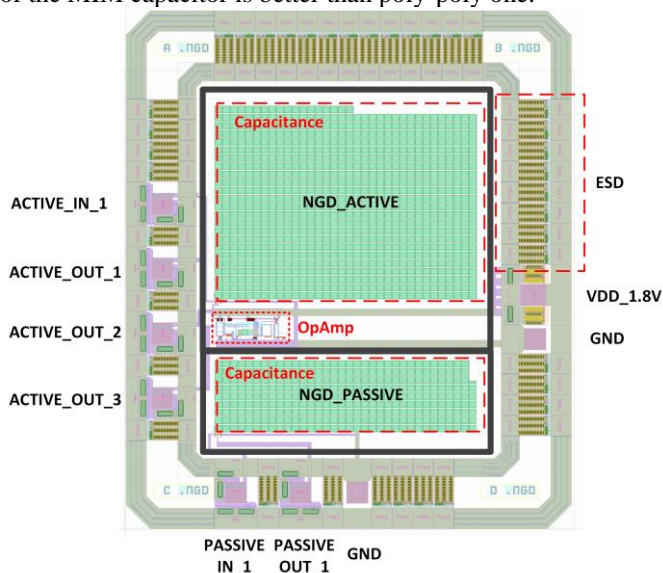


Fig. 4. Layout of the LP-NGD circuit chip.

The poly cap is usually used in processes above 500 nm, but rarely used in modern analog CMOS processes. In order to measure the performance of the circuit in detail, more output PADs are added. In addition, because the resistance of the active NGD unit is small, in order to prevent excessive power consumption, a 60 Ω current limiting resistor is added before the actual circuit, so an output PAD (ACTIVE_OUTPUT_1) is

derived between the input PAD and the circuit layout, and this signal is used as the actual input of the active circuit. The whole layout has 2 input ports, 4 output ports, 1 V_{DD} port, and 2 GND ports. The overall chipset size is 2.5 mm \times 2.2 mm.

B. Design of CMOS Resistors Layout

The resistor implemented in the layout of Fig. 5 is poly gate resistance, and the typical value of the resistance is 2-3 Ω / square. It means that the resistance value is 2-3 Ω under the minimum square area of the manufacturing process. For example, if the design is 180 nm process, the unit resistance value of 180 nm \times 180 nm is 2-3 Ω . It is noteworthy that the error of poly resistance is small, the temperature coefficient can be controlled, the parasitic resistance is small and the matching is good. But the square resistance of the poly resistor is small, it is not suitable for making high resistance resistor.

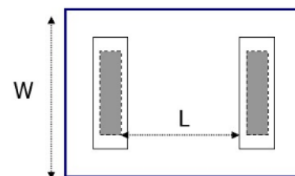


Fig. 5. Resistance layout structure diagram of resistance unit.

In this basic resistor layout, a layer of polysilicon is deposited on the substrate, and then an oxide layer is covered on the polysilicon layer to form an isolated insulating layer, and then the contact holes for connection are etched on the oxide layer. Generally, the contact holes are located at both ends of polysilicon. Just like the capacitance layout, because the resistance value of a single resistance unit is small, it is necessary to connect the contact holes of several resistors to form the resistors with different resistance values.

C. Design of Constituting CMOS Capacitor

Fig. 6 represents the layout design of the capacitors constituting the LP-NGD circuit. The inner part of the layout is divided into two parts, the upper part is the active unit, and the lower part is the passive unit. It can be seen that the capacitance in the layout occupies the largest area, which is also due to the use of metal-insulator-metal (MIM) capacitor in this IC process library.

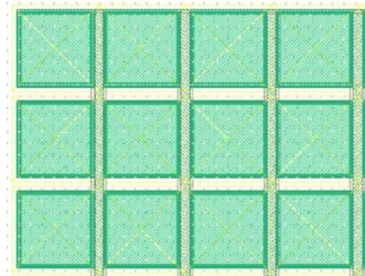


Fig. 6. MIM capacitor layout structure (1 fF/ μm^2).

By using metal as two electrodes, the capacitor device with MIM structure can effectively reduce the parasitic capacitance and the contact resistance between the two electrodes of the capacitor, with high accuracy. Therefore, the high capacitance density MIM capacitor with strong conductivity and no loss has become a new type of capacitor device to replace the traditional integrated circuit capacitor. In the CMOS circuit design, the type of devices used usually

depends on the model library file provided by the manufacturer. By selecting the appropriate device unit from the model library, the manufacturer will also provide the detailed parameter values of each component for selection, so the actual library should prevail. MIM capacitor is equivalent to a parallel plate capacitor. The gap between the top two layers of metal is large, which leads to the smaller capacitance value per unit area of the capacitor. However, the capacitance value in negative group delay circuit is generally larger. Therefore, in order to obtain the required large capacitance value, it is necessary to connect the metal layers of several capacitor units to expand the area of the metal surface, so as to form a capacitor with large capacitance value.

D. Operational Amplifier Design

Fig. 7(a) shows the scheme of active LP-NGD circuit. The amplifier is a basic CMOS two-stage Miller compensated operational transconductance amplifier, which mainly includes four parts: the first stage input stage amplifier circuit, the second stage amplifier circuit, the bias circuit and the phase compensation circuit. As illustrated by Fig. 7(a), the input stage amplifier consists of M1-M5. Compared with single ended input, differential input can effectively suppress common mode signal interference; M3 and M4 current mirrors are active loads; M5 provides constant bias current for the first stage. The operational amplifier layout is depicted in Fig. 7(b). The output stage amplifier consists of M6 and M7. M6 is a common source amplifier, and M7 provides a constant bias current for it and serves as the second stage output load. The phase compensation circuit consists of M14 and C_C . M14 works in the linear region and can be equivalent to a resistor. It is bridged with capacitor C_C between the second input and output to form R_C Miller compensation.

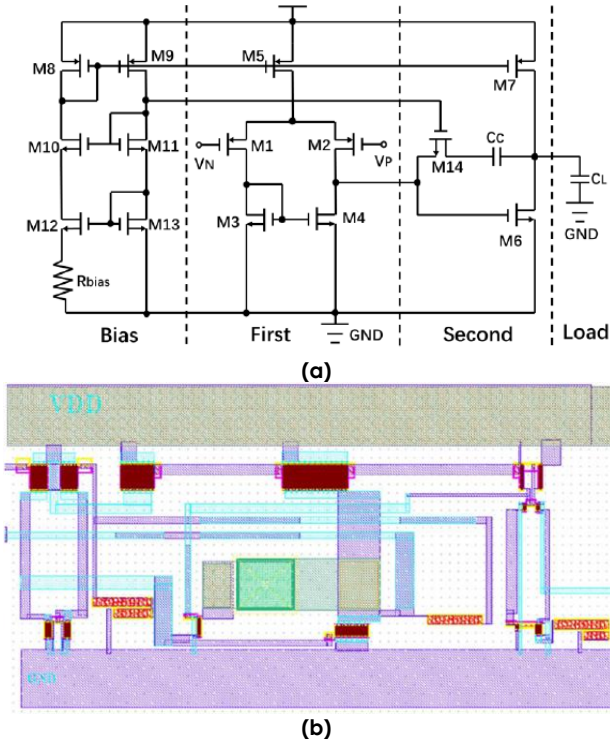


Fig. 7. Operational amplifier (a) scheme and (b) layout.

The bias circuit consists of M8-M13 and R_B , which is a common source and common gate current source. M8 and M9 have the same aspect ratio. Compared with M13, the resistor R_{Bias} is added to the source of M12 to form a micro current source, which generates current I_B . Symmetrical M11 and M12 form a common source and common gate structure to reduce the current error caused by channel length modulation effect. At the same time, it also provides bias voltage for M14 gate. The specific circuit parameters are shown in Table III.

TABLE III
STRUCTURE PARAMETERS OF ACTIVE LP-NGD CIRCUIT SHOWN IN FIG. 7(A)

Circuit part	Type	Name	Value (Ω)
NGD passive	Resistor	R	25 Ω
		R_0	20 Ω
	Capacitor	C	720 pF
Operational amplifier	W/L (μm)	M ₁ M ₂	84/1
		M ₃ M ₄	18/1
		M ₅	168/1
		M ₆	72/1
		M ₇	336/1
		M ₈ M ₉	14/1
		M ₁₀ M ₁₁	3/1
		M ₁₂	12/1
		M ₁₃	3/1
		M ₁₄	10/1
Active circuit	Resistor	R_A	7 k Ω
		R_B	5 k Ω
		R_{Bias}	7 k Ω
	Capacitor	C_C	780 fF
	Voltage	V_{DD}	1.8 V

The practical feasibility of the LP-NGD test vehicle design and fabrication process will be examined in the next section.

V. DESCRIPTION OF THE INDUCTORLESS LP-NGD CHIP ON BOARD (COB) AND PCB TEST VEHICLE

This section describes the CMOS CoB package of the inductorless LP-NGD prototype introduced by Fig. 1 implemented in 180 nm technology. We remind that CoB is an encapsulation method (Fig. 8(a)). The bare chip is adhered to the interconnection substrate with conductive or non-conductive adhesive, and then wire bonding is carried out to realize its electrical connection. The CoB integration in the PCB test vehicle will also be presented.

A. Methodology of the Fabrication and Integration Process

A particular attention must be paid on the board integration of the previously described chip before the test. The CoB integration process was performed with respect to the following phases:

- **Phase 1:** The CoB process first covers the silicon wafer with a thermally conductive epoxy resin (generally epoxy resin doped with silver particles) on the surface of the substrate.
- **Phase 2:** The circuit was placed the silicon wafer directly on the surface of the substrate.
- **Phase 3:** The circuit was heated until the silicon wafer is firmly fixed on the substrate.
- **Phase 4:** Then, we use wire bonding to directly establish an electrical connection between the silicon wafer and the substrate.

The next subsection will highlight the processes of the fabricated CoB.

B. Description of the Designed and Manufactured LP-NGD CoB

The LP-NGD CoB prototype was designed and manufactured following the previous integration process. Figs. 8 show the photographs of the designed and manufactured chip packaging. To realize conveniently the test, the option of CoB was used. The top view of the uncapped CoB is presented by Fig. 8(b) and Fig. 8(c). Fig. 8(d) highlights the size of the miniaturized CoB. The fabricated test vehicle of PCB integrating the obtained CoB will be introduced in the following subsection.

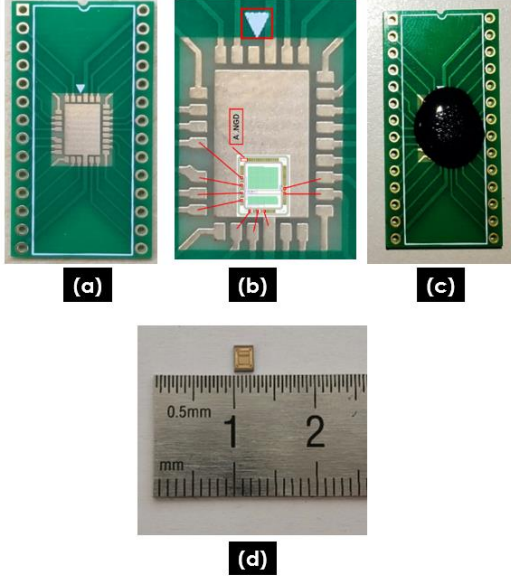


Fig. 8. (a) Dielectric board for packaged chip, (b) correspondence between pins and chip ports, (c) finished chip package and (d) unpackaged chip.

VI. SIMULATED AND EXPERIMENTAL VALIDATION RESULTS

The present section deals with the validation of the unfamiliar LP-NGD function with CMOS CoB implemented in 180 nm technology. Then, the confirmation of the LP-NGD is based on the comparative study of simulated and measured results. The next subsections are dedicated to the examination of the results.

A. Frequency Domain (FD) Results

The LP-NGD FD verification of the CMOS CoB prototype is based on the voltage transfer function (VTF) analysis in order to consider the low frequencies. The following paragraphs introduce the obtained FD results.

1) Description of the VTF Experimental Setup

Fig. 9 depicts the FD validation experimental setup of the LP-NGD CMOS CoB prototype. The VTF experimental validation was carried out using an arbitrary signal generator and an oscilloscope. The signal generator generates sine signal which serves to sweep the frequency from $f_{min}=1$ kHz to $f_{max}=20$ MHz. The oscilloscope enables to simultaneously measure the amplitudes and phases of both the input and output voltages. The VTF magnitude and the GD at the frequency sample, f_n , (with subscript n varied from 1 to 100) are determined from the following equations:

$$VTF_{measured}(f_n) = V_{out_{max}}(f_n) / V_{in_{max}}(f_n) \quad (11)$$

$$\varphi_{measured}(f_n) = \Delta\varphi(f_n) \quad (12)$$

$$TL_{measured}(f_n) = 20\log[VTF_{measured}(f_n)] \quad (13)$$

$$GD_{measured}(f_{n=\{2, \dots, n_{max}\}}) = \frac{\varphi_{measured}(f_n) - \varphi_{measured}(f_{n-1})}{2\pi(f_n - f_{n-1})} \quad (14)$$

In order to ensure the experiment precision, T-SMA connectors are directly used between the tested circuit without cables during the passive LP-NGD FD test, and the SMA cables that transmit input and output signals have same length. The specifications of the employed equipment's are indicated by Table IV. For the furthermore curious validation of the LP-NGD function, the obtained FD results from the CMOS CoB will be discussed in the next paragraphs.

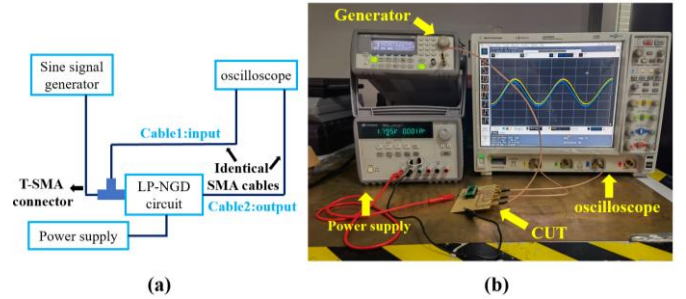


Fig. 9. FD experimental setup of LP-NGD CMOS CoB.

TABLE IV

REFERENCES OF THE TEST EQUIPMENT

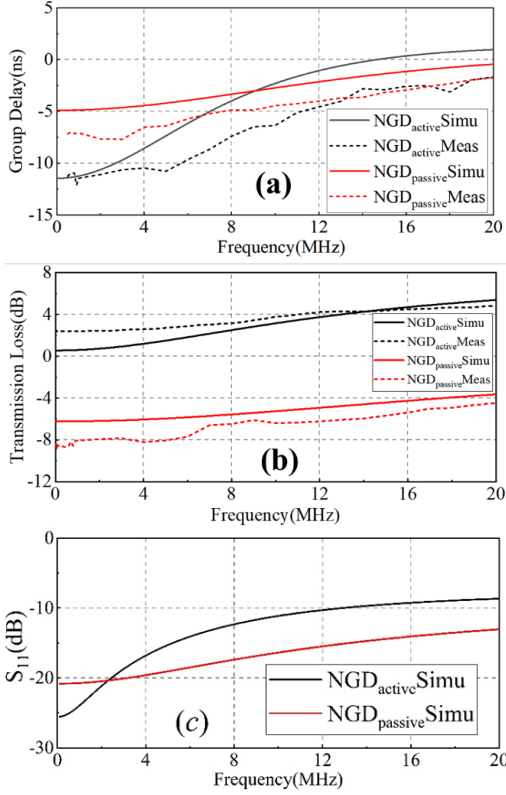
Name	Model/Type	Specifications
Power supply	KEYSIGHT E3631A	80 W, 25 V
Signal source	Agilent 33220A	20 MHz, 14-bit, 50-MSa/s
Oscilloscope	Agilent DSO9404A	4 GHz, 20 GSa/s

2) LP-NGD CMOS CoB Prototype FD Validation Results

As mentioned in the previous paragraph, the FD validation is based CADENCE® simulation and VTF experimentation. Fig. 10 presents the comparisons of the simulated active results (“NGD active Simu.”, black solid line), the measured active results (“NGD active Meas.”, black dotted line), the simulated passive results (“NGD passive Simu.”, red solid line) and the measured passive results (“NGD passive Meas.”, red dotted line). As seen in Fig. 10, from 100 kHz to 6 MHz, the group delay of active LP-NGD circuit is better than -10 ns, and the transmission loss is about 2.4 dB to 2.8 dB. From 100 kHz to 11 MHz, the group delay of active LP-NGD circuit is better than -5 ns, and the transmission loss is about 2.4 dB to 4 dB. Then, it can be seen from Fig. 10(c) that the reflection coefficients of the LP-NGD CMOS CoB prototype are better than -20 dB.

The differences between the simulation and experimental results are due to the undesired degradations from interconnect structure (generator, wire, connectors, ...), and also the IC fabrication imperfections. Moreover, the tolerance of the poly gate resistance used in the LP-NGD CMOS layout is about 10%, in the future design, the more accurate process library will be used to ensure the consistency of measurement results. Table V introduces the comparison of the investigated CMOS NGD circuit and the literature [18-20,38]. It can be pointed out that the proposed CMOS NGD circuit allows to achieve a mm level size while other NGD circuits have a cm level size. The active CMOS technology compensates the insertion loss to 2.4 dB, the GD reaches -11 ns, and the reflection loss reaches -20 dB. The bandwidth of the active CMOS circuit is up to 20 MHz. In

general, this CMOS NGD has better insertion loss, better reflection coefficient and small size compared to the other literatures.



Figs. 10. Comparisons of passive and active NGD frequency performance: (a) GD, (b) transmission and (c) reflection loss.

TABLE V
COMPARISON BETWEEN THE PROPOSED CMOS NGD AND THE EXISTING ONES

References	GD_n	BW	S_{21} (dB)	S_{11} (dB)	Size
[18]	-40 μ s	1 kHz	-21	-0.8	10 mm \times 17 mm
[19]	-0.25 s	1.5 Hz	6	-0.01	25 mm \times 33 mm
[20]	-1.96 ns	75 MHz	-9.8	-7.1	29 mm \times 18 mm
[38]	-1 ns	46 MHz	-2.5	-12	centimeter level
This work	-11 ns	20 MHz	2.4	-20	2.5 mm \times 2.2 mm

B. Time-Domain (TD) Validation Results

The present subsection is dealing with the complete validation of the LP-NGD IC CMOS CoB. This ultimate validation is focused on the TD investigation with different input test signals. The TD experimental setup of LP-NGD CMOS CoB is the same as the setup in Fig. 9 except the input signals.

1) Time-Domain Validation Results of LP-NGD CMOS IC with Sinc Test Signal

In this case of experimental study, the input test signal is chosen with sinc waveform having amplitude about 120 mV and pulse time duration of about 500 ns. Therefore, we obtain the transient signal results displayed by Figs. 11. The input signal is plotted in black solid line. Three different output signals were recorded: The output signal of the passive CMOS IC prototype from measurement is plotted in red dotted line, The output signal of the active CMOS IC prototype is plotted in blue dotted line, Then, the simulated output one of the active CMOS IC prototype from ADS® is plotted in green dotted line. As expected, the output signal from the active CMOS IC appears in time-advance compared to the input one. We can

emphasize from Fig. 11(b) that the output signal is once again in time advance compared to the input one. Table VI compares the time-advances between the input and output ones. This sinc TD result provides a further confident on the feasibility of the CMOS IC design of LP-NGD prototype under study.

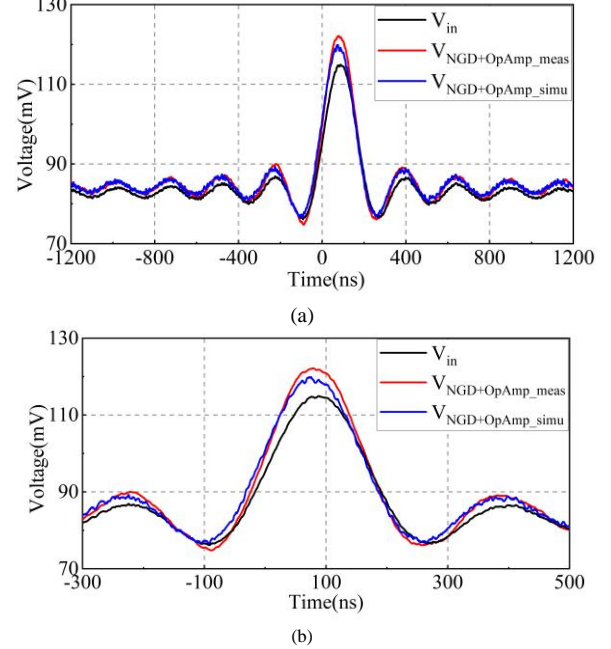


Fig. 11. Time domain results of sinc signal: (a) large and (b) narrow time window plots.

TABLE VI
COMPARISON OF SIMULATED AND EXPERIMENTED NGD PERFORMANCES

Tested signal	V_{in}	V_{NGD+OP_meas}	V_{NGD+OP_simu}
Time-advance GD (ns)	-	7.6	8.5

However, further question may still be wondered at this stage about the time advance as the sinc input signal is defined as predictable waveform with analytical expression. This curious question leads to the imagine a more convincing TD experimentation. As a solution against all the scientific curious remark, we performed another final test with completely arbitrary waveform signal whose results are discussed in the following last paragraph.

2) Time-Domain Validation Results of LP-NGD CMOS IC with Arbitrary Waveform Signal

Figs. 12 show ultimate validation results of the LP-NGD function with the CMOS IC prototype by injecting a completely arbitrary waveform input signal. The simulated and experimented results are in good correlation. The maximal time duration of the TD plot is fixed to $t_{max}=17 \mu$ s. The test signal presents an amplitude fluctuating between 7 mV and 15 mV as shown by Fig. 12(a). The present study was performed with the passive CMOS IC prototype for this reason the outputs are attenuated compared to the input signals.

The amplification ratio is determined in the process of CMOS circuit design, but in the actual manufacturing process, there is error in the resistance value, which leads to the actual amplification ratio is slightly small. In the future, we will consider this situation and increase the amplification ratio in the design.

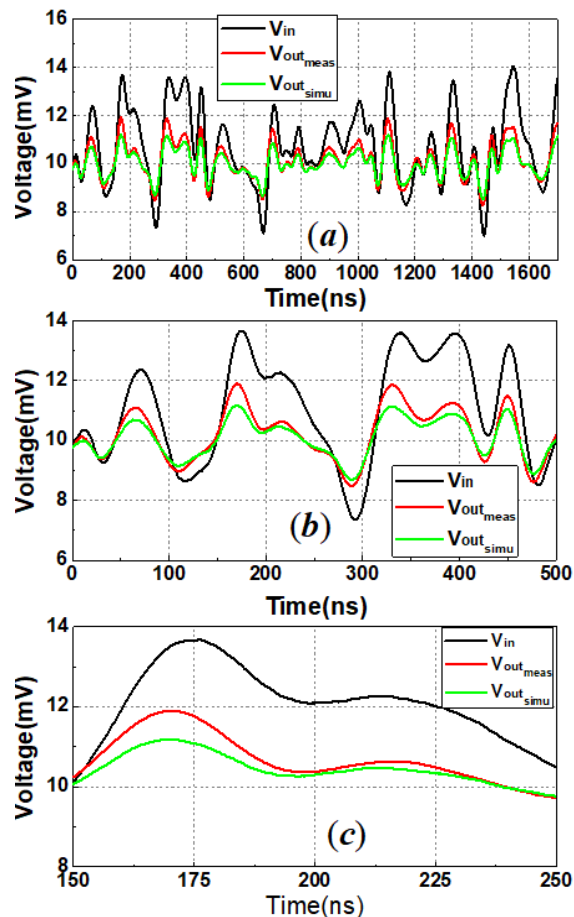


Fig. 12. Time domain results of arbitrary waveform with smoothed signals: (a) very large, (b) large and (c) narrow time window plots.

TABLE VII
COMPARISON OF SIMULATED AND EXPERIMENTED OUTPUT SIGNAL
TIME-ADVANCE

Tested signal	V_{in}	$V_{NGD\ meas}$	$V_{NGD\ simu}$
Time-advance GD (ns)	-	-6.6	-6.4

Table VII summarizes the comparison between the amplitudes and time advance of the simulated and measured outputs. We can understand from Fig. 12(b) and Fig. 12(c) that if we normalized the input and output signals, we can observe the time advance effect. Accordingly, we can evaluate the time advance from the signal peak instant time indicated in Table VIII. One of the most challenging aspect of the LP-NGD circuit design is the noise effect. We have also answered to the ambiguity and curious questions about the noise issue. Doing this, a challenging test was performed with noisy arbitrary waveform signal. It can be pointed out from this plot that despite the noise effect, the simulated and measured output of the CMOS IC prototype appear with the time-advance signature.

VII. CONCLUSION

An innovative investigation on the 180 nm CMOS design, implementation and test of the LP NGD IC is developed. The specificity of the LP NGD function represented by the RC-network based LP NGD circuit is presented. Then, the design methodology of the LP NGD CMOS circuit is described in function of the technological requirement. The different

processes of the step as the chip design including the DRC and LVS consideration are described.

A prototype of 2.5 mm \times 2.2 mm chip layout is fabricated as LP NGD IC prototype. The CMOS design feasibility is validated by a good correlation between the calculation, simulation and measurement in both frequency and time-domain. Different TD investigations confirm the time advance signature related to the LP-NGD behavior of the passive and active CMOS IC prototypes. It was innovatively also demonstrated experimentally the feasibility of the CMOS IC design and fabrication to operate with noise arbitrary waveform signal.

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