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Theory and Original Design of Resistive-Inductive Network High-Pass Negative Group Delay Integrated Circuit in 130-nm CMOS Technology

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ABSTRACT This paper develops an original design method of high-pass (HP) negative group delay (NGD) integrated circuit (IC). The considered HP-NGD IC is based on a passive topology which is essentially composed of resistor-inductor (RL) network. The paper presents the first time that an unfamiliar HP-topology is designed in miniaturized circuit implemented in 130-nm CMOS technology. The theory of unfamiliar HP-NGD topology based on the voltage transfer function (VTF) analysis is elaborated. The design equations with synthesis formulas of the resistor and inductor are established. The HP-NGD IC CMOS design methodology is introduced. The feasibility of the miniature NGD IC implementation is approved by design rule check (DRC) and layout versus schematic (LVS) approaches. The HP-NGD passive IC is designed in 130-nm CMOS technology. The HP-NGD topology is constituted by RL-network based on CMOS high Ohmic unsalicyded N + poly resistor and symmetrical high current spiral inductor. Then, the schematic and layout simulations are presented. The validity of the 130-nm CMOS HP-NGD design is verified by the investigation of $225 \mu\text{m} \times 215 \mu\text{m}$ chip two different miniature circuit proofs-of-concept (POC). The HP-NGD behavior is validated by comparison between the calculated, and schematic and post-layout simulations of the HP-NGD POCs carried out by a commercial tool. As expected, the group delay and VTF magnitude diagrams are in very good correlation. HP-NGD optimal value, NGD cut-off frequency and attenuation, of about (-31 ps, 141 MHz, -3 dB) and (-47 ps, 204 MHz, -5 dB) are obtained from the miniature POCs.

INDEX TERMS 130-nm CMOS technology, design method, negative group delay (NGD), high-pass (HP) NGD function, HP-NGD theory, integrated circuit (IC) design, synthesis equation, RL-network passive topology, miniature circuit.

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I. INTRODUCTION

The modern communication system evolution depends fundamentally on the research progress in term of electronic

function design. Among the existing electronic function, the negative group delay (NGD) is the less familiar to most of engineers. Therefore, academic research on NGD circuit engineering is necessary.

A. OVERVIEW ON NGD CIRCUIT APPLICATION IN ELECTRONIC ENGINEERING

Recent studies report potential applications of unfamiliar negative group delay (NGD) circuits for the improvement of performance of diverse electronic and communication devices [1], [2]. Among the NGD potential applications, an innovative design method of antenna system for multiband wireless applications [2] was developed. An innovative synthesis method of RF and microwave phase shifters operating independently to the frequency was introduced [3], [4]. Novel design of unconventional high Q series negative capacitor as non-Foster components was also presented in [5], [6]. The most natural applications of NGD circuits are the delay equalization or merely the delay cancellation in the electronic systems [7], [8]. Promising improvement the area of electronic communication engineering is particularly expected with the NGD equalization technique. For example, it enables to correct and to reduce the undesirable effects of signal distortion [7], [8]. Furthermore, the NGD equalization technique allows to cancel out as the delays induced by electronic interconnects [9], [10]. Moreover, we can insert NGD circuits in cascaded upstream or downstream to reduce the group delay (GD) induced by electronic communication systems [11], [12]. The diversity of potential applications notably in the area of electronics and communication engineering constitutes the main motivation factor to pursue the research work on the NGD engineering.

B. STATE OF THE ART ON NGD CIRCUIT ENGINEERING

Nevertheless, because of its counterintuitive property, so far, few electronic design and fabrication engineers are familiar to the NGD circuit designing. For this reason, further academic and more didactical research must be developed for the non-specialist engineers to open world widely the NGD engineering.

The NGD function was initially experimented with optical system operating with negative group velocity (NGV) [13], [14]. Then, the existence of the NGD function was an attractive topic for some curious RF and microwave design researchers. It was found that the negative refractive index (NRI) metamaterials are susceptible to operate with NGD effect [15]–[17]. Some remarkable microstrip microwave passive circuits with left-handed metamaterial structures were designed and experimented in the microwave frequency range [15]–[20]. The NRI metamaterials based NRI circuits were initially implemented with periodical passive cells [16], [17]. To overcome to such technical bottleneck, deeper design study of lumped circuits was performed based on the equivalent resonant circuit approach. The topology of split ring resonator based microstrip structure [18] was identified as one of the most elementary

NGD cells. However, it was emphasized that the metamaterial based NGD passive circuits [15]–[18] are either significantly lossy or implemented with large size printed circuit boards (PCBs). Then, more complex microwave function was innovatively imagined with tunable metamaterial resonator using varactor diodes [15]. Another variant of metamaterial NGD circuit with resistive lossy left-handed transmission lines (TLs) was proposed [20]. To overcome the challenge in term of size reduction, NGD compact circuit designs based on TL elements were raised last decade [21]–[23].

Despite the progress of the microwave NGD circuit design methods and identified passive circuit topologies, there is a lack of understanding about the basic physical meaning of the NGD function.

C. NGD CIRCUIT TYPE CLASSIFICATION

To answer to such a curious question, an innovative pedagogical theory enabling to classify the different categories of NGD topologies was initiated [24]. This fundamental NGD circuit theory was inspired from the similitude with the filter theory [24]. In different with the filter, the NGD circuit classification depends on the group delay (GD) diagram. The NGD function class can be easily understood with the frequency band where the GD is negative. For example, the class of low-pass (HP) NGD function was identified [25], [26]. However, because the magnitude behavior of HP-NGD circuit, some confusions maybe raised by electronics design engineers.

Some curious remarks maybe stated on the confusion between the HP-NGD function and high-pass (HP) filter. To clarify the difference between these two electronic functions in the present paper, we study the design of HP-NGD circuit.

D. NOVELTY OF THE PAPER

The main originality of the research work is focused on the miniaturization of the HP-NGD circuit based on the resistive-inductive (RL) passive network. In the best of the authors knowledge, despite the development of integrated circuit (IC) microelectronic design [27]–[31], no research work is available in the literature on the HP-NGD circuit. A lot of study was conducted on the CMOS design of electronic devices as frequency synthesizer [27], wireless transceiver [29], inductors and transformers [30] and active inductors [31]. The present paper develops, the first time, the design study of miniature HP-NGD IC in 130-nm CMOS technology.

E. OUTLINE OF THE PAPER

The present research work is organized in five main sections described as follows:

- Section II introduces the theory of unfamiliar HP-NGD circuit. The considered passive topology is based on RL-network. The theoretical study is based on the voltage transfer function (VTF) elaboration.
- The synthesis formulas allowing to determine the resistor and inductor components in function of the desired HP-NGD specifications are established in Section III.

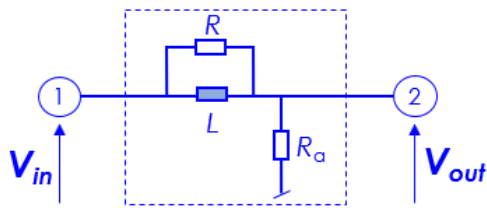


FIGURE 1. Scheme of the HP-NGD topology under study.

- Section IV develops the design method of the HP-NGD IC in 130-nm CMOS technology. The design methodology including the schematic and layout implementation in the CADENCE-VIRTUOUSO environment is described.
- Section V discusses the validation of the HP-NGD theory and the 130-nm CMOS design in the frequency domain. The feasibility study is based on the comparison of results from the theoretical model, schematic circuit simulation and post-layout simulation (PLS).
- Finally, the paper conclusion is drawn in Section VI.

II. THEORETICAL STUDY OF THE RL-NETWORK BASED HP-NGD PASSIVE TOPOLOGY

The present section introduces the HP-NGD passive circuit theory including the associated basic specifications. After the VTF consideration, the design and synthesis equations are developed in the following subsections.

A. TOPOLOGICAL DESCRIPTION

Fig. 1 depicts the topology of HP-NGD passive cell under study. The proposed topology is an L-shape passive cell. It is composed by a series resistor R_a associated to parallel RL-network constituted by resistor R and inductor L .

The initial step of the VTF calculation is based on the Laplace variable $s = j\omega$, in function of angular frequency ω and complex number $j^2 = -1$. Similar to all classical RL-network based electronic circuit, the HP-NGD analysis is elaborated by considering the input and output voltages $V_{in}(s)$ and $V_{out}(s)$, respectively. By definition, the VTF model is obtained by:

$$N(s) = \frac{V_{out}(s)}{V_{in}(s)}. \quad (1)$$

The associated transmittance is a complex number $N(j\omega)$ which can be expressed as:

$$N(j\omega) = \Re e [N(j\omega)] + j \Im m [N(j\omega)] \quad (2)$$

with the real part expressed by $\Re e [N(j\omega)]$ and the imaginary expressed by $\Im m [N(j\omega)]$. The associated magnitude is mathematically given by:

$$|N(j\omega)| = \sqrt{\Re e [N(j\omega)]^2 + \Im m [N(j\omega)]^2}. \quad (3)$$

The phase is defined by:

$$\varphi(\omega) = \arctan \left\{ \frac{\Im m [N(j\omega)]}{\Re e [N(j\omega)]} \right\}. \quad (4)$$

Then, the less familiar parameter for the HP-NGD analysis is the GD expressed as:

$$GD(\omega) = \frac{-\partial \varphi(\omega)}{\partial \omega}. \quad (5)$$

These basic parameters serve to develop the HP-NGD specifications.

B. IDEAL SPECIFICATIONS OF HP-NGD FUNCTION

The NGD analysis depends essentially on the responses of the frequency dependent GD expression defined by equation (5). The familiarization to the NGD analysis consists in the interpretation of sign of the GD in function of the frequency band.

1) EXISTENCE CONDITION OF HP-NGD FUNCTION

An electronic circuit can be assumed as a HP-NGD function if its VTF satisfies the following three conditions:

- **Condition 1:** The GD must be positive at very low-frequencies (VLFs) where the frequency is approximately equal to zero. The condition in function of GD at VLFs denoted GD_0 can be written as:

$$GD_0 = GD(\omega \approx 0) > 0. \quad (6)$$

- **Condition 2:** The GD must present a cut-off angular frequency denoted by $\omega_n = 2\pi f_n$. This frequency parameter is the roof of equation:

$$GD(\omega_n) = 0. \quad (7)$$

- **Condition 3:** The two previous condition implies that the GD at the higher frequency must be ideally always negative. Therefore, in the NGD frequency band indicated by Fig. 2(a), we must satisfy the following inequation:

$$GD(\omega \geq \omega_n) \leq 0. \quad (8)$$

The graphical illustration of these conditions is represented by the GD diagram depicted by Fig. 2(a). In addition to the GD response, the VTF magnitude response behave generally as shown in Fig. 2(b). This diagram ($N_{dB}(\omega) = 20 \log [N(\omega)] \leq 0$) is associated to typical passive topology as introduced by Fig. 1.

2) PARTICULAR CHARACTERISTIC FREQUENCIES OF HP-NGD FUNCTION

Similar to the typical LP-NGD one, the HP-NGD function is characterized by certain frequencies associated to particular values of the GD defined by equation (5).

In the following paragraph, we take the real positive variables N_0 and N_a , and angular frequency ω_a . The following three particular frequencies are considered to characterize an HP-NGD circuit:

- **VLFs ($\omega \approx 0$):** We can remark from the diagram of Fig. 2(b) that the magnitude at VLFs can be specified by:

$$N(\omega \approx 0) = N_0 \leq 1. \quad (9)$$

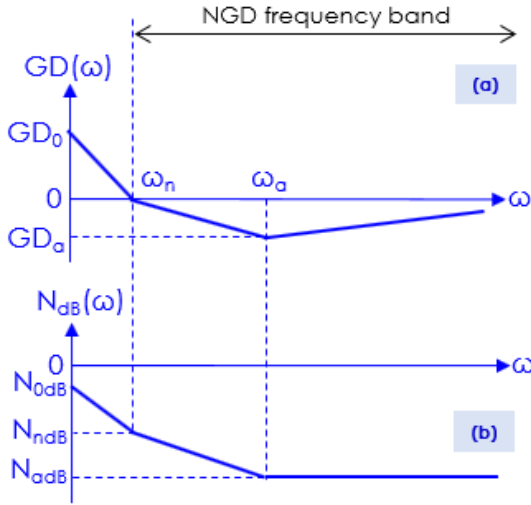


FIGURE 2. Typical (a) GD and (b) magnitude responses of HP-NGD function.

- **Cut-off frequency** ($\omega \approx \omega_n$): The magnitude can be defined by:

$$N(\omega \approx \omega_n) = N_n < N_0. \quad (10)$$

- **Optimal frequency** ($\omega \approx \omega_a$): This frequency is the root of equation:

$$\frac{\partial GD(\omega = \omega_a)}{\partial \omega} = 0. \quad (11)$$

At this optimal frequency, the GD reaches its minimal negative value:

$$GD(\omega_a) = \min [GD(\omega)] < 0. \quad (12)$$

Then, the optimal magnitude can be defined by:

$$N(\omega_a) = N_a < N_n. \quad (13)$$

The concrete application of these specifications to our RL-network based topology is elaborated in the following subsection.

C. FREQUENCY-DEPENDENT RESPONSES

The NGD analysis is based on the RL-circuit VTF model defined by equation (1). From where, we determine the transmittance:

$$N(j\omega) = \frac{R_a(R + j\omega L)}{R_a R + j\omega L(R + R_a)}. \quad (14)$$

As defined by equation (3), the associated magnitude is equal to:

$$N(\omega) = R_a \sqrt{\frac{R^2 + (\omega L)^2}{(R_a R)^2 + [\omega L(R_a + R)]^2}}. \quad (15)$$

Emphatically, the associated phase, which is defined by equation (4), is written as:

$$\varphi(\omega) = \arctan\left(\frac{\omega L}{R}\right) - \arctan\left[\frac{\omega L(R_a + R)}{R_a R}\right]. \quad (16)$$

Then, it yields the GD of the RL-network topology under study is given by:

$$GD(\omega) = \frac{R^2 L [R^2 R_a - L^2 \omega^2 (R + R_a)]}{(R^2 + L^2 \omega^2) [R^2 R_a^2 + L^2 \omega^2 (R + R_a)^2]}. \quad (17)$$

The exploration of each of these expressions lead to the synthesis method of the HP-NGD circuit in the following section.

III. HP-NGD NGD ANALYSIS AND SYNTHESIS EQUATIONS

The theoretical approach including the HP-NGD analysis and synthesis of the circuit topology under study is developed in the present section.

A. ANALYTICAL VERIFICATION OF HP-NGD EXISTENCE CONDITION

The three conditions cited in previous Subsection II-B can be explored in more details as follows:

- **Verification of Condition 1:** At VLFs, we can demonstrate that the GD established previously becomes:

$$GD(\omega \approx 0) = \frac{L}{R_a}. \quad (18)$$

We can remark that condition of inequation (6) is unconditionally verified for any values of R , R_a and L .

- **Verification of Condition 2:** By means of GD written in relation (17), the NGD cut-off frequency defined by equation (7) implies the equation:

$$R^2 R_a - L^2 \omega_n^2 (R + R_a) = 0 \quad (19)$$

The positive real solution of the previous polynomial equation is:

$$\omega_n = \frac{R}{L} \sqrt{\frac{R_a}{R + R_a}}. \quad (20)$$

We underline that the VTF magnitude at the cut-off frequency defined by equation (10) is equal to:

$$N_n = \sqrt{\frac{R_a}{R_a + R}}. \quad (21)$$

- **Verification of Condition 3:** Let us denote $a > 1$ a real positive defined by:

$$\omega_a = a \omega_n. \quad (22)$$

For the optimal frequency determined from equation (11), this coefficient is equal to:

$$a = \sqrt{1 + \frac{R + 2R_a}{\sqrt{R(R + R_a)}}}. \quad (23)$$

We can demonstrate that by means of GD expressed in relation (17), the optimal GD can be expressed as:

$$GD(\omega_a) = \frac{\left\{ \frac{\sqrt{R}(\sqrt{R} - \sqrt{R + R_a})}{[\sqrt{R(R + R_a)} + 2R + R_a]} \right\}}{\left[\frac{\omega_a(2R + R_a)(\sqrt{R} + \sqrt{R + R_a})}{\sqrt{R + R_a}} \right]}. \quad (24)$$

We remark that this GD, $GD_a = GD(\omega_a) < 0$, is always negative whatever the values of resistors, R and R_a , and inductor L . At the same frequency, the magnitude expressed in equation (15) becomes:

$$N(\omega_a) = \sqrt{\frac{R_a^3}{(R + R_a)^3}}. \quad (25)$$

We can analytically demonstrate that N_a and N_n are linked by the relation:

$$N_a = N_n^3 \quad (26)$$

which implies:

$$N_n = N_a^{1/3}. \quad (27)$$

In inference, the RL-network topology is theoretically classified as an HP-NGD topology.

B. INPUT AND OUTPUT IMPEDANCE ANALYTICAL EXPRESSIONS

The access impedances can play a significant role on the performance of electronic circuit matching in function of the surrounding interface components. The present section investigates analytically on the access impedance of our HP-NGD cell.

The input impedance of the circuit introduced by Fig. 1 can be expressed as:

$$Z_{in}(j\omega) = R_a + \frac{j\omega RL}{R + j\omega L}. \quad (28)$$

From this expression, we can underline that:

- At VLFs which corresponds to $\omega \approx 0$:

$$Z_{in}^{LF} = R_a \quad (29)$$

- At very high frequencies (VHF) which corresponds to $\omega \approx \infty$:

$$Z_{in}^{HF} = R_a + R. \quad (30)$$

It is worth to remind also that the output impedance is equal to:

$$Z_{out}(j\omega) = R_a. \quad (31)$$

We emphasize that the output impedance is independent to the frequency. Moreover, at low frequencies, we have the relation $Z_{in}^{LF} = Z_{out}$ and at high frequencies $Z_{in}^{HF} = Z_{out} + R$.

C. HP-NGD SPECIFICATION OBJECTIVES

The HP-NGD circuit parameters can be established in function of:

- The targeted value of NGD cut-off frequency f_n ,
- The optimal frequency f_a ,
- The GD optimal value $GD_a < 0$.
- And the voltage amplitude V_{\max} and maximal power P_0 which are linked by relation:

$$P_0 = \frac{V_{\max}^2}{\min [|Z_{in}(j\omega)|]}. \quad (32)$$

By taking into account the input impedance, this power can be reformulated by:

$$P_0 = \frac{V_{\max}^2}{R_a}. \quad (33)$$

In addition to the previous relation, the other resistor and inductor values can be determined from equation system:

$$\begin{cases} GD(\omega_a) = GD_a \\ N(\omega_a) = N_a. \end{cases} \quad (34)$$

The following subsection treats the synthesis equations of the HP-NGD topology. The synthesis formulas consisting in calculating the values of components R , R_a and L as components of the RL-network topology under study will be established in the next subsection.

D. ELABORATION OF THE HP-NGD SYNTHESIS EQUATIONS

The resistor R_a can be determined knowing the input voltage amplitude and IC maximal power by means of equation (28):

$$R_a = \frac{V_{\max}^2}{P_0}. \quad (35)$$

Emphatically, substituting the previous expression into the attenuation given by equation (21), we have the following resistor synthesis formula:

$$R = \frac{V_{\max}^2}{P_0} \left(\frac{1}{N_a^{2/3}} - 1 \right). \quad (36)$$

During the synthesis, the NGD optimal attenuation $N_a < 1$ is linked to the optimal frequency and GD by the relation:

$$N_a = \frac{(9\xi^{2/3} + 3\xi_1\xi^{1/3} - 3\xi_2 + \xi_1^2)^3}{729\xi^3} \quad (37)$$

with:

$$\begin{cases} \xi_1 = \frac{2\pi f_n GD_a - 1}{2\pi f_n GD_a} \\ \xi_2 = \frac{1 + 2\pi f_n GD_a}{2\pi f_n GD_a} \end{cases} \quad (38)$$

and:

$$\xi = \frac{\xi_1\xi_2}{6} - \frac{\xi_1^3}{27} - \frac{1}{2} + \sqrt{\frac{\left(\frac{\xi_1^3}{27} - \frac{\xi_1\xi_2}{6} + \frac{1}{2}\right)^2}{\left(\xi_2 - \frac{\xi_1^2}{3}\right)^3} + \frac{1}{81}}. \quad (39)$$

Moreover, by inverting the equation of the NGD cut-off frequency established in equation (20), we have the synthesis formula of the inductor:

$$L = \frac{R\sqrt{R_a}}{2\pi f_n \sqrt{R + R_a}}. \quad (40)$$

E. ANALYTICAL RELATIONS BETWEEN THE HP-NGD PARAMETERS

Knowing the previous formulas of resistors, we can demonstrate that the optimal and cut-off frequencies given by the coefficient expressed by equation (23) are linked by relationship:

$$a = \sqrt{N_n + 1 + \frac{1}{N_n}}. \quad (41)$$

Furthermore, the HP-NGD topology presents a property linked to the different parameters, N_a , GD_a , and ω_a . Substituting the formulas of resistors established by equation (35) and equation (36) into the GD expression proposed by equation (24), we have:

$$GD_a = \frac{N_n(N_n - 1)}{\omega_n(1 + N_n)(1 + N_n^2)}. \quad (42)$$

By using the coefficient of equation (36), the previous expression transforms as:

$$GD_a = \frac{N_a^{1/3}(N_a^{1/3} - 1)\sqrt{1 + N_a^{1/3} + N_a^{2/3}}}{\omega_a N_a^{1/6}(1 + N_a^{1/3})(1 + N_a^{2/3})}. \quad (43)$$

With these expressions, a HP-NGD IC in 130-nm CMOS technology can be designed with the following method.

IV. HP-NGD CMOS IC POC DESIGN METHOD AND PROCESS

The present section deals with the HP-NGD IC design methodology. The different steps to be fulfilled allowing to design the HP-NGD chips are described. The HP-NGD POC is aimed to be designed in 130-nm CMOS technology.

A. DESIGN METHODOLOGY

Similar to classical CMOS ICs of classical electronic functions (filter, amplifier, oscillator and many other devices) [27]–[31], the HP-NGD function design must start from the circuit specifications to the final layout design. In more clear view, the methodology of HP-NGD ICs can be illustrated by the design flow summarized by the successive steps of Fig. 3. This HP-NGD CMOS IC design flow can be described as follows.

In Step 1, the design process must begin with the choice of the HP-NGD cut-off frequency and NGD optimal value which will imply the optimal attenuation. The designer can refer to the specifications of Figs. 2.

In Step 2, knowing the HP-NGD specifications, the constituting resistor and inductor values can be calculated in the present step. The ideal component values can be calculated via formulas (35), (36) and (40).

In Step 3, the range of the calculated component value must be verified in the library of the simulation software (for the present study, Cadence-VURTUOSO). Then, the feasibility of the HP-NGD can be verified by the comparison between the calculated results from the VTF model given in equation (14) and the schematic simulation.

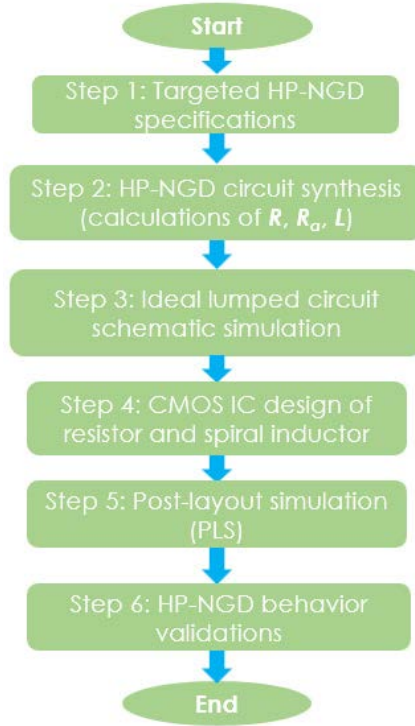


FIGURE 3. Design flow of HP-NGD CMOS IC.

In Step 4, after schematic ideal simulation, the layout can be drawn according to the schematic. The IC is implemented with respect to the design rule check (DRC) with high Ohmic unsalicyded $N +$ poly resistor and symmetrical high current spiral inductor. The DRC is a program that uses layout database to check every design rule involved in layout. After the preliminary drawing of the layout, the DRC is needed to ensure the ideal schematic and layout IC consistency. For example, the width and spacing of each wire constituting the layout must be correctly implemented and should not violate the specified minimum value. The DRC ensures that the design can be manufactured within the limits of production process. The layout versus schematic (LVS) step then makes it possible to compare the diagram of a circuit with its layout in order to check whether they are comparable, and list any differences between them.

In Step 5, this step consists of analyzing the content of the HP-NGD circuit layout in order to extract the active elements (transistors, diodes) but also the parasitic capacitances and resistors. An extracted view is thus obtained, permitting to simulate the circuit while considering the parasitic components.

In Step 6, the results of the PLSs are compared with the specifications of the HP-NGD circuit. Any modifications are then made, in particular at the layout level, to improve the results.

Following the previous design flow, HP-NGD IC POC result is investigated in the following subsection.

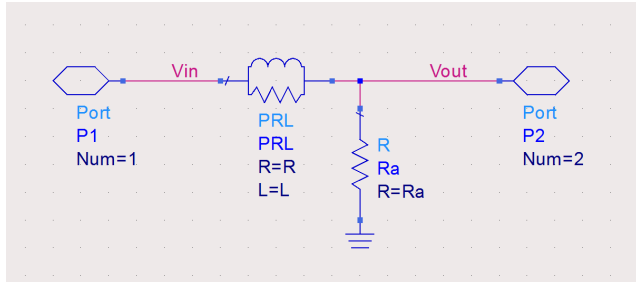


FIGURE 4. ADS schematic of HP-NGD circuit.

B. DESCRIPTION OF THE SCHEMATIC DESIGN OF HP-NGD LUMPED CIRCUIT

The first stage of the pre-simulation was carried by the lumped HP-NGD POC design from two different software standard tools for electronic and microwave circuits. The present study is performed in the frequency band from 1 MHz to 1 GHz.

The design of the passive circuit POCs were performed in the schematic environment of:

- **The ADS software from Keysight Technologies:** The ADS schematic of the designed RL-network based HP-NGD POC is presented in Fig. 4. Two circuits with different parameters were considered.

The main parameters of the RL lumped elements constituting the circuit are R , R_a and L . The schematic circuit design includes the AC voltage source. The input and output accesses are represented by Port₁ and Port₂, respectively.

- **And the CADENCE -VIRTUOSO software:** The corresponding chip design was designed by taking into account the 130-nm BiCMOS parameters. The schematic displayed in Fig. 5 represent the two different ICs of the HP-NGD POCs.

The HP-NGD IC schematic parameters were calculated from synthesis formulas (35), (36) and (40) with respect to the desired specifications. The chosen circuit parameters are indicated by Table 1. From the chosen lumped components, we can design the corresponding layout. The CMOS components are designed following the library of 130-nm technology CADENCE-VURTUOSO.

The following subsection describes the DRC based on the HP-NGD IC layout designs.

C. DESCRIPTION OF THE LAYOUT DESIGN

The STMicroelectronics BiCMOS-130 nm manufacturing process was chosen for this study because of its component integration potential in the range of HP-NGD desired specification values.

Due to the relatively large size of the components, expensive manufacturing processes such as 28 nm-FDSOI are not needed. Figs. 6 display the two layouts of the designed CMOS IC chipsets.

Each layout is designed with $225 \mu\text{m} \times 215 \mu\text{m}$ size. The circuit is expected to operate with $V_{max} = 5 \text{ V}$. The

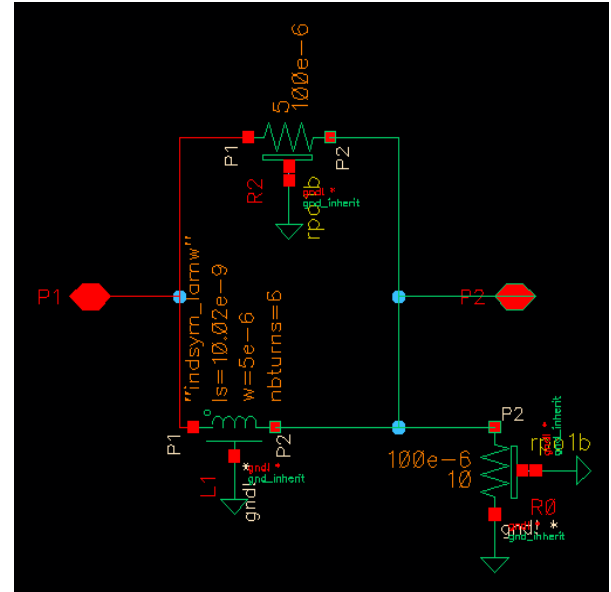


FIGURE 5. Schematic of HP-NGD circuit POCs representing chip₁ and chip₂ designed in VIRTUOSO environment.

TABLE 1. Proposed specifications and calculated parameters of the HP-NGD POCs.

Circuit	Parameter	Name	Chosen value
Chip ₁	Cut-off frequency	f_n	140 MHz
	NGD optimal value	GD_a	-30 ps
	Optimal attenuation	N_a	-1.4 dB
	Resistor	R	5 Ω
		R_a	20 Ω
		Inductor	L
Chip ₂	Cut-off frequency	f_n	204 MHz
	NGD optimal value	GD_a	-48 ps
	Optimal attenuation	N_a	-3.3 dB
	Resistor	R	10 Ω
		R_a	15 Ω
		Inductor	L

resistors and inductor were expected to be implemented under the manufacturing process minimum square area. The SISO circuit whole layout area is occupied by the two resistors in left and the large spiral inductor. The $100 \mu\text{m} \times 4.9 \mu\text{m}$ size resistors are implemented in 100-nm thickness poly-Si on 4.5-relative permittivity dielectric insulator. Each resistor is guard-ring surrounded in order to ensure their polarization and the ground plane connection through the dielectric substrate. The inductor is implemented in Al-metal spiral octagon with 0.0145 mm^2 surface over $1 \mu\text{m}$ thickness. All the layout component interconnections are Cu-based interconnect metallization with $0.1 \mu\text{m}$ thickness.

The range of the geometrical parameters (width, length, number of turns, diameter, Silicium area) of the considered

TABLE 2. Ranges of geometrical parameters of the used designed 130-nm CMOS resistors.

Description	Type of resistor design	Width, w		Length, d		Resistor value	
		w_{min}	w_{max}	d_{min}	d_{max}	R_{min}	R_{max}
Parameter	Unsalicided N+active resistor						
Value	rpo1b	1 μm	100 μm	3 μm	100 μm	4 Ω	13 k Ω

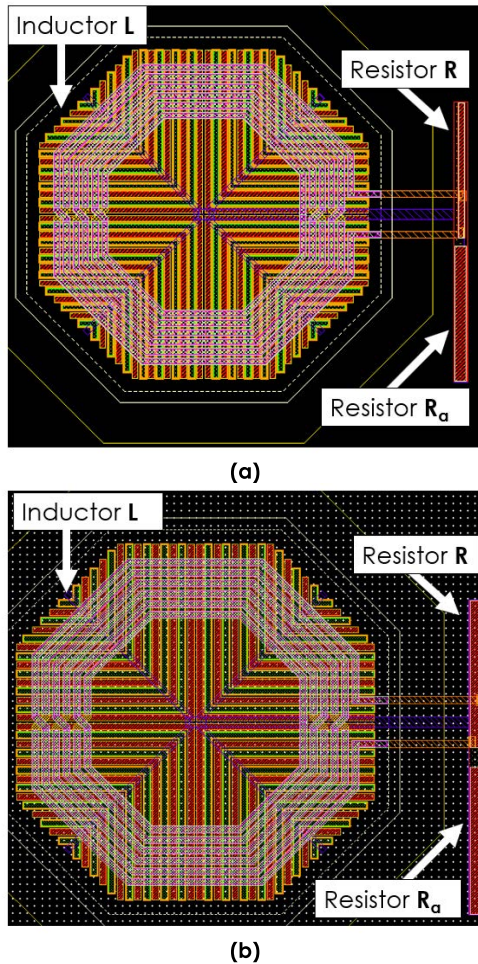


FIGURE 6. (a) Chip₁ and (b) chip₂ Cadence-VIRTUOSO layout (DRC check steps and results. $225 \mu\text{m} \times 215 \mu\text{m} = 0.04837 \text{mm}^2$) of HP-NGD circuit chipsets.

resistor and inductor layouts in function of the constituting materials are addressed in Table 2 and Table 3, respectively. The minimal resonance frequency is also indicated.

The feasibility study based on the HP-NGD function validation will be examined in the following subsection.

V. FEASIBILITY STUDY OF THE HP-NGD THEORY AND THE DEVELOPED CMOS IC POC DESIGN

To validate the HP-NGD function of the designed CMOS IC, frequency (AC) and transient Cadence-VIRTUOSO simulations were performed. The present section deals with the feasibility study of the HP-NGD 130-nm CMOS IC. Then, the calculated and Cadence simulated results are discussed. Comparisons between the calculated (“Calc.”), schematic (“Schem.”) and post-layout simulation (“PLS”)

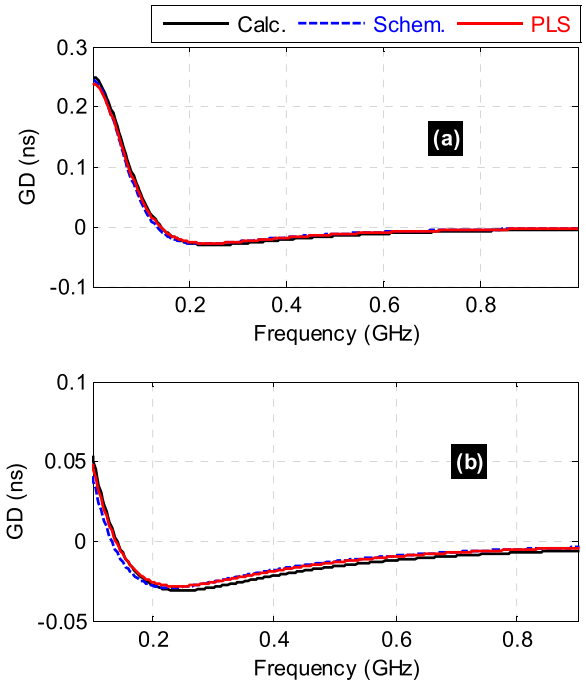


FIGURE 7. GD results of the HP-NGD circuit chip₁: (a) large and (b) narrow band plots.

simulated VTFs were carried out. The calculated results were generated from MATLAB program of VTF modeled by equation (1).

The following subsections discuss the obtained validation results.

A. HP-NGD VALIDATION OF CMOS CHIP₁

The results discussed in the present subsection correspond to VIRTUOSO AC schematic and PLS results from CMOS chip₁ shown in Fig. 5 and Fig. 6(a), respectively. Figs. 7, Figs. 8 and Figs. 9 reveal the GDs, magnitudes and phases of POC represented by CMOS chip₁, respectively. The plot of Fig. 7(a) presents the large frequency band representation. Then, narrower frequency band result of GD from 100 MHz to 900 MHz is introduced by Fig. 7(b) to highlight the HP-NGD characteristics as expected from diagram of Fig. 2(a). These plots highlight the HP-NGD function validity by means of the comparisons of the calculated, schematic-based and PLS results. Figs. 7 validate the HP-NGD behavior with a good correlation between the calculation, schematic simulation and PLS.

Table 4 addresses the associated HP-NGD parameters. The notable differences of the magnitudes displayed by Figs. 8 between the schematic and post-layout simulations are mainly due to via effect of the interconnect due to layout

TABLE 3. Ranges of geometrical parameters of the used designed inductor.

Description	Type of inductor	Width, w		Diameter, ϕ		Number of turns, N		Inductor value	
Parameter	Inductor symmetrical high current	w_{min}	w_{max}	ϕ_{min}	ϕ_{max}	N_{min}	N_{max}	L_{min}	L_{max}
Value	indsym_lamw	5 μm	12 μm	53 μm	163 μm	2	9	3.8 nH	25.8 nH

Description	Type of inductor	Si area, S		Resonance frequency	
Parameter	Inductor symmetrical high current	S_{min}	S_{max}	f_{min}	f_{max}
Value	indsym_lamw	0.0144 mm ²	0.0961 mm ²	3.33 GHz	91.4 GHz

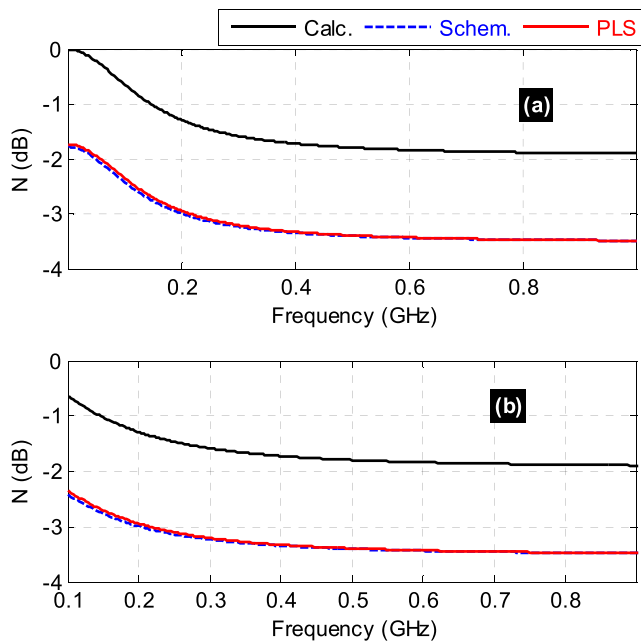


FIGURE 8. VTF magnitude results of the HP-NGD circuit chip₁: (a) large and (b) narrow band plots.

TABLE 4. Comparison of HP-NGD chip₁ characteristics.

Approach	f_a (MHz)	GD_a (ps)	N_a (dB)	f_n (MHz)	N_n (dB)
Calc.	246	-31	-1.4505	141	-0.96
Schem.	228	-29.1	-3.08	132	-2.65
PLS	237	-28.2	-3.065	138	-2.63

step which involves the creation of parasitic resistances and capacitors.

Because of the CMOS inductance parasitic and design imperfection, it can be found that the NGD optimal value and attenuation from CMOS IC present a difference of about $GD_a \approx -31$ ps and $N_a \approx -1.45$ dB at $f_a \approx 246$ MHz.

For more convenient illustration of the validation, the following subsection examines the AC responses of the other POC.

B. HP-NGD VALIDATION OF CMOS CHIP₂

Figs. 10, Figs. 11 and Figs. 12 present the frequency domain comparison results of GDs, magnitudes and phase results

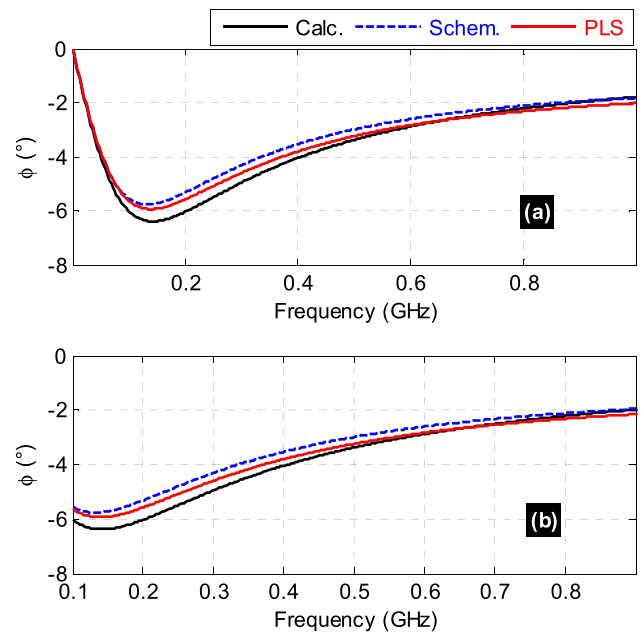


FIGURE 9. VTF phase results of the HP-NGD circuit chip₁: (a) large and (b) narrow band plots.

TABLE 5. Comparison of HP-NGD chip₂ characteristics.

Approach	f_a (MHz)	GD_a (ps)	N_a (dB)	f_n (MHz)	N_n (dB)
Calc.	357	-47.6	-3.3151	204	-2.2
Schem.	315	-44.6	-5.058	183	-4.14
PLS	324	-42	-4.916	189	-4.03

from chip₂. The designed schematic and layout are shown in Fig. 6(a) and Fig. 6(b). Once again, Figs. 10 confirm the HP-NGD behavior. In addition, a good correlation between the calculated model, and schematic simulation and PLS of GDs proposed by Figs. 10 and the associated phases of Figs. 12 is observed. in the frequency domain. Table 5 addresses the associated HP-NGD parameters. In this case of study, the calculated optimal GD and attenuation are of about $GD_a \approx -47$ ps and $N_a \approx -3.3$ dB at the frequency $f_a \approx 357$ MHz. It can be pointed out that the magnitude attenuation of Figs. 11 from CMOS IC presents a difference of about 1.7 dB.

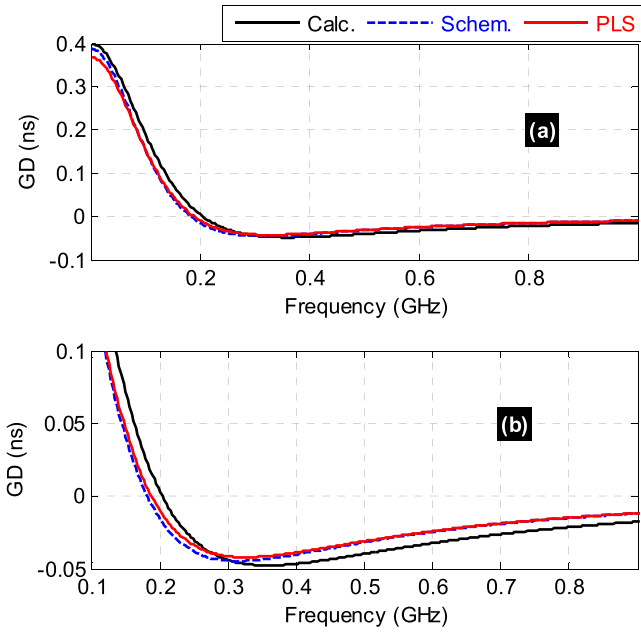


FIGURE 10. GD results of the HP-NGD circuit chip₂: (a) large and (b) narrow band plots.

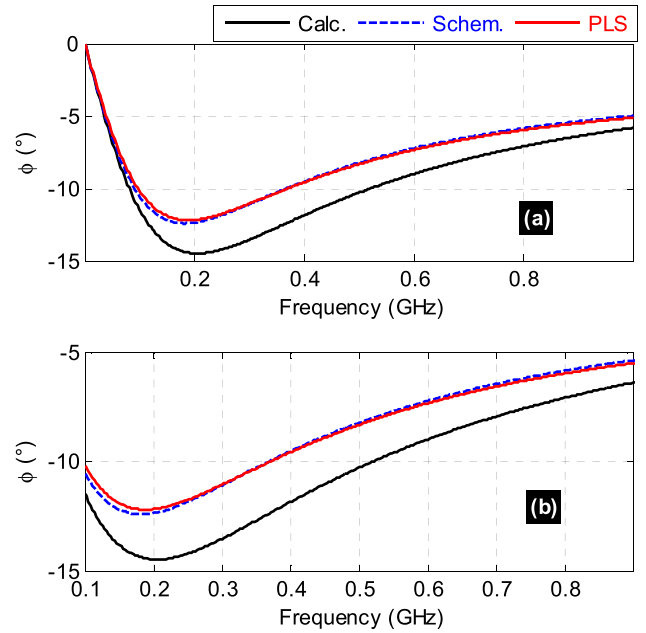


FIGURE 12. VTF phase results of the HP-NGD circuit chip₂: (a) large and (b) narrow band plots.

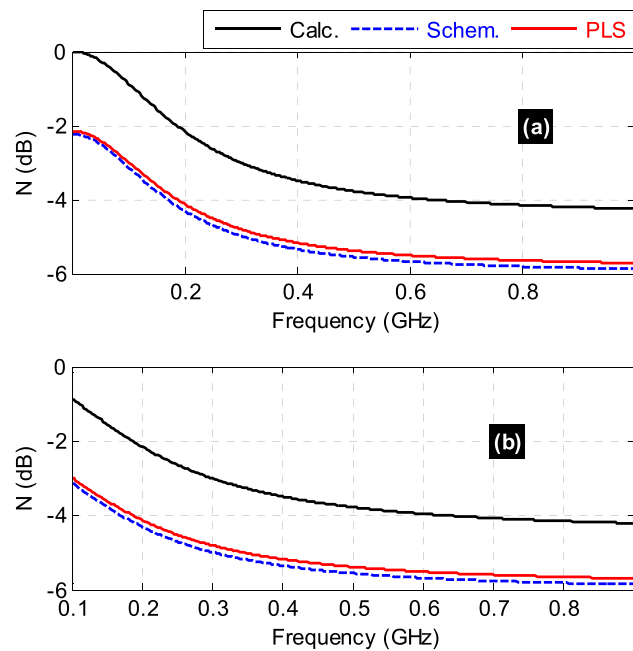


FIGURE 11. VTF magnitude results of the HP-NGD circuit chip₂: (a) large and (b) narrow band plots.

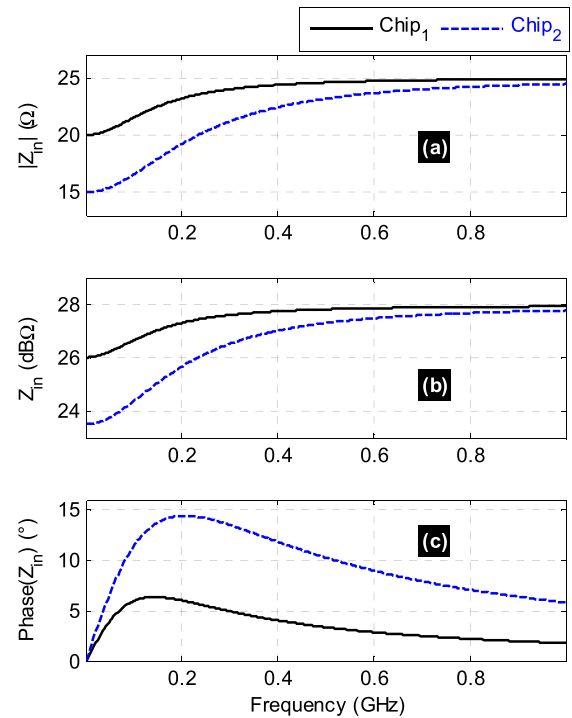


FIGURE 13. Magnitude in (a) linear, (b) in dB and (c) phase of input impedances of HP-NGD POC chip₁ and chip₂.

The observed difference corresponds to around 18% relative error. The differences between the calculation, schematic simulation and PLS are mainly due to the interconnect. The resistor CMOS design induces an undesired losses and imperfection. Hence, the inductor CMOS design is susceptible to operate with undesired resonance and parasitic effects. To reduce these parasites to a minimum, the layout is re-worked in order to use large metal lines as well as a large number of vias in parallel.

C. ACCESS IMPEDANCES ANALYSIS

By curiosity, one may curiously wonder about the input and output matching of the HP-NGD CMOS circuit under investigation. To address such a curiosity, the present subsection is dealing with the analysis of the input impedance Z_{in} expressed in equation (28). We remind that the output

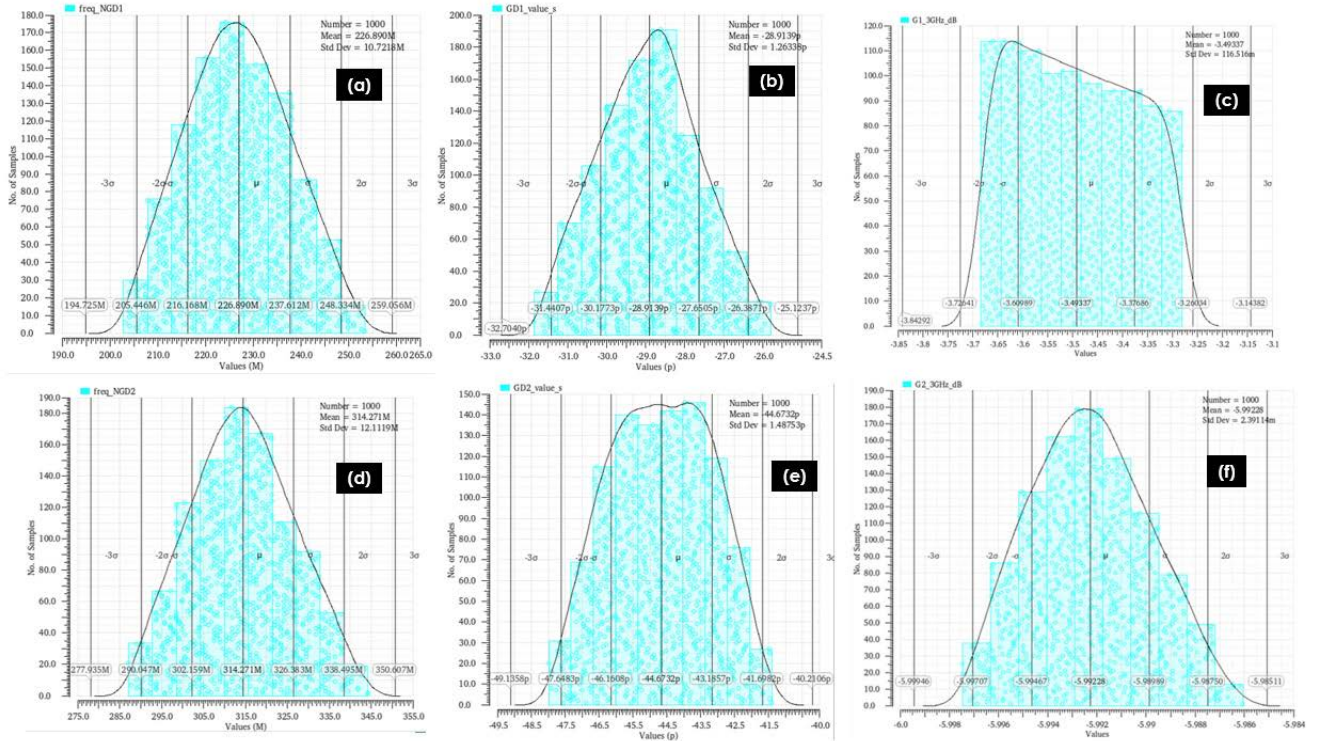


FIGURE 14. Histograms of schematic MC SA: (a) NGD cut-off frequency, (b) GD, and (c) attenuation from chip₁, and (d) NGD cut-off frequency, (e) GD, and (f) attenuation from chip₂.

impedance shown in equation (31) is equal to $R_a = 20 \Omega$ and $R_a = 15 \Omega$ for chip₁ and chip₂ POCs, respectively. The frequency dependent plots of the input impedance magnitudes and phase of the two POC circuits analyzed in the previous subsection are displayed in Figs. 13.

As pointed out in Subsection III-B, the input impedance is approximately equal to $R_a = 20 \Omega$ for chip₁ and $R_a = 15 \Omega$ for chip₂ at VLFs. Then, the input impedance is equal to $R + R_a = 25 \Omega$ for both chip₁ and chip₂ at very high frequencies. We can underline that the proposed HP-NGD topology presents a flexibility to be designed with respect to the other component impedances by adjusting for example R and R_a . Of course, the design formulas established in equation (35), equation (36) and equation (40) should integrate the compromise.

For more convenient illustration of the validation, the following subsection examines the sensitivity analyses with respect to the geometrical parameters of the resistor and inductor layouts.

D. MONTE CARLO (MC) SENSITIVITY ANALYSES (SAs)

The present SAs were performed by considering the geometrical parameter $\pm 5\%$ variations of the implemented resistor and inductor by means of schematic and PLSs. For the last case, the resistor and inductor parameters are indicated by Table 2 and Table 3, respectively.

The following paragraphs present the obtained results following the MC analyses via distribution statistical probability (DSP).

TABLE 6. Mean and standard deviations from $N_1 = 1000$ trial SAs.

HP NGD characteristics	Statistical parameter	Chip ₁	Chip ₂
N_a	Mean	-3.493 dB	-5.99 dB
	Standard deviation	0.116 dB	0.0024 dB
f_n	Mean	226.9 MHz	314.3 MHz
	Standard deviation	10.72 MHz	12.11 MHz
GD_a	Mean	-28.91 ps	-44.67 ps
	Standard deviation	1.26 ps	1.49 ps

1) SCHEMATIC MC SA WITH $N_1 = 1000$ TRIALS

In this first case of study, the SAs were based on the CADENCE-VIRTUOSO simulations by considering $\pm 5\%$ variations of the HP-NGD POCs initial parameters (through standard deviations). The present paragraph reports the MC SAs of HP-NGD POC with $N_1 = 1000$ trials. The obtained data was considered for the statistical analyses of the samples in the intervals delimited by the one, two and three times multiple of standard deviation. The statistical analyses from the computed results lead to the flat typical Gaussian variations with assessed values addressed by Table 6.

Fig. 14(a), Fig. 14(b), and Fig. 14(c) present the histograms and DSPs of the NGD cut-off frequency, GD optimal value and magnitude attenuations from chip₁ POC schematic, respectively. Then, Fig. 14(d), Fig. 14(e), and Fig. 14(f) illustrate those of from the schematic of the other POC represented by chip₂, respectively.

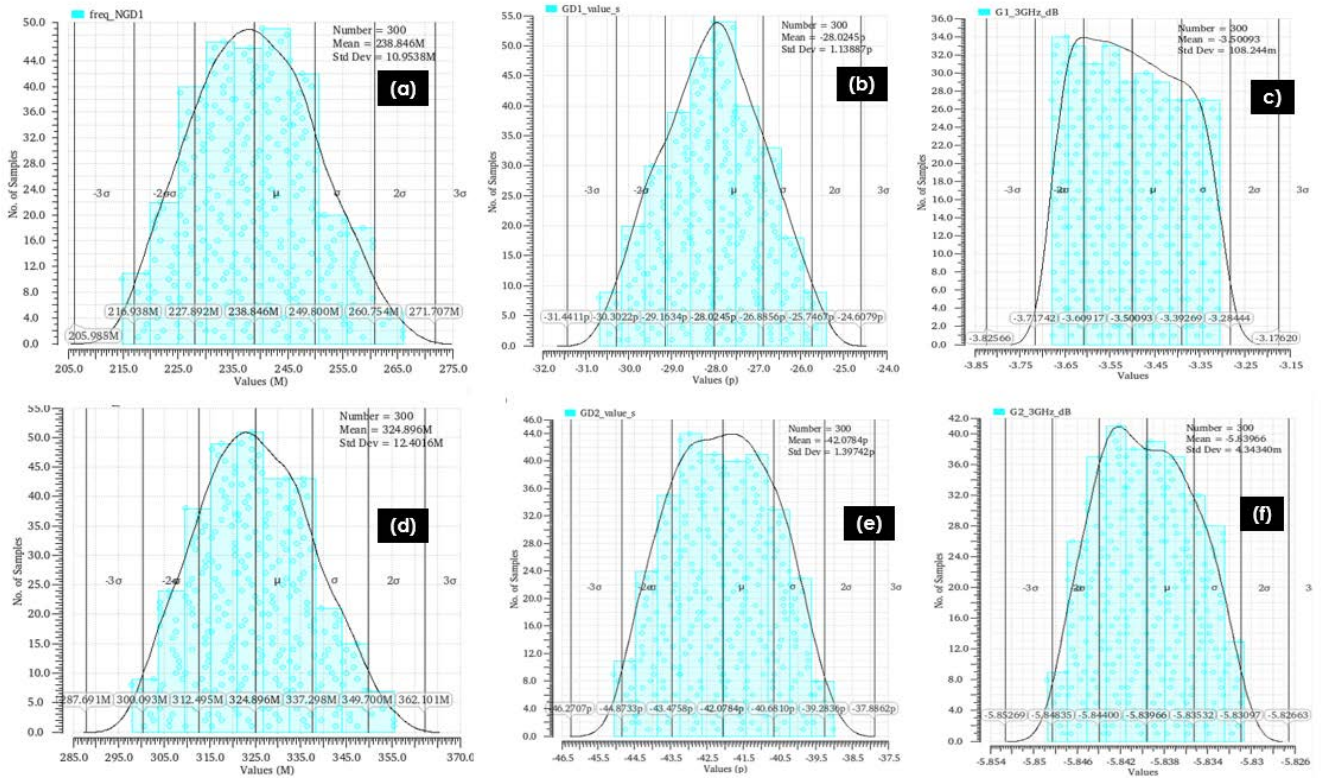


FIGURE 15. Histograms of layout MC SA: (a) NGD cut-off frequency, (b) GD, and (c) attenuation from chip₁, and (d) NGD cut-off frequency, (e) GD, and (f) attenuation from chip₂.

TABLE 7. Mean and standard deviations from N₂ = 300 trial SAs.

HP NGD characteristics	Statistical parameter	Chip ₁	Chip ₂
N _a	Mean	-3.501 dB	-5.84 dB
	Standard deviation	0.108 dB	0.004 dB
f _n	Mean	238.8 MHz	324.9 MHz
	Standard deviation	10.95 MHz	12.40 MHz
GD _a	Mean	-28.02 ps	-42.08 ps
	Standard deviation	1.14 ps	1.40 ps

The following paragraph examines the results of the post-layout analyses.

2) POST-LAYOUT MC SA WITH N₂ = 300 TRIALS

The SAs were carried out based on the CADENCE-VIRTUOSO simulations of the HP-NGD POCs by considering +/-5% variations of each geometrical parameter from the initial POC characteristics (through standard deviations). In this case, the simulations were performed on an extracted view of the circuit. This model view considers all the parasitic resistors and capacitances created during the layout-design step. The MC analyses of the post-layout MC SAs of HP-NGD POC were run with N₂ = 300 trials.

Fig. 15(a), Fig. 15(b), and Fig. 15(c) present the histograms of the NGD cut-off frequencies, GD optimal values and

magnitude attenuations based on the statistical analyses of the samples from POC chip₁, respectively. The histograms of those from chip₂ are displayed by Fig. 15(d), Fig. 15(e), and Fig. 15(f) illustrate the variations and, respectively. The statistical analyses from the computed results lead to the flat typical Gaussian variations with assessed values addressed by Table 7.

The results obtained on the post-layout circuit are very close (about 5% difference) to those observed on the schematic version. This concordance of results is made possible by the layout optimization work in order to reduce parasitic resistance.

VI. CONCLUSION

An original investigation on the HP-NGD miniature circuit is developed. The analytical theory enabling to determine the resistive and inductive parameters in function of the desired HP-NGD specifications is established.

An innovative design method of HP-NGD IC in 130-nm CMOS technology based on the Cadence-VIRTUOSO commercial tool is presented. After the synthesis equation formulation, the HP-NGD CMOS chip design methodology is described in function of the technological requirement. The different design steps including the DRC and LVS consideration are described.

To validate the theory, two POC of RL-network are designed and simulated. The design feasibility of each components and the overall chip is introduced. Then, the

validity of the HP-NGD behavior is validated by the comparison between the calculations, schematic simulation and PLS. The obtained results showing the NGD cut-off frequencies and the NGD optimal values are in good agreement.

From the present study, we underline the main challenges to conquer during the design phase of CMOS HP-NGD circuit. The choice of the HP-NGD specifications in function of the considered CMOS technology. The validity of the component values from the synthesis equation results in function the choses HP-NGD specifications and also the considered CMOS technology. The consideration of physical limitations of the metal and dielectric constituting the IC component available in the computer aided-design library. The geometrical parameter limitations of the resistor width and length in 130-nm CMOS technology as indicated in Table 2. And the geometrical parameter limitations of the inductor width, diameter of the loop and number of turns in 130-nm CMOS technology as indicated in Table 3.

The manufacturing process and test is scheduled as the next step of the present study.

In addition, the feasibility study will open the NGD circuit applications in many electronic systems. For example, a technique of electronic system unwanted effects can be avoided with NGD equalization [7], [8], [32], [33] and the design of improved UWB system with reduced delay [34].

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