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# Transient Stability Assessment and Enhancement of Grid-Forming Converters Embedding Current Reference Saturation as Current Limiting Strategy

Ebrahim Rokrok, *Student Member, IEEE*, Taoufik Qoria, Antoine Bruyere, *Member, IEEE*,  
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**Abstract**—This paper deals with the transient stability of a grid-forming converter while embedding a current reference saturation strategy. The novelty of this work consists in investigating the impact of the current reference angle on the transient stability. In case of a balanced voltage sag, analytical formulas to estimate the critical clearing angle (CCA) and critical clearing time (CCT) while considering different values of the current reference angle are derived. It is demonstrated that this angle is constrained by the ability of the power converter to *switch back* to the voltage control mode. Based on that, its optimal value that enhances the transient stability and allows a switching from the saturated current control mode to the voltage control mode is calculated. Thereafter, the effectiveness of this optimal choice to guarantee the stability in case of a phase shift caused by a line reclosing event is verified. Time-domain simulations and experimental tests validate the correctness of the presented theoretical approaches.

**Index Terms**—Critical clearing time, current limitation, current saturation algorithm, grid-forming control, inertial effect, transient stability.

## I. INTRODUCTION

THE energy paradigms have experienced a significant change from fossil-based to clean renewables in the past few decades. The scenario of highly penetrated renewables is going to be further enhanced. Hence, more power electronic converters are integrated in electrical grids to connect renewable energy sources and to transmit this power with high-voltage direct current (HVDC) lines [1]. When the synchronous generators (SGs) are dominating the electrical grid, they can create a stable voltage and frequency that enable the power converters to be synchronized at the point of common coupling (PCC) through a phase-locked loop (PLL) and then to inject the power to the grid. These converters are known as “grid-following” converters. Increasing the grid-following converters will strongly affect the power system stability and security [2]–[4].

To tackle these challenges, the way to control power converters has to be changed from grid-following control to grid-forming control in which the converter behaves as a voltage source. Due to the voltage source behavior of a grid-forming converter, the overcurrent protection requires a specific attention [5]. Compared to synchronous generators that

can support up to seven times over their rated current, power converters can only cope with few percent of overcurrent (typically 20%) [6]. Therefore, the grid-forming converters have to be protected against extreme faults such as short circuit, heavy load connection, line-tripping/reclosing and voltage phase jump only based on the control, while being able to stay synchronized to the power system.

Many control strategies have been proposed for grid-forming converters in order to limit the current during large transients [7]–[9]. One strategy is to limit the current with a current saturation algorithm (CSA). In practice, this technique is implemented on the generated current reference of the converters by saturating the reference current during over current period [9], [10]. Another well-known current limiting strategy is based on a virtual impedance (VI) that emulates the effect of an impedance when the current exceeds its rated value [6], [11], [12]. This method has shown its effectiveness to limit the current transients in case of various events while keeping the voltage source nature of the power converter. In [13] a comparative study between the CSA and VI strategies in case of a three-phase short circuit is performed. It has been demonstrated that the CSA strategy has a better performance in limiting the current during the first milliseconds after the fault, while for the VI strategy, an overcurrent during the first 25 milliseconds has been observed.

Grid-forming converters have not only to cope with the current limitation, but also to remain stable and synchronized to the AC grid after large disturbances. In the power system, this ability is defined as the angle stability or the transient stability. This aspect has been studied in [14], [15] while neglecting the current limitation. However, as mentioned in [10], [13], the current limitation has a large impact on the transient stability. In [16], [17], the transient stability of the grid-forming converters including the VI in investigated. In [16], the transient stability of a droop-based virtual synchronous generator in case of a 30% grid voltage sag is studied in two steps. First, the VI is not taken into account. Based on that, a theoretical approach relying on the Lyapunov’s direct method to predict the critical clearing time (CCT) is developed. Then, when including a constant VI, it has been demonstrated that the stability region becomes more limited. In [17], a method for critical clearing angle (CCA) and CCT calculation in case of a bolted fault while

limiting the current with a VI is proposed. To improve the CCA and CCT, authors in [16], [17] propose to decrease the power reference with respect to the AC voltage magnitude. An alternative solution that consists to increase the inertia constant with respect to the AC voltage magnitude is suggested in [18]. Referring to [19], the management of the power reference or inertia constant with respect to the voltage magnitude is mainly effective when the voltage magnitude is decreasing as in case of a voltage sag. However, in the case of a voltage phase shift, which is a very likely event, these solutions are useless.

Considering the effect of a CSA on the transient stability, authors in [10], [20] has determined a stability criterion based on CCA for an inertia-less droop-controlled converter in case of a voltage sag. Then, in [10] a stability enhanced P-f droop control scheme is presented to improve the transient stability of the converter by modifying the frequency set point through the quadrature voltage axis. In [10] and [20], the priority has been given to the d-axis component of the current reference, so the converter injects the current aligned with the d-axis during the fault. To the best of our knowledge, the impact of the current reference (i.e., the current reference angle) during the fault has not been justified and its impact on the transient stability has not been highlighted. Based on that, this paper proposes the following main contributions:

- Investigation of the impact of the current reference angle on the transient stability by means of the analytical formulas of the CCA and CCT.
- Proposal of an optimal determination of the saturated current angle, which is based on a trade-off between the transient stability enhancement and the ability to switch-back to the voltage control mode after the fault clearance.

The effectiveness of the calculation of the saturated current angle has been demonstrated for two different types of balanced faults (i.e., three phase short-circuit fault and phase-shift).

The remaining of the paper is organized as follows. Section II introduces the studied system including the grid-forming control architecture and large signal models for transient stability analysis. In section III, the transient stability of the grid-forming converter in the case of a voltage is assessed and enhanced. Section IV demonstrates the effectiveness of the proposed method in increasing the stability margin of the system in case of a phase shift. The experimental validation of the proposed method is given in section V. Finally, section IV

concludes the paper.

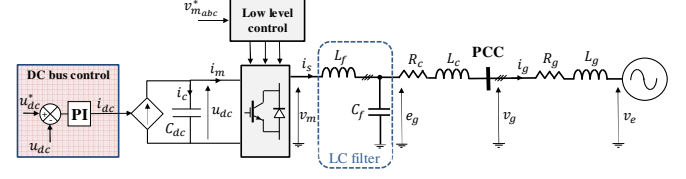


Fig. 1. Generic topology of the VSC.

## II. PRESENTATION OF THE STUDIED SYSTEM

The main aim of a voltage source converter (VSC) is to convert a DC power to AC power and vice-versa. In what follows, the VSC is considered as a controllable three-phase AC voltage source:  $v_{ma}, v_{mb}, v_{mc}$ , which are modulated from a constant DC bus voltage (see Fig. 1). The control system defines a set of three-phase reference signals  $v_{ma}^*, v_{mb}^*, v_{mc}^*$ , in such a way that the average values of  $v_{ma}, v_{mb}, v_{mc}$  during the switching time of the transistors are equal to  $v_{ma}^*, v_{mb}^*, v_{mc}^*$ . Following assumptions are considered:

- It is supposed that the VSC is connected to the grid with a transformer, which is modeled with its series impedance ( $L_c, R_c$ ).
- An LC filter ( $L_f, C_f$ ) is used to eliminate the high-frequency harmonics caused by the PWM signals.
- The grid is modeled by a Thevenin equivalent circuit composed of a voltage source  $v_{e_{abc}}$ , an inductance  $L_g$  and a resistance  $R_g$ .
- The converter is connected to a power transmission system, and therefore, the resistance is much smaller than the reactance ( $R_g \ll L_g$ ).
- A capacitor is placed on the DC bus in order to take into account a simplified model of the DC bus dynamics. The charging time of the DC capacitor is 80 [ms] and the response time of the DC voltage controller is 50 [ms] [21].

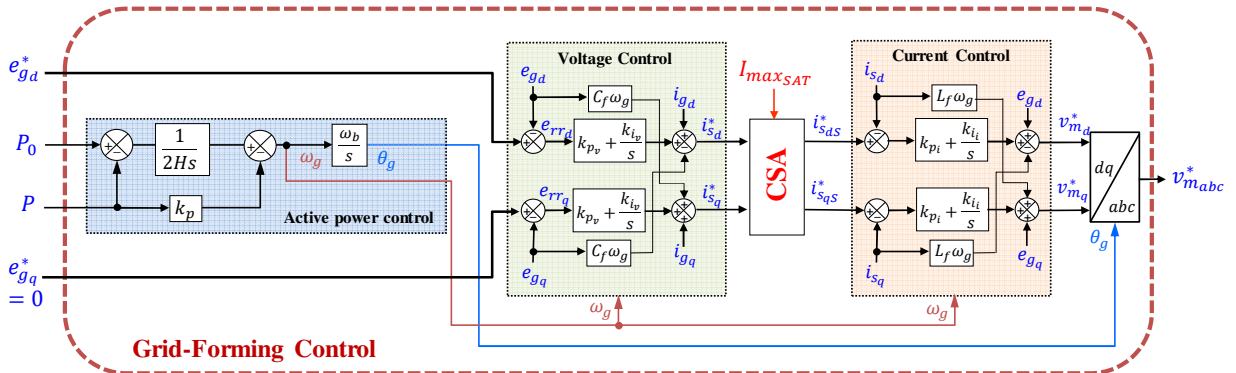
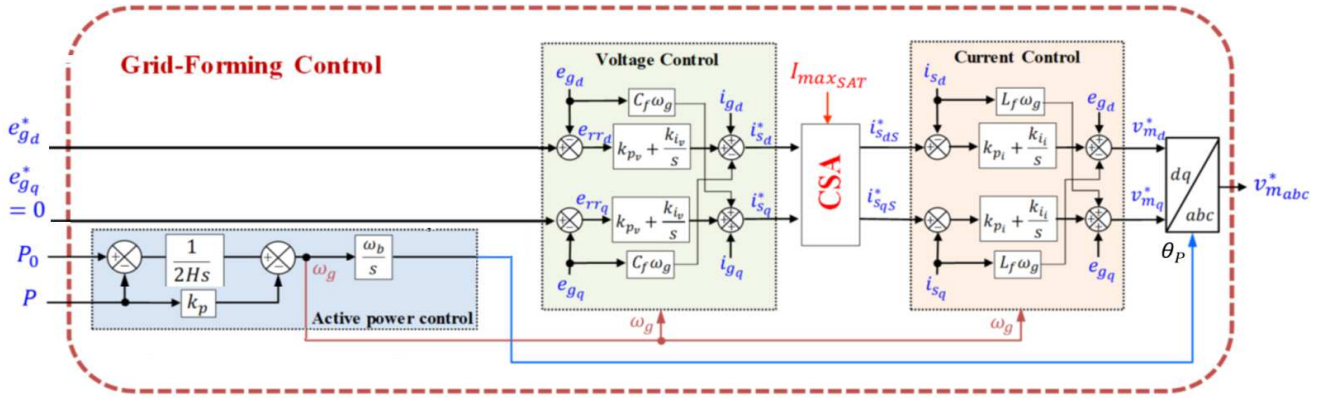


Fig. 2. Implemented VSC control system.



### A. Control Structure

The control structure of the grid-forming VSC is presented in Fig. 2. Inner control includes the cascaded voltage and current control loops, which allows the output voltage  $e_g$  to track its reference value  $e_g^*$ . The voltage  $e_g$  is aligned to the d-axis ( $e_{gq}^* = 0$  pu).

In this paper, the outer active power controller is based on a PLL-free IP-controller [18]:

$$\omega_g = \frac{1}{2Hs}(P_0 - P) - k_p P \quad (1)$$

$$\theta_g = \omega_g \omega_b / s \quad (2)$$

where  $H$ ,  $k_p$  and  $P_0$  denote the inertia constant, damping factor and active power setpoint, respectively.  $\theta_g$  denotes the time-domain internal angle and also the angle of the Park frame.

Generally, the dynamic of the outer power loop is over ten times slower than that of the inner control loops [22]. In fact, when analyzing the transient stability problem caused by the power control loop, the inner control loops can be neglected because of their faster response time [10], [14]. Hence, based on this assumption, large signal models for transient stability studies are derived.

### B. Phasor Model for Transient Stability Studies

In order to analyze the large transient stability, a classical phasor model is proposed in Fig. 3 (a). Neglecting the internal loops dynamics, only the voltage  $e_g$  is considered in the converter side. In steady state, it is represented by a complex quantity  $\bar{E}_g$ . The magnitude is supposed to be 1 pu and the angle is  $\delta_g$ , which is equal to  $\theta_g$  in steady state:

$$\theta_g(t) = \omega_g t + \delta_g.$$

$\bar{V}_e$  represents the voltage vector at the grid side, the magnitude is 1 [pu] and the phase angle is  $\delta_e$ . By neglecting losses (and so the resistance  $R_c$ ), fig. 3 (b) illustrates the corresponding phasor diagram in the normal operation mode (unsaturated current operation mode). The vector  $\bar{E}_g$  (in blue) is the controlled vector that is supposed to be aligned with the d-axis. The current vector  $\bar{I}_g$  (in green) is a consequence of this operation mode. The well-known expression of the power can be written in steady state as follows:

$$P = \frac{E_g V_e}{X_c + X_g} \sin(\delta_g - \delta_e) = P_{max} \sin \delta, \quad (3)$$

where  $\delta = \delta_g - \delta_e$  denotes the power angle,  $P_{max} = E_g V_e / (X_c + X_g)$ .

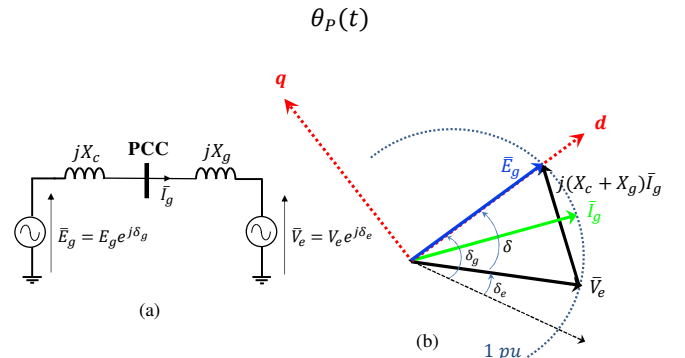


Fig. 3. (a) Equivalent circuit of VSC. (b) Phasor diagram.

During some transient times, the current may increase over the maximum current of the converter. To limit the current, a CSA is used and defined as follows [13], [18]:

$$\begin{cases} i_{sd}^* = i_{sd}^*, i_{sq}^* = i_{sq}^* & \text{if } \sqrt{i_{sd}^2 + i_{sq}^2} \leq I_{maxSAT} \\ i_{sd}^* = I_{maxSAT} \cos(-\phi) & \text{if } \sqrt{i_{sd}^2 + i_{sq}^2} > I_{maxSAT} \\ i_{sq}^* = I_{maxSAT} \sin(-\phi) & \end{cases} \quad (4)$$

$I_{maxSAT}$  stands for the maximum allowable current magnitude of the converter, which is typically 1.2 (p.u.).  $i_{sdq}^*$  denotes the saturated  $d$ - $q$  currents. By neglecting the current in the capacitor, it is possible to draw a new phasor diagram of the VSC in this saturated current operation mode (Fig. 4). The magnitude of  $\bar{I}_g$  is  $I_{maxSAT}$ , its angle  $\phi$  can be chosen freely by the control. It is referenced to the d-axis. As the voltage vector  $\bar{E}_g$  is neither controlled, it becomes a consequence in this operation mode. Hence, the active power is now calculated with the grid voltage  $\bar{V}_e$  and the controlled vector  $\bar{I}_g$  as follows [10], [20]:

$$P = P_{maxSAT} \cos(\delta - \phi) \quad (5)$$

where  $P_{maxSAT} = V_e I_{maxSAT}$ .

According to (3) and (5), the large signal model of the grid-forming converter for both unsaturated and saturated current operation modes is illustrated in Fig. 5.

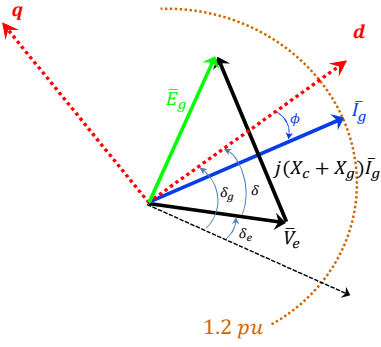


Fig. 4. Phasor-diagram of the VSC in saturated current operation mode.

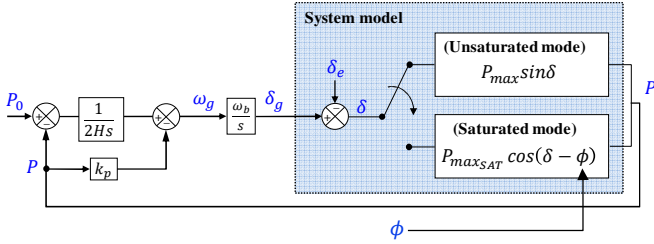
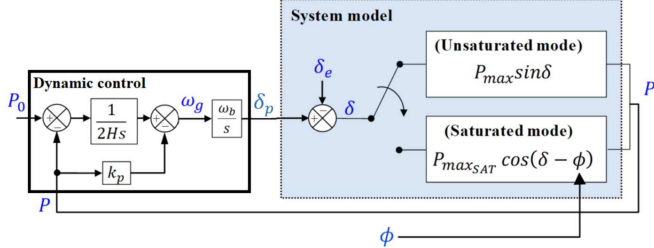


Fig. 5. Large signal model including the dynamic control for transient analysis.



In the literature, the angle  $\phi$  has been set to  $\phi = 0$  rad [10], [17], [20]. However, this choice has not been justified and its impact on the stability has not been analyzed. In the following sections, the effect of this choice on the transient stability of the grid-forming converter under various events is investigated.

Le fonctionnement du système en dehors de l'équilibre peut être décrit en tenant compte du comportement dynamique des moyens

### III. TRANSIENT STABILITY ANALYSIS IN CASE OF A VOLTAGE SAG

In this section, first, a specific case considering a 100% voltage sag at the PCC is investigated. The aims of this study are to simply explain the operation mechanism of the VSC under this event, to derive the CCA and CCT formulas and to investigate the impact of an optimal calculation of the saturated current angle  $\phi$  on the transient stability. After that, a generic case of voltage sag is considered.

#### A. Analysis of the Operation under a 100% Voltage Sag

The quasi-static  $P - \delta$  characteristic of the grid-forming converter for both saturated and unsaturated current operation mode is used to study the large signal stability graphically and to propose an analytical formula to calculate the critical clearing time. Fig. 6 describes the operation mechanism of the grid-forming VSC subjected to a bolted fault. Initially the converter is operating in normal condition and the initial operating point

is  $(\delta_0, P_0)$ :

- Phase 1 (from 'a' to 'b'): The voltage drops to zero resulting in an increase of the current, which is limited by the CSA, and a decrease of the active power. According to the control described in Fig. 5, the angle  $\delta$  increases until  $\delta_c$ , which is defined as the clearing angle (moving from 'a' to 'b').
- Phase 2: The fault is cleared, the CSA is activated and the operating point jumps to the point (c) located on the saturated  $P - \delta$  curve.
- Phase 3: The active power is higher than its setpoint, however, the angle  $\delta$  is still increasing until the point (d) due to the inertial effect.
- Phase 4: Once the converter frequency becomes lower than the grid frequency, the angle starts to decrease until reaching the operating point (e), which is the intersection point of the saturated and unsaturated  $P - \delta$  curves.
- Phase 5: At the operating point (e), the CSA is deactivated and the system switches back to the voltage control mode. The angle decreased until the equilibrium point (a), where  $P = P_0$ .

For a given  $\delta_c$ , the system remains stable as long as the areas A1 and A2 are equal. The stability limit is reached when  $\delta_c = \delta_{cc}$ , which is called the "critical clearing angle (CCA)"  $\delta_{cc}$ . Under this condition, the internal angle reaches to its maximum value  $\delta_{maxSAT}$  after the fault clearance.

$$\delta_{maxSAT} = \arccos\left(\frac{P_0}{P_{maxSAT}}\right). \quad (6)$$

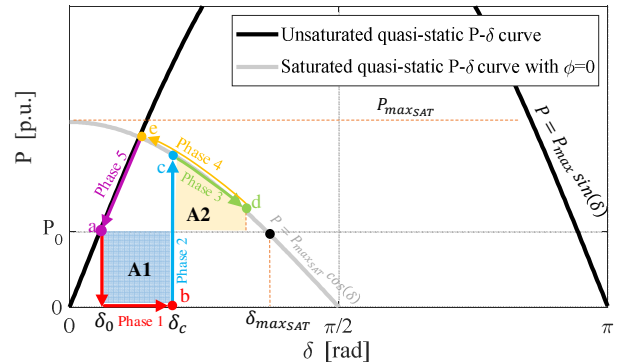


Fig. 6. Operation mechanism of the VSC under 100% voltage sag.

It should be mentioned that during the fault (Phase 1), where the converter is operating in saturated current mode, the voltage control loop generates a current reference higher than the maximum current ( $I_s^* > I_{maxSAT}$ ). However, in the post-fault (Phase 3 and Phase 4) apart from the fact that the converter works in saturated current mode, it is always trying to take the control back by generating a current reference lower than the maximum current ( $I_s^* \leq I_{maxSAT}$ ). In quasi-static point of view, when the operating point reaches to the point (e), the output voltage of the converter is 1 [pu]. Therefore, the voltage error is zero and the generated current reference  $I_s^*$  is exactly equal to  $I_{maxSAT}$ . Having in mind that the converter always tends to attract the operating power to its setpoint thanks to the power control loop after any disturbance, the system will naturally switch to the unsaturated current mode at the point (e) and the power is reduced in the unsaturated current mode to  $P_0$

TABLE I

SYSTEM AND CONTROL PARAMETERS

$P_b = S_b$	1000 MW	$U_{ac}$	320 kV
$L_g = 10R_g$	0.1 p.u.	$I_{maxSAT}$	1.2 p.u.
$L_c$	0.15 p.u.	$e_{gd}^*$	1 p.u.
$R_c$	0.005 p.u.	$e_{gq}^*$	0 p.u.
$C_f$	0.066 p.u.	$k_{pi}$	0.73 p.u.
$L_f$	0.15 p.u.	$k_{ii}$	1.19 p.u.
$R_f$	0.005 p.u.	$k_{pv}$	0.52 p.u.
$V_e$	1 p.u.	$k_{iv}$	1.16 p.u.
$\omega_b$	314.16 rad/s	$H$	5 s
$U_{ac}$	640 kV	$k_p$	0.007
$C_{dc}$	0.39 mF		

according to this quasi-static solution. In dynamic point of view, a mismatch on this deactivation point might be observed due to the voltage control loop dynamics. A proper anti-windup strategy can effectively mitigate the voltage control loop dynamics in order to enable the converter to smoothly switch back to the voltage control mode at the point (e).

### B. Critical Clearing Time Calculation

The critical clearing angle is calculated by considering equal surfaces  $A_1$  and  $A_2$ :

$$\int_{\delta_0}^{\delta_{cc}} P_0 d\delta = \int_{\delta_{cc}}^{\delta_{maxSAT}} (P_{maxSAT} \cos(\delta) - P_0) d\delta$$

$$\Rightarrow \delta_{cc} = \text{asin} \left( \frac{P_0(\delta_0 - \delta_{maxSAT})}{P_{maxSAT}} + \text{si} \, n(\delta_{maxSAT}) \right), \quad (7)$$

where  $\delta_0 = \text{asin}\left(\frac{P_0(X_c + X_g)}{E_g V_e}\right)$ . In order to calculate the critical clearing time (CCT)  $t_{cc}$ , the expression of the angle  $\delta$  during the phase I is needed. According to the control system (Fig. 5) and considering a fault condition ( $P=0$ ), it can be written:

$$\delta(t) = \frac{\omega_b P_0}{4H} t^2 + \delta_0 \quad (\delta_0 \leq \delta \leq \delta_{cc}) \quad (8)$$

Hence, the CCT can be expressed as:

$$t_{cc} = 2 \left( \sqrt{\frac{H(\delta_{cc} - \delta_0)}{\omega_b P_0}} \right) \quad (9)$$

Equation (9) clearly demonstrates the effect of the initial operating point and inertial effect on the CCT. Two large assumptions have been used to obtain the expression of the critical clearing time:

- 1- The effect of the damping is negligible.
- 2- The quasi-static model is valid enough even during large transient phenomena.

The validity of these assumptions is demonstrated in the following lines through dynamic simulations.

The system and control parameters are given in the Table I. Note that an anti-windup is applied to the PI regulators in the voltage control loop (see Appendix) [19]. Considering the given parameters in Table I, the CCT predicted from (9) and the one observed from the time-domain simulations are compared in Table II for different operating points. One can notice a small error between both CCTs. This error is due to the damping effect as it is mentioned in [23].

Taking  $P_0 = 1 \text{ pu}$  as an illustrative example, Fig 7 shows the simulation results with two different fault durations of  $t_{f1} = t_{cc} = 38 \text{ ms}$  and  $t_{f2} > t_{cc}$  (45 ms). As expected if the clearing time is lower or equal to the CCT, the internal angle of the VSC stably recovers its equilibrium point, otherwise it

diverges and the system loses the synchronism. The DC bus voltage is in the acceptable range when the AC system is stable. Note that in case of having a restriction on the energy provided by storage elements to the DC bus, the stability of the AC system is troubled. This subject is out of the scope of this paper. Interested readers can find more details about this issue in [8].

TABLE II  
RESULTS OF THE CCT DETERMINATION

$P_0$	$\phi = 0$	
	Predicted CCT by (9)	CCT in simulation
1 pu	41 ms	38 ms
0.9 pu	69 ms	63 ms
0.8 pu	99 ms	91 ms
0.7 pu	133 ms	120 ms
0.6 pu	173 ms	157 ms
0.5 pu	221 ms	204 ms

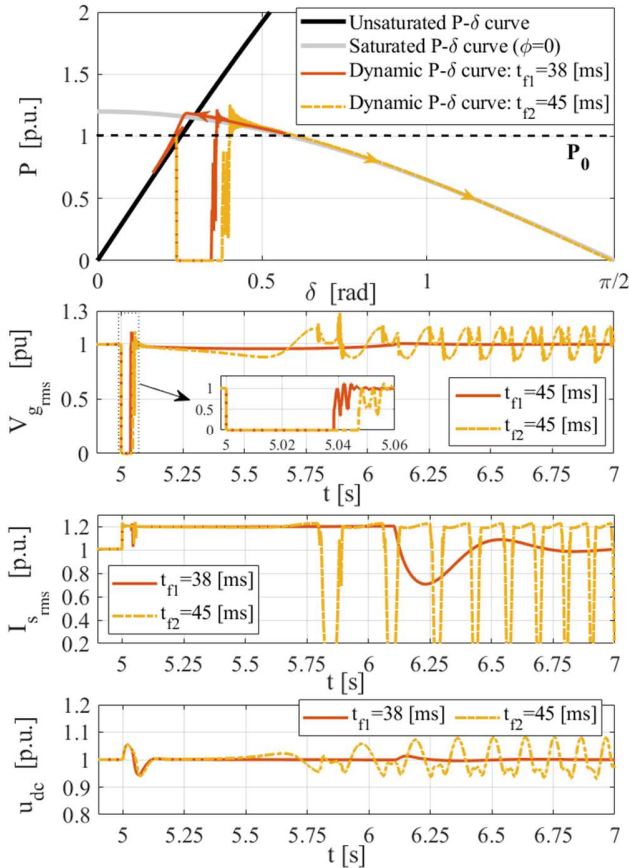


Fig. 7. Simulation results in case of a 100% voltage sag with different fault time durations.

In order to investigate the impact of the inertia constant on the accuracy of (9), another case study with  $H = 1.25$  [s] is examined. To have a fair comparison, the damping ratio  $\zeta$  of the active power response should be the same for different inertia constants. As it is demonstrated in [18], the damping ratio is proportional to  $k_p\sqrt{H}$ . Therefore, the controller gain  $k_p$  is set to 0.014 [pu]. Table III summarizes the obtained CCT for various operating points. It can be seen that the accuracy of the predicted CCT is slightly reduced compared to the case with  $H = 5$  [s] (in Table II). In fact, when the inertial effect is negligible, the angle  $\delta$  right after the phase 2, shown in Fig. 6, tends to be decreased immediately. This makes the critical clearing angle  $\delta_{cc}$  closed to the maximum allowable angle  $\delta_{maxSAT}$  and therefore, a different formula for the CCT can be derived without using the equal area criterion as it has been already studied in [13].

TABLE III  
RESULTS OF THE CCT DETERMINATION FOR A SMALL INERTIA CONSTANT

$\phi = 0$ $H = 1.25$ s, $k_p = 0.014$		
$P_0$	Predicted CCT by (9)	CCT in simulation
1 pu	20 ms	17 ms
0.9 pu	34 ms	28 ms
0.8 pu	50 ms	44 ms
0.7 pu	67 ms	58 ms
0.6 pu	86 ms	78 ms
0.5 pu	110 ms	98 ms

In any case, the obtained value of the critical clearing time is quite small. Next section proposes to set the current reference angle in order to increase this critical clearing time.

### C. Impact of the Saturated Current Angle $\phi$ on Transient Stability

From (9), two control parameters, namely the power set point ( $P_0$ ) and inertia constant ( $H$ ), affect the transient stability of the VSC. As pointed out in [16] the transient stability of grid-forming converters can be enhanced by reducing the active power reference during grid voltage sags. References [17], [18] have demonstrated that increasing the inertia constant in case of a voltage sag also improves the transient stability. The angle  $\phi$  is a new control degree of freedom that has not been exploited in the literature to enhance the transient stability of the grid-forming VSCs.

As explained in (5), the angle  $\phi$  has an influence on the expression of the active power. When applying a positive angle, the quasi-static  $P - \delta$  curve in the saturated current operation mode is shifted to the right side (see Fig. 8). In this condition, the maximum angle that converter can reach is given by:

$$\delta_{maxSAT}^{\phi} = \arccos\left(\frac{P_0}{P_{maxSAT}}\right) + \phi. \quad (10)$$

Using the equivalent area criteria (EAC) and in this condition, the following expression for the CCA and CCT are obtained:

$$\delta_{cc}^{\phi} = \arcsin\left(\frac{P_0(\delta_0 - \delta_{maxSAT}^{\phi})}{P_{maxSAT}} + \sin(\delta_{maxSAT}^{\phi} - \phi)\right) + \phi \quad (11)$$

$$t_{cc}^{\phi} = 2 \left( \sqrt{\frac{H(\delta_{cc}^{\phi} - \delta_0)}{\omega_b P_0}} \right) \quad (12)$$

Comparing to (7) and (9), (11) and (12) demonstrate that the CCA and CCT are increased with respect to the increase of  $\phi$ ; giving more time for clearing the fault while ensuring a stable restoration. However, the parameter  $\phi$  could not be incautiously chosen. Referring to Fig. 8 and focusing on the “Phase 4”, where the operating point moves from (d) to (e), in this particular situation the internal angle is locked at the operating point (e) located in the saturated  $P - \delta$  curve since  $P$  reaches  $P_0$ . In other words, the system cannot switch back to the voltage control mode. Therefore, the choice of  $\phi$  is constrained by the ability of the VSC to switch from the saturated current control mode to the voltage control mode. Consequently,  $\phi_{opt}$  is defined as the optimal shift of saturated  $P - \delta$  curve that allows at once a transient stability enhancement and a post-fault recovering to the voltage control mode. The rightness of the analysis proposed in this subsection is validated through time domain simulations in the next subsection.

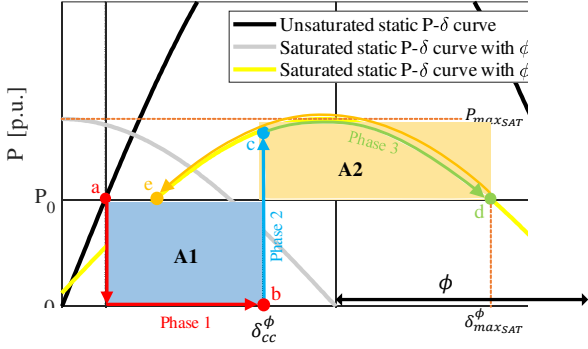


Fig. 8. Operation mechanism of the VSC under a 100% voltage sag by including  $\phi = 1.5$  rad.

#### D. Optimal Calculation of the Saturated Current Angle $\phi$

In order to avoid the internal angle being locked in the saturated current mode during the re-synchronization, the maximum value of  $\phi$  can be calculated in such a way that the operating points 'a' and 'e' in Fig. 9 are matched. Hence:

$$\phi \leq a \cos\left(\frac{P_0}{P_{maxSAT}}\right) + a \sin\left(\frac{P_0}{P_{max}}\right) \quad (13)$$

The value  $\phi$  obtained by (13) is the maximum allowable shift in the saturated quasi-static characteristic that guarantees the ability of the converter to switch back to the voltage control mode and a better transient stability compared to the case with  $\phi = 0$ . According to (13), the maximum value of  $\phi$  depends on the initial power set point and grid impedance. By defining the grid impedance with the short circuit ratio (SCR) of the grid as:  $SCR = (1/X_g)$ , the optimal value of  $\phi$  can be obtained by solving the following optimization problem:

$$\begin{cases} \phi_{opt} = \min \left\{ \phi = a \cos\left(\frac{P_0}{P_{maxSAT}}\right) + a \sin\left(\frac{P_0}{P_{max}}\right) \right\} \\ \text{constraints:} & 0 \leq P_0 \leq 1 \\ & SCR_{min} \leq SCR \leq SCR_{max} \end{cases} \quad (14)$$

To solve this problem, it is possible to simply draw a surface that relates  $\phi$  to the SCR and  $P_0$  as shown in Fig. 9. It can be seen that for a wide range of SCR and various initial operating power, the maximum value of  $\phi$  that satisfies the constraints is around 0.8 radian. Therefore,  $\phi_{opt} = 0.8$  [rad] is considered as the optimal value. It should be mentioned that  $SCR = 1.2$  corresponds to the minimum grid impedance that allows the VSC to transfer 1 pu active power (according to (3)).

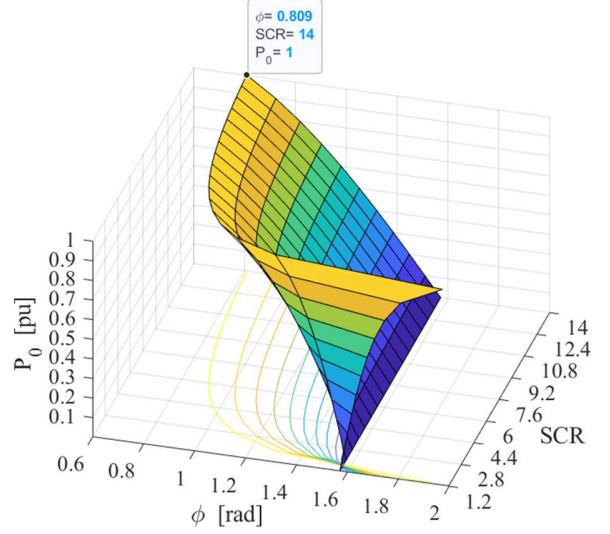


Fig. 9. The angle  $\phi$  with respect to the variation of SCR and power setpoint.

Considering the given parameters in Table I and the initial power setpoint of  $P_0 = 1$ , Fig. 10 shows the simulation results with two different values of  $\phi$ . In case that  $\phi = \phi_{opt}$ , the theoretical value of CCT is  $t_{cc} = 96$  [ms], which is higher than the CCT in the case of  $\phi = 0$ . As it can be seen, the system, switches back to the voltage control mode approximately in 1200 [ms] after the beginning of the transient. If  $\phi = 1.5$  [rad] ( $\phi > \phi_{opt}$ ), the system remains stable and  $P = P_0$  in steady-state. However, the angle reaches a new operating point, which is higher than the pre-fault value  $\delta_0$ . Consequently, the VSC operating remains in the saturated current mode, as shown by the curve of the current  $I_{s,rms}$ , and the voltage is no longer under control. This verifies the presented claims in subsection II.C.

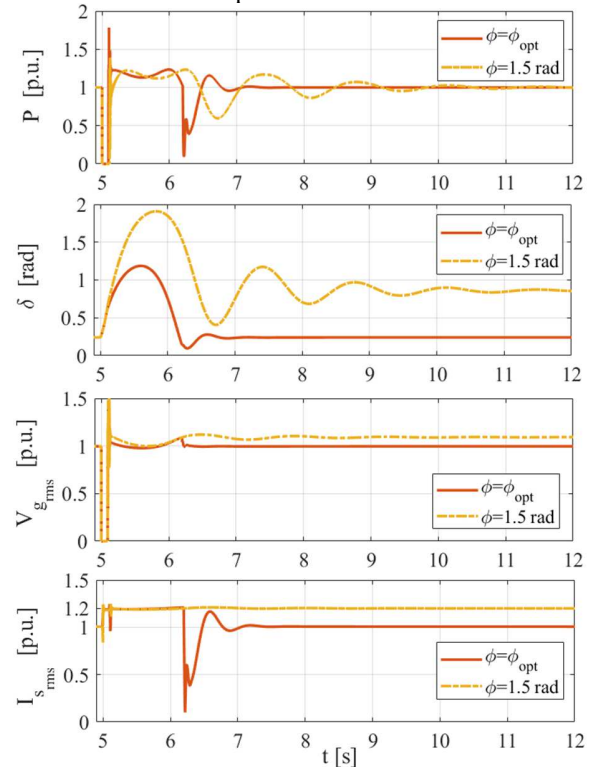


Fig. 10. Effect of including  $\phi$  in the control on transient stability in case of a 100% voltage sag.



I am curious to see also the time variations of control variables : the speed  $\omega_g$  and  $\theta_g$ .

Table IV presents the CCT values while including the current angle shift for different power setpoints. These results confirm that the proposed method can enhance the transient stability and (12) gives a satisfactory accuracy in the pre calculated CCT.

TABLE IV  
RESULTS OF THE CCT DETERMINATION

$P_0$	$\phi = \phi_{opt}$	
	Predicted CCT by (12)	CCT in simulation
1 pu	96 ms	94 ms
0.9 pu	135 ms	130 ms
0.8 pu	175 ms	164 ms
0.7 pu	217 ms	204 ms
0.6 pu	266 ms	247 ms
0.5 pu	325 ms	304 ms

### E. Impact of the Saturated Current Angle $\phi$ on the Transient Stability in Case of a Generic Voltage Sag

In order to validate that the proposed transient stability enhancement method with the current reference angle is effective in more general cases, a given voltage drop ( $\Delta V$ ) in the grid voltage is considered as follows:

$$\Delta V = 1 - V_{e_{drop}} \quad (15)$$

Considering  $\phi = 0$ , the quasi-static expression of the active power during the fault is:

$$P = V_{e_{drop}} I_{maxSAT} \cos(\delta) \quad (16)$$

Fig. 11 shows the operation mechanism of the grid-forming VSC subjected to a generic voltage sag. The various phases are the same as previously. The only difference is that during the fault (Phase 1), some amount of active power is exchanged with the grid by the VSC that can be determined with (15). According to the large signal model presented in Fig. 5, this injection of the power during the fault reduces the divergence speed of the angle  $\delta$ . Therefore, it is expected that the CCT in this case is higher than the one with a 100% voltage drop.

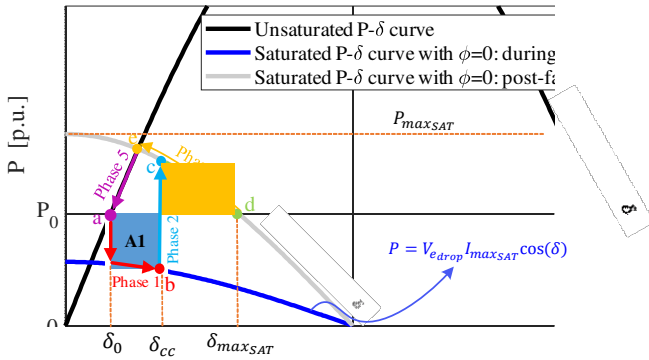


Fig. 11. Operation mechanism of the VSC under a generic voltage sag with  $\phi = 0$ .

If  $\phi = \phi_{opt}$ , the quasi-static expression of the active power during the fault is updated to:

$$P = V_{e_{drop}} I_{maxSAT} \cos(\delta - \phi_{opt}) \quad (17)$$

Fig. 12 shows the operation mechanism of the grid-forming VSC subjected to a generic voltage sag with optimally shifted

saturated  $P - \delta$  curves. Since the maximum allowable angle is increased in this case ( $\delta_{maxSAT}^{\phi} > \delta_{maxSAT}$ ), it is expected to get a higher CCT. Having in mind that the optimal value of  $\phi$  is based on matching the intersection point of the unsaturated  $P - \delta$  curve and saturated one during the post-fault, since the saturated curve in the post fault (yellow curve) is not affected by the magnitude of the voltage drop, the optimal value of  $\phi$  remains unchanged.

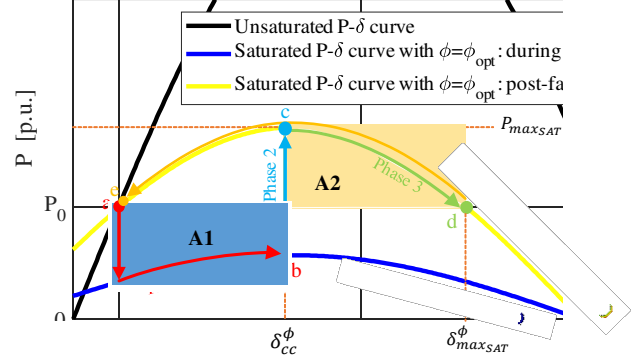


Fig. 12. Operation mechanism of the VSC under a generic voltage sag with  $\phi = \phi_{opt}$ .

Considering the given parameters in Table I, and taking  $P_0 = 1$  pu as an illustrative example, Fig. 13 shows the simulation results for a 20% grid voltage sag. The fault time durations ( $t_{f1}, t_{f2}$ ) are equal to CCTs ( $t_{cc1}, t_{cc2}$ ) in each case. It can be seen that the proposed optimal setting of the saturated current angle increases the CCT and the dynamic simulations are matched to the described operation phases in quasi-static state.

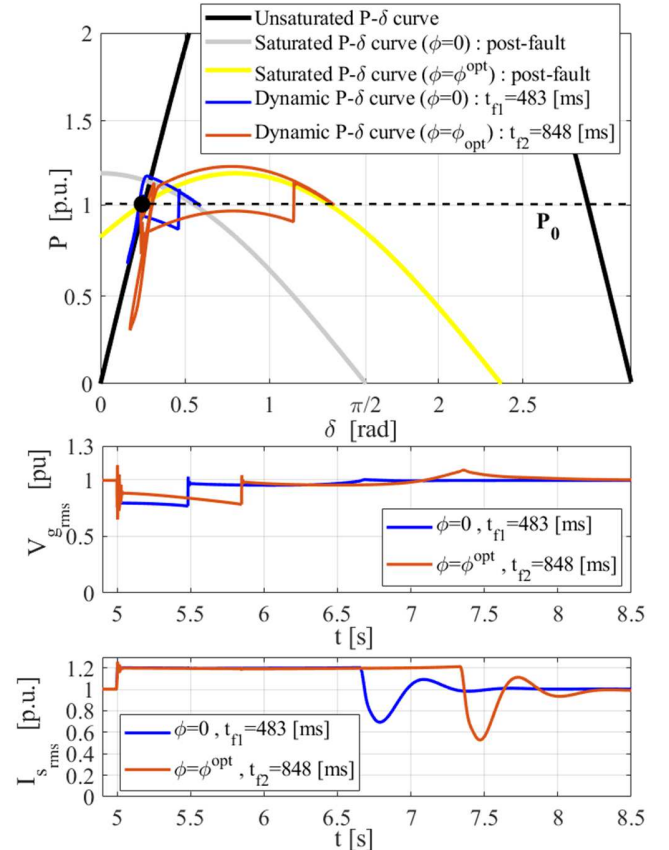


Fig. 13. Simulation results in case of a 20% grid voltage sag.

#### IV. TRANSIENT STABILITY ANALYSIS IN CASE OF A PHASE SHIFT

Another large event, which can happen in the grid, is a line tripping/reclosing. Due to the large grid impedance variation, it results in a phase shift [24]. The stability of the VSC has to be analyzed, especially in case of weak grid conditions. To analyze this effect, a small benchmark is studied (see Fig. 14). Depending on the  $K_2$  breaker position, the short circuit ratio is  $SCR_1 = \frac{1}{X_{g1}}$  or  $SCR_2 = \frac{X_{g1}+X_{g2}}{X_{g1} \cdot X_{g2}}$ .

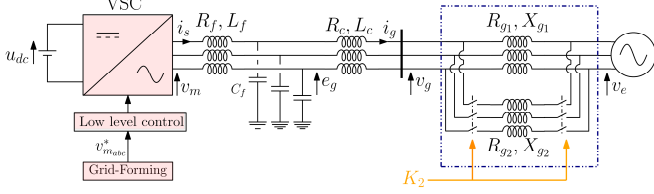


Fig. 14. Studied system with a line tripping/reclosing scenario.

As previously, the different phases are described with the help of some curves derived from the quasi-static models.

Considering the line-tripping scenario, according to Fig. 15, the VSC is initially operating at the point B located on the light blue curve with  $SCR = SCR_2$ . When the second line is tripped, the operating point suddenly moves to the other curve with  $SCR = SCR_1$  (black curve) while keeping the same angle (point C) and then the angle increases to reach the point A, where the initial operating point (power before the fault) is recovered. It should be mentioned that in this scenario, since the grid impedance suddenly increases, the current is initially dropped and then incrementally reaches to the value corresponding to  $P_0$ , the CSA is not activated.

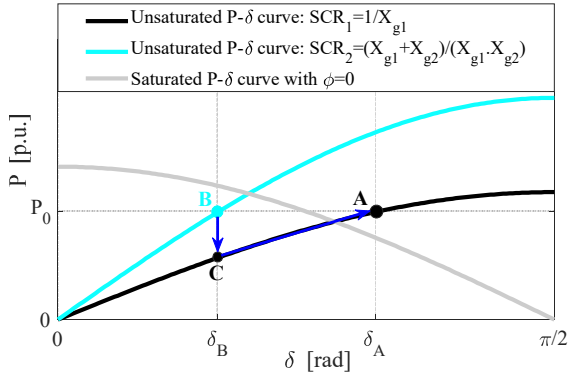


Fig. 15. Operation mechanism of the VSC in case of line tripping under low SCR.

Considering the line-reclosing scenario, according to Fig. 16, the VSC is initially operating at the point A. When connecting the second line, it is expected that the operating point jumps to the other curve with  $SCR = SCR_2$  (light blue curve) while keeping the same angle (operating point D). However, reclosing the line activates the CSA due to a sudden decrease of the connection impedance and therefore, the operating point moves to the saturated curve to limit the current (operating point E). At this point, the active power is smaller than its setpoint. Therefore, the angle  $\delta$  diverges and the VSC loses the synchronism. Actually, the instability issue caused by a line

reclosing is linked to the location of the initial operating point with respect to the saturated curve in the  $P - \delta$  plane. If the initial operating power is located above the saturated quasi-static  $P - \delta$  curve, then the system loses the synchronism as explained previously. If the initial operating point is below the saturated curve (A'), the operating point moves to E', whose corresponding power is higher than the initial power setpoint. Therefore, the angle decreases to reach its new equilibrium point (B').

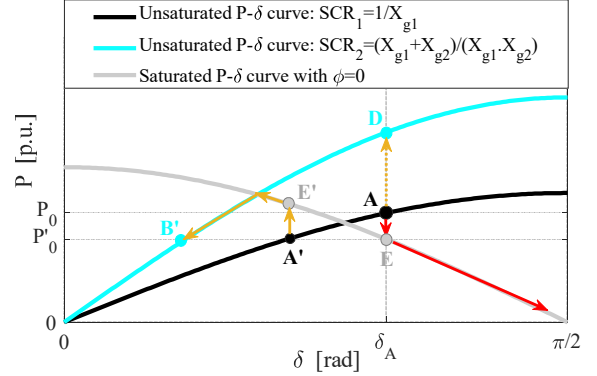


Fig. 16. Operation mechanism of the VSC in case of line reclosing under low SCR.

According to the coordinates of the initial operating point with respect to the saturated current curve, the following constraints on the initial angle and therefore on the initial power setpoint can be derived to guarantee a stable line reclosing:

$$\begin{cases} P_0 \leq V_e I_{maxSAT} \cos(\delta_0) \\ P_0 = P_{max1} \sin(\delta_0) \end{cases} \quad (18)$$

where  $P_{max1} = \frac{E_g V_e}{X_c + SCR_1}$ . Therefore:

$$\delta_0 \leq \text{atan} \left( \frac{I_{maxSAT} (X_c + \frac{1}{SCR_1})}{E_g} \right) \quad (19)$$

$$P_0 \leq P_{max1} \sin \left( \text{atan} \left( \frac{I_{maxSAT} (X_c + \frac{1}{SCR_1})}{E_g} \right) \right) \quad (20)$$

Using the proposed shifting of the saturated current curve to the right side of the  $P - \delta$  plane, (19) is updated to (20) as follows:

$$P_0 \leq P_{max1} \sin \left( \text{atan} \left( \frac{I_{maxSAT} (X_c + \frac{1}{SCR_1})}{E_g - (I_{maxSAT} (X_c + \frac{1}{SCR_1})) \cdot \sin \phi} \right) \cdot \cos \phi \right) \quad (21)$$

By setting  $\phi = \phi_{opt}$  in (21), Fig. 17 demonstrates the capability of the VSC to deal with the line-reclosing for the full range of initial power set point ( $0 \leq P_0 \leq 1$ ) under very low grid impedances.

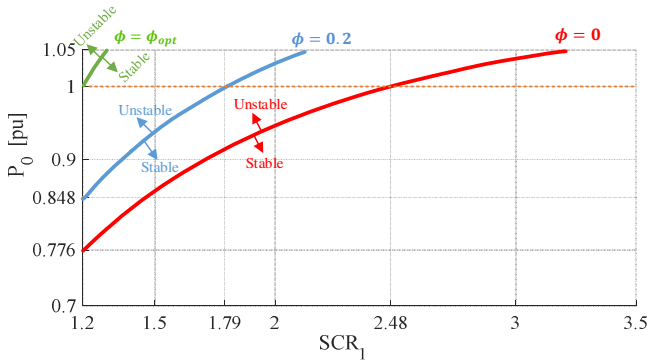


Fig. 17. Effect of shifting the saturated quasi-static  $P - \delta$  curve on the stability region in case of a line reclosing.

To verify the correctness of the presented analysis, we consider  $P_0 = 1$  [pu],  $SCR_1 = 1.2$ ,  $SCR_2 = 2.4$  and simulate the line reclosing. In this situation, according to Fig. 18, if  $\phi = 0$  rad, it is expected that the VSC loses the synchronism, while if  $\phi = \phi_{opt}$ , it stably shifts to a new operating point. It can be seen that with the proposed setting of the angle  $\phi$ , the VSC can stably deal with the phase shift.

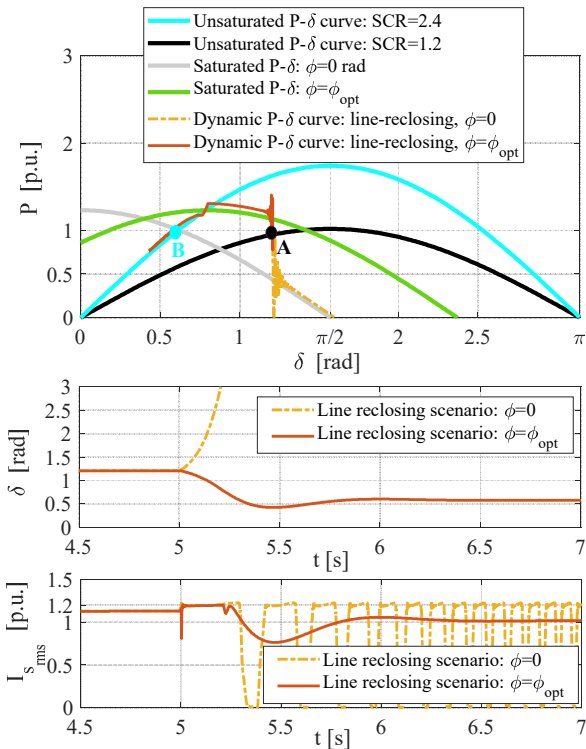


Fig. 18. Dynamic simulation of the line-reclosing under low SCR.

## V. EXPERIMENTAL VALIDATION IN DYNAMIC STATE

The aim of this section is to validate experimentally the theoretical developments. The experimental bench is illustrated in Fig. 19.

The 2-Level VSC (1) is supplied by an ideal 600V DC voltage source (4) and connected to a high bandwidth AC amplifier (5) through an LCL filter (3) as depicted in Fig. 20. Table V presents the mockup parameters. The amplifier is used to emulate the AC system (i.e.; 300V ph-ph) as well as to generate the events discussed in this paper (i.e.; 100% voltage sag emulating a 3-

phase bolted fault). The 2-Level VSC is controlled with a dSPACE ds1005 (2) with a  $40 \mu s$  time step. The switching frequency of the converter is  $f_{sw} = 10kHz$ .

Two test cases are performed:

- A 100 % voltage sag considering  $\phi = 0$ .
- A 100 % voltage sag considering  $\phi = \phi_{opt}$ .

### A. A 100 % Voltage Sag Considering $\phi = 0$

Initially,  $P_0 = 0.6$  [p.u]. Subsequently, a 100 % voltage sag with the 200 ms duration is applied to the system. According to Table II when  $\phi = 0$ , the CCT obtained from the simulation is 157 ms. Hence, it is expected that the system cannot be operated stably under this fault duration.

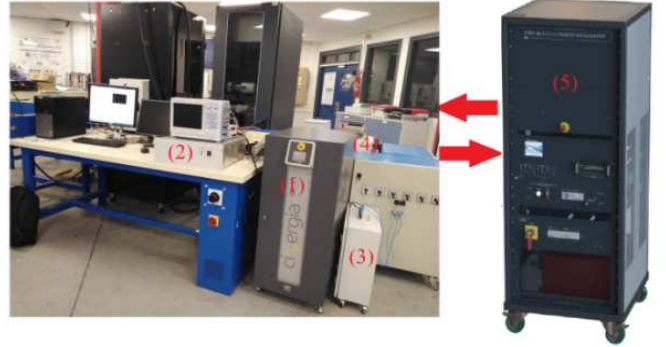


Fig. 19. Mockup presentation.

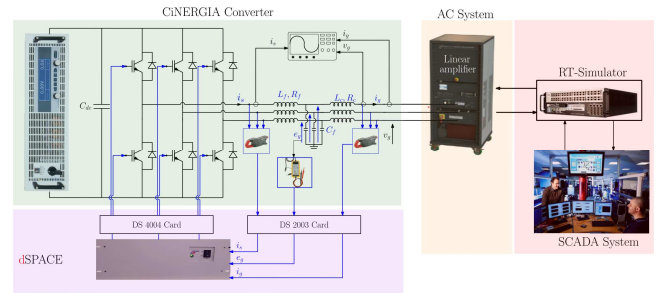
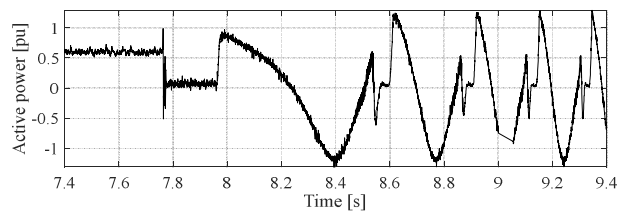


Fig. 20. Functional scheme.

TABLE V  
MOCKUP PARAMETERS

$S_n$	5,625 kVA	$L_f$	10.9mH
$I_n$	10 A	$L_c$	10.9mH
$f_n$	50 Hz	$C_f$	9.2 $\mu F$

Fig. 21 shows the output power, voltage and current of the VSC in response to the fault. It can be clearly seen that the VSC loses the synchronism and it becomes unstable.



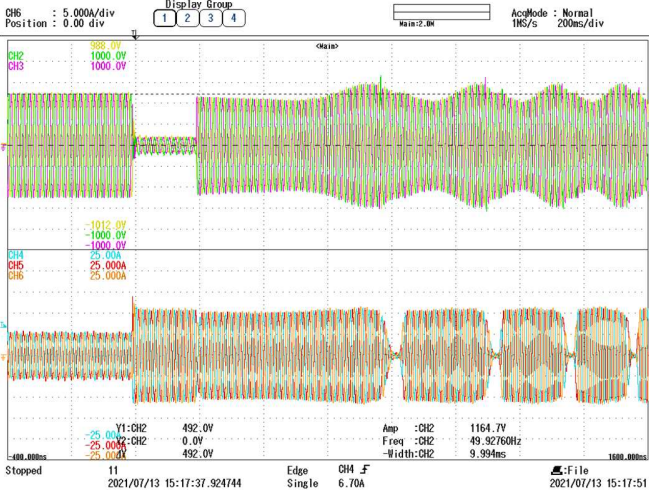


Fig. 21. Response to a 100 % voltage sag with the duration of 200 ms considering  $\phi = 0$ .

I am curious to see also the time variations of control variables : the speed  $\omega_g$  and  $\theta_g, \theta_p$

### B. A 100 % Voltage Sag Considering $\phi = \phi_{opt}$

As in the previous case, the active power reference  $P_0$  is set to 0.6 [p.u] and a 100 % voltage sag with the duration of 200 ms is applied to the system. According to Table IV, when  $\phi = \phi_{opt}$  the CCT obtained from the simulation is 247 ms. Hence, it is expected that the VSC does not lose the synchronism and recovers the initial operating point stably. Fig. 22 demonstrates the stable performance of the VSC under this scenario, which confirms the effectiveness of the proposed method.

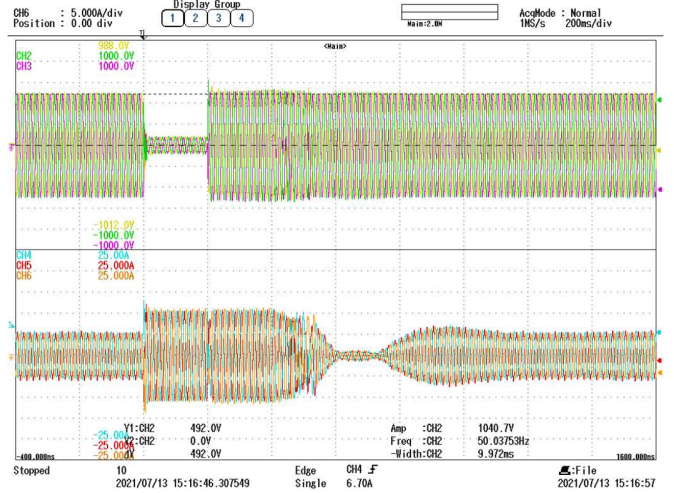
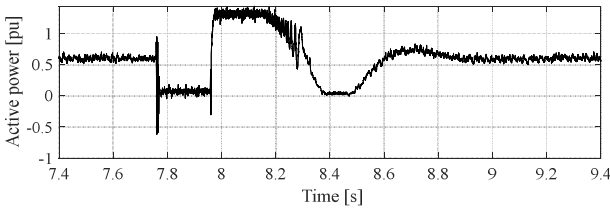


Fig. 22. Response to a 100 % voltage sag with the duration of 200 ms considering  $\phi = \phi_{opt}$ .

I am curious to see also the time variations of control variables : the speed  $\omega_g$  and  $\theta_g, \theta_p$

## VI. CONCLUSION

In this paper, the transient stability of the grid-forming control embedding a current saturation algorithm as the control limiting strategy has been investigated. In case of large grid disturbances, the converter switches to the saturated current control mode. According to the active power expression in this control mode, a new degree of freedom is identified, which is the angle of the saturated current reference. Thanks to the derived formulas for the critical clearing angle and critical clearing time in case of a voltage sag event, the impact of this angle on the transient stability has been investigated and its optimal value has been calculated. It was also demonstrated that this optimal value enhances the stability margin in case of a phase shift event. It has been demonstrated that this angle has a better positive effect in the case of a phase shift than for a voltage sag. This is explained by the fact that the proposed method does not prevent the power angle deviation caused by

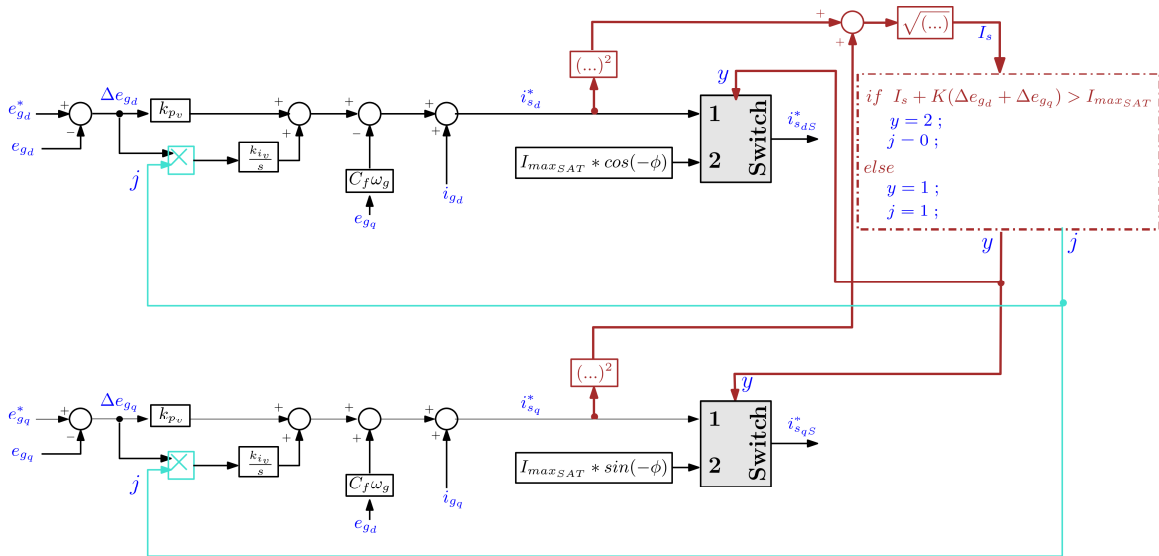
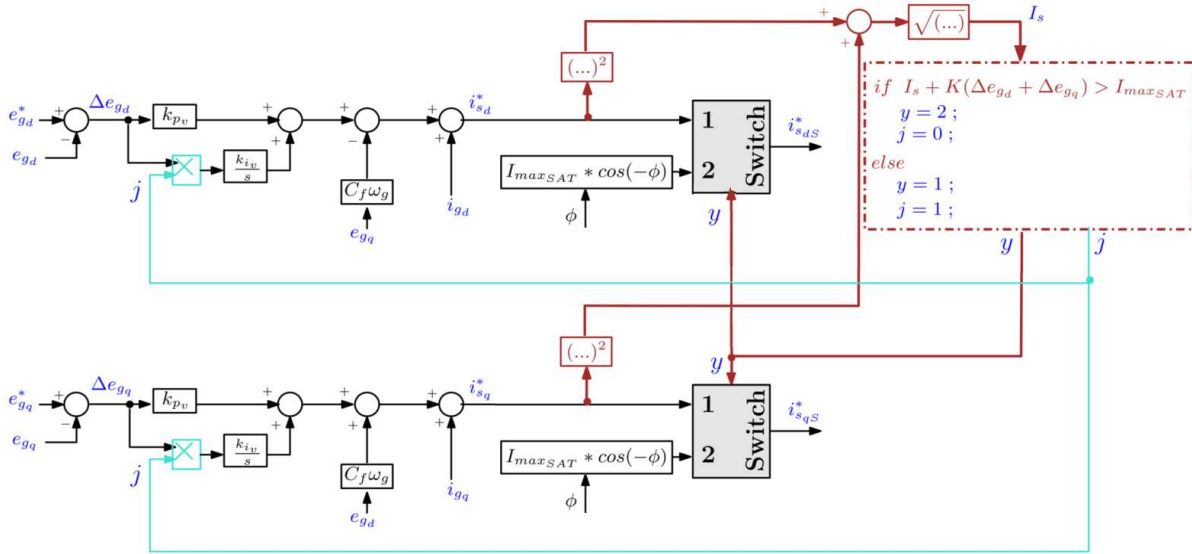


Fig. A-1. Structure of the implemented CSA and anti-windup ( $K = 1$ ). The angle  $\phi$  is a control variable (as shown in fig.5), so I have added it in the figure below I have re organized also the figure. Take care of the sum symbols that are not drawn as previously (see fig 5, fig.2)



the power mismatch in the power control loop during the fault.

The overall idea of this paper is to promote some simple methods in order to improve these kinds of control. Of course, some more advanced controls can be found in the literature but it seems important to use all the possible degrees of freedom of these kinds of control in order to push these methods to their limit and evaluate with cases more advanced control can really bring some better performance.

Another possibility is to use a combination of the proposed solution with an additional transient management of the active power set point or inertia constant that would result in a higher system performance. In the future works, more focus will be made on the dynamic management of the proposed control degree of freedom. Moreover, it is worthy to compare the effect of using different current limiting strategies (i.e. current saturation algorithm and virtual impedance) on transient stability in case of various grid events.

#### APPENDIX

During the operation of the converter in saturated current mode, an anti-windup on the voltage PI controller is required. Fig. A-1 shows the implemented CSA and anti-windup strategy. In voltage control mode,  $\Delta e_{gd} = \Delta e_{gq} = 0$  and the current magnitude is less than the threshold  $I_{maxSAT}$ . Therefore, the input "1" of the switches appears in the output ( $i_{sdq}^* = i_{sdq}^*$ ). When a fault activates the saturation mode, the input (2) passes through the switches. During the saturated current operation mode, the integrator is frozen by multiplying its input to zero. Note that the voltage errors  $\Delta e_{gdq}$  are used to eliminate the switching effect around  $I_{maxSAT}$ . As soon as the voltage is recovered to 1 pu,  $\Delta e_{gdq} = 0$  and the converter switches back to the voltage control mode.

#### ACKNOWLEDGMENT

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