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# Advanced TCAD Simulation of Tunnel Oxide Degradation for EEPROM Applications

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**Abstract-** In this paper we have simulated dynamic Constant Voltage Stress (CVS) and subsequent degradation of MOS capacitor representative of Non-Volatile Memory (NVM) devices. Oxide degradation was modelled through trap defects generation at SiO<sub>2</sub>/Si interface and SiO<sub>2</sub> bulk. A very good agreement was obtained between simulation and experimental data.

## I. INTRODUCTION

Charge Storage Floating Gate-based Non-Volatile Memory Electrically Erasable Programmable Read Only Memory (EEPROM) and Flash-EEPROM (or, more simply, Flash), are among the most successful devices ever introduced in the semiconductor market [1]. Either stand-alone in Storage Charge Memory (SCM) or embedded in Microcontroller Units (MCUs), they are at the very core of every modern digital equipment, from digital cameras to smartphones, tablets and personal computers, to mention a few. Their operating principle relies in charge transfer from/to a polysilicon layer (called floating gate) through a thin silicon dioxide layer (called tunnel oxide) when appropriate voltage biases are applied to control gate and silicon substrate (Fig.1a, for EEPROM). The basic element for both EEPROM and Flash is therefore a simple PolySi/SiO<sub>2</sub>/Si stack planar capacitor, commonly called MOS capacitor (Fig.1b). The oxide integrity is what ultimately determines the devices' reliability, and consequently, it has been extensively studied in the past three decades [2-5].

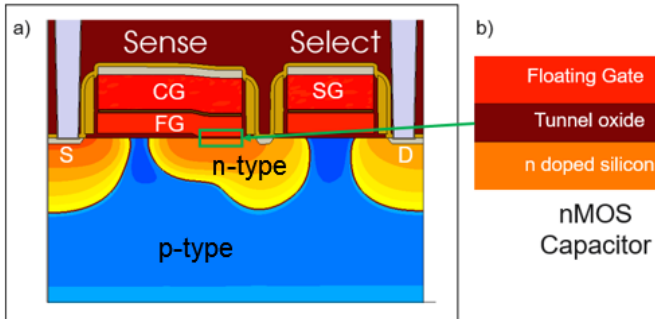


Figure 1: a) EEPROM 2T device, consisting of a Sense Transistor (for data storage) and Select Transistor (for data accessing). b) Basic storage element of Sense device is a planar capacitor.

In this paper, we have performed Technology Computer Aided Design (TCAD) simulations of MOS oxide degradation due to Constant Voltage Stress (CVS). The applied voltage stress is representative of the operating conditions of a 110 nm-CMOS technology node-based 4Mbit EEPROM manufactured by STMicroelectronics and recently introduced in the semiconductor market [6].

## II. TCAD Simulation Framework

This study was carried out using Sentaurus™ Suite by SYNOPSYS®, for both process and electrical simulations [7]. Process simulation was based on a 110 nm embedded NVM CMOS technology. All the relevant front-end process flow steps were included up to metal contacts. The obtained TCAD nMOS structure is shown in Fig.2a and corresponds to a large plate capacitor device with an area of  $1 \times 10^5 \mu\text{m}^2$  (in this 2D simulation total surface was taken into account by a scaling area factor). Tunnel oxide thickness is around 8 nm, as measured in TEM cross section (Fig.2b).

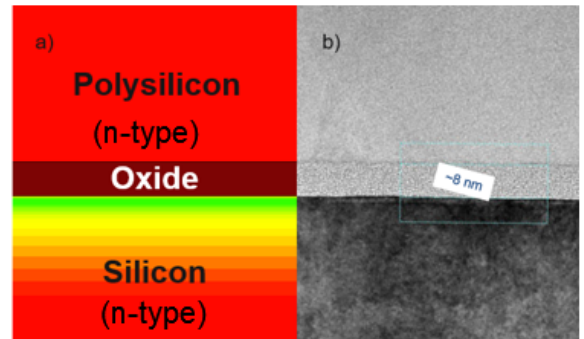


Figure 2: Planar MOS Capacitor. a) TCAD process simulation. b) TEM cross section

### A. Charge transport across tunnel oxide

For typical EEPROM operating voltages ( $> 10 \text{ V}$ ) and tunnel oxide thickness ( $7 \sim 10 \text{ nm}$ ), charge transport across the silicon dioxide is driven by quantum mechanical tunneling through a trapezoidal potential barrier. This phenomenon was first described by Fowler and Nordheim (FN), with a simple

closed-form expression for the current density  $J_{FN}$  that is given by [8, 9]:

$$J_{FN} = AF^2 \exp(-B/F) \quad (1)$$

where  $F$  is the electric field at the Si/SiO<sub>2</sub> interface and  $A$ ,  $B$  are physical related parameters. Despite its utility in modeling high field tunneling current thanks to its reliability and simplicity, this model doesn't cover direct tunneling for ultra-thin oxide and trap assisted tunneling of degraded oxide. Consequently, a more general model [10] is used in this paper, that considers band edge profile along the entire path across the SiO<sub>2</sub> between the two points connected by tunneling, also called Non-Local Tunneling (NLT) [8]. The key parameter in NLT is the electron effective tunneling mass, which has been set equal to 0.48 times the electron mass. Moreover, coupled with trap capture and emission models described in [8][11][12], the simulation accounts for traps assisted tunneling (TAT) thus covering a wide spectrum of tunneling phenomena.

### B. Degradation model

Several models for oxide degradation under high voltage stress can be found in the literature. According to anode hole injection (AHI) mechanism, some of the tunneling electrons reaching the anode with high-enough energy will generate electron-hole pairs in the oxide, and some of the generated holes will be trapped in the oxide [13-15]. This mechanism was initially heralded as the origin of dielectric breakdown, a claim that was first disputed [16] and later disproven [17]. According to another model, hot electrons release hydrogen (HR) near the anode which drift or diffuse through SiO<sub>2</sub> consequently generating defects [18,19,20]. In this paper, defects generation is modeled by stress-induced breaking of Si-H bonds (depassivation). From first-order kinetics [8][21] Si-H concentration  $N_{hb}$  is given by:

$$\frac{dN_{hb}}{dt} = -v * N_{hb} \quad (2)$$

where  $v$  is a reaction constant that can be described approximately by an Arrhenius law [22]:

$$v = v_0 \exp\left(\frac{-\varepsilon_A}{kT}\right) k_{tun} \quad (3)$$

where  $v_0$  is the reaction depassivation constant,  $k$  is the Boltzmann constant,  $T$  is the absolute temperature, and  $k_{tun} = 1 + \delta_{tun}(I_t/I_0)^{\rho_{tun}}$  is an enhancement factor due to tunneling current  $I_t$ . The activation energy  $\varepsilon_A$  (not constant) is given by:

$$\varepsilon_A = \varepsilon_A^0 - \delta_{\perp}|F|^{\rho_{\perp}} + kT(1 + \beta F) \ln\left(\frac{N - N_{hb}}{N - N_{hb}^0}\right) \quad (4)$$

where  $\varepsilon_A^0$  is the activation energy constant,  $N_{hb}^0$  is the initial Si-H concentration and  $\beta$ ,  $\delta_{\perp}$ ,  $\rho_{\perp}$  are field-enhanced parameters.  $N$  is the trap concentration saturation value and

varies as a function of energy within the bandgap,  $N - N_{hb}$  is the concentration of hydrogen released (i.e concentration of traps) and  $N - N_{hb}^0$  corresponds to the initial concentration of traps which we have set to  $1 \times 10^{12} \text{ cm}^{-2}$ . Although this model was first developed to describe Si-H breaking mechanism occurring at Si/SiO<sub>2</sub> interface, we have extended it to the bulk oxide where we have set  $N - N_{hb}^0$  equal to  $1 \times 10^{12} \text{ cm}^{-3}$ . The complete parameter set used for simulations is reported on Table 1 below.

Table 1: Degradation model parameters set

Parameter	Value	Unit
$v_0$	$2.1 \times 10^{-12}$	$\text{s}^{-1}$
$\varepsilon_A^0$	0	eV
$T$	300	K
$\beta$	$1.0 \times 10^{-7}$	
$\delta_{tun}$	$8.9 \times 10^5$	
$\rho_{tun}$	0.9	
$\delta_{\perp}$	1e-3	
$\rho_{\perp}$	0.33	

### C. Traps distribution

Distribution of the trap concentration parameter  $N$  in bulk oxide and at Si/SiO<sub>2</sub> interface are reported in Fig.3 and Fig .4, respectively. For bulk oxide traps, following [23] we have assumed that for each acceptor trap there is a corresponding donor trap. Thus, traps in SiO<sub>2</sub> are generated in the whole bandgap (but only acceptors levels are represented in Fig.3).

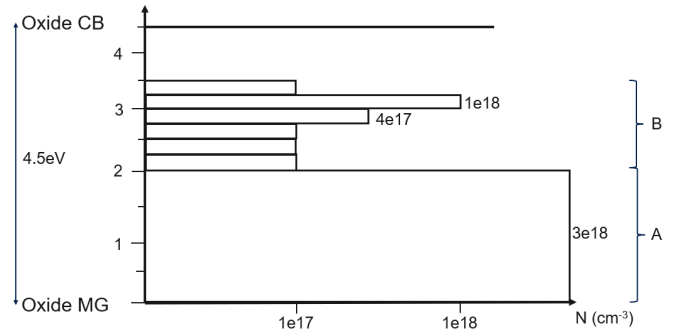


Figure 3: Distribution of traps parameter  $N$  in bulk SiO<sub>2</sub>. Only the upper part of the band gap is shown (energy levels relative to the mid-gap).

Since we neglected impact ionization during electron injection into polysilicon gate, donor traps stay mostly neutral because no hole are available for trapping. Deep acceptor traps (A), which extend 2 eV from mid-gap (MG), are mostly filled with electrons and have low probability for electron release. This negative trapped charge is responsible for Fowler-Nordheim efficiency reduction. Shallow traps (B) located within the range 2 eV to 3.5 eV from MG, have high capture

and emission rates and trigger TAT mechanism. Finally, we assumed that very shallow traps located above 3.5 eV from MG are neutral with a too low capture probability to have any significant effect. We have therefore neglected them.

At Si/SiO<sub>2</sub> interface traps spread over the entire silicon bandgap (Fig. 4), both acceptor and donor states are therefore included in this model. Acceptor states, however, have higher concentrations. The concentration peak located at 0.8 eV from the valence band edge is the typical signature of Pb0 center [24] and was reported by the authors in [25], who performed similar stress to ours.

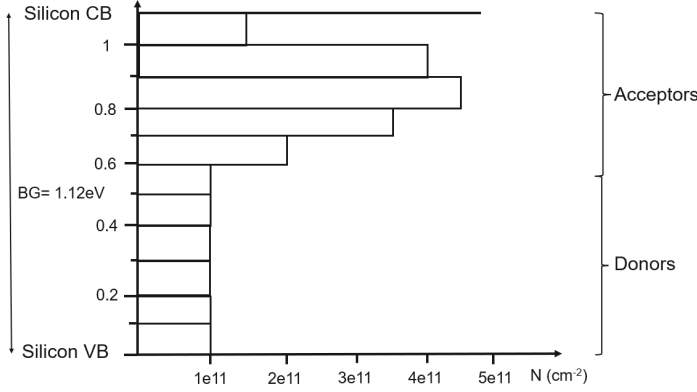


Figure 4: Distribution of traps parameter  $N$  at Si/SiO<sub>2</sub> interface. Both acceptors and donors states are included in the simulation.

The spatial location of traps is schematically represented in Fig. 5. At the interface, we set a uniform spatial distribution along the entire interface. Furthermore, shallow traps (B) were distributed mainly at the center of the oxide (when they are positioned close to interface, it induces nonrealistic simulated tunneling current value), whereas deep traps (A) evenly distributed inside SiO<sub>2</sub>.

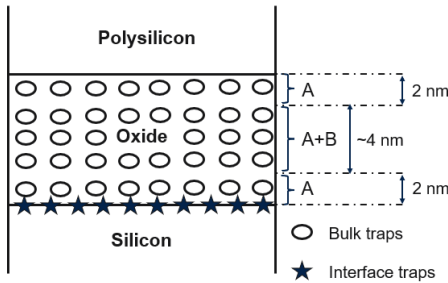


Figure 5: Traps spatial distribution. Deep traps (A) are uniformly distributed in the oxide. Shallow traps (B) are mainly located at the SiO<sub>2</sub> center.

### III. Results & Discussion

#### A. Constant Voltage Stress (CVS)

In Fig. 6, the measured and simulated CVS curves are represented. Since deep traps located near MG (A traps in Fig. 3) have highest electron capture section, they will charge

negatively, leading to the observed gate current decrease during CVS.

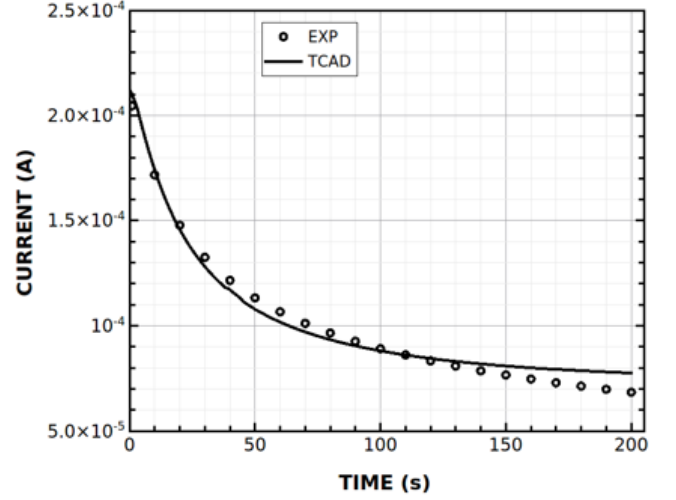


Figure 6: Gate current during Constant Voltage Stress (CVS).

This mechanism is well captured in our simulations, leading to the excellent agreement with experimental data.

#### B. Capacitance vs Voltage (C-V)

The measured and simulated C-V curves before and after stress are shown in Fig. 7, where we can appreciate a very good agreement between the two. The reason is briefly explained in the following considerations Si/SiO<sub>2</sub> interface traps are very sensitivity to the electrostatic field, since small change in the applied voltage (few volts) drastically modify their occupancy state. They therefore strongly influence the C-V shape after oxide degradation.

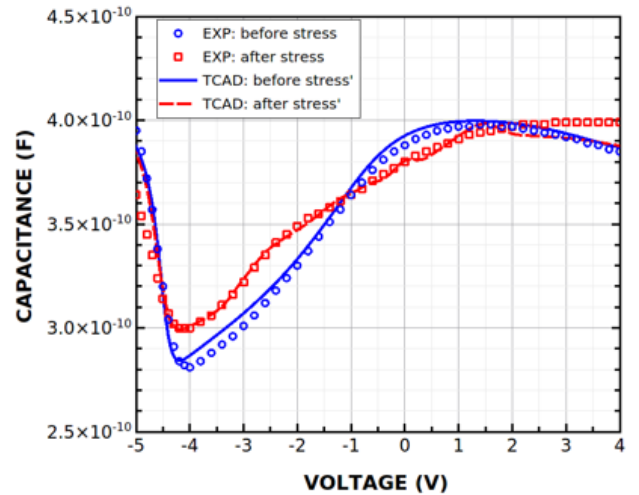


Figure 7: Capacitance vs voltage before and after stress.

A detailed analysis of C-V after laser induced degradation on MOS [26] showed that donor interface traps (i.e traps with an energy level between the valence band and the mid gap) are the first to release their holes becoming neutral from positively charged, then acceptor interface traps (i.e traps with an energy level between de mid gap and the conduction band) capture electrons and become negatively charged. Assuming this to be also valid after CVS induced oxide degradation, from -4.5 V to -3 V the capacitance degradation is ruled by donor traps, then from -3 V to -1.5 V by acceptor traps and, finally, above -1.5 V there is the cumulate influence of filled interface traps and bulk oxide traps. The small C-V mismatch in the strong inversion regime (above 2V), where poly-depletion effects are known to take place, are likely due to poor TCAD electrical modelling of PolySi.

### C. Gate Tunneling Current

In Fig.8, the measured and simulated I-V curves are represented before and after CVS.

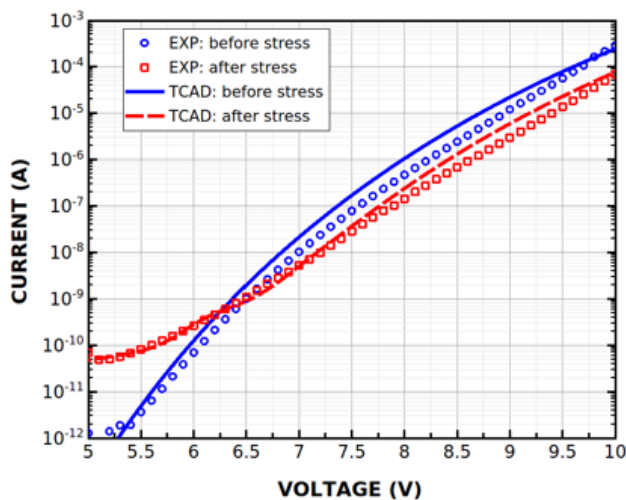


Figure 8: Capacitance vs voltage before and after stress

For an oxide of approximately 8 nm thick and at low electric field, gate current is mostly due to TAT. At high field, gate current main contributor is Fowler-Nordheim tunneling mechanism.

Concerning the unstressed nMOS capacitor, gate current follows, as expected, a pure Fowler-Nordheim injection curve from 5.5 V to 10 V. On stressed nMOS capacitor, from 5 V to 6 V, TAT is the main contributor to gate current. A combination of TAT and Fowler-Nordheim is observed between 6V to 7V and above, Fowler-Nordheim mechanism becomes preponderant.

Vertical cuts (TCAD simulated structure) of volumetric trap concentration after stress and electrostatic field at  $V_g=10V$  are shown in Fig.9. Due to higher electrostatic field close to the gate, traps concentration increase.

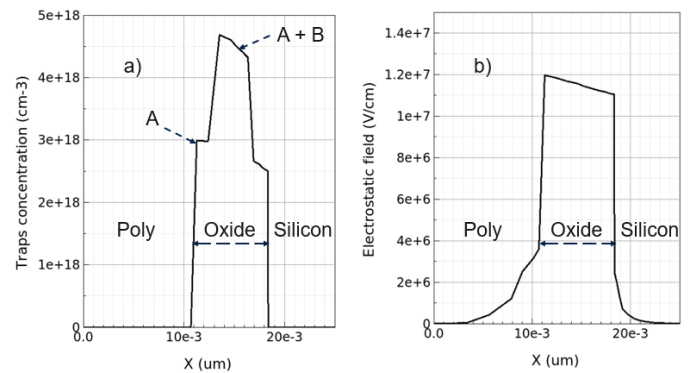


Figure 9: a) Vertical cut of volumetric trap concentration and b) Vertical cut of electrostatic field

However, the impact of electric field is probably overestimated here since we have neglected traps generation due to high kinetic energy injected electrons.

### V. Conclusion

In this paper, we have performed advanced TCAD simulation of NVM device tunnel oxide degradation during Constant Voltage Stress. We showed that Si/SiO<sub>2</sub> interface traps modify MOS electrostatic behavior throughout capacitance versus voltage measure, whereas SiO<sub>2</sub> bulk acceptor-type traps lead to Fowler-Nordheim tunneling current decrease and to TAT at lower electric field. A very good agreement with experiments was obtained for C-V and I-V pre and post stress. The model used in these simulations could be further improved using dedicated degradation kinetics for bulk and interface traps. Finally, this approach can be easily implemented for endurance and retention simulation of industrial NVM devices.

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