



HAL
open science

STATE: A Test Structure for Rapid Prediction of Resistive RAM Electrical Parameter Variability

Hassen Aziza, Jeremy Postel-Pellerin, Hussein Bazzi, Mathieu Moreau, Adnan Harb

► **To cite this version:**

Hassen Aziza, Jeremy Postel-Pellerin, Hussein Bazzi, Mathieu Moreau, Adnan Harb. STATE: A Test Structure for Rapid Prediction of Resistive RAM Electrical Parameter Variability. IEEE International Symposium on Circuits and Systems (ISCAS) 2022, May 2022, Austin, United States. pp.3532-3536, 10.1109/ISCAS48785.2022.9937716 . hal-03941188

HAL Id: hal-03941188

<https://hal.science/hal-03941188v1>

Submitted on 22 Mar 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

STATE: A Test Structure for Rapid Prediction of Resistive RAM Electrical Parameter Variability

Hassen Aziza¹, Jeremy Postel-Pellerin¹, Hussein Bazzi^{1&2}, Mathieu Moreau¹, Adnan Harb²

¹Aix-Marseille Univ, Univ Toulon, CNRS, IM2NP, Marseille, France, ²Lebanese International University, Beirut, Lebanon.

Abstract— Resistive RAM (RRAM) design optimization and reliability monitoring is essential not only to gain market share in the highly competitive emerging memory sector, but also to enable future high-capacity and power-efficient brain-inspired systems, beyond the capabilities of today’s hardware. Common problems with RRAM are related to high variability in operating conditions and low yield. Although research has taken steps to resolve these issues, variability remains a major hurdle for the wide spread of the technology. In this paper, a novel test structure consisting of an array of non-addressable 1T-1R RRAM memory cells with parallel connection of all memory elements is introduced. The test structure can be used as a powerful tool for process variation monitoring during a new process technology introduction and also for marginal cell populations detection during process maturity. The test structure is designed to measure RRAM parameters of interest based on a simple measurement methodology: from the transfer characteristic measured under the select transistor clamping bias, it is possible to obtain accurate information on the RRAM switching parameters as well as the ON/OFF resistance values.

Keywords— RRAM, OxRAM, Test structure, Variability, Reliability, Emerging Memory.

I. INTRODUCTION

The race to follow Moore’s law to its ultimate limits has reached the RRAM technology, which is designed in nanoscale sizes for high density embedded memory applications [1-2]. With the device dimensions scale down to the nanoscale regime, the device variability has taken a crucial relevance into the device’s behavior [3]. In this context, RRAM intrinsic variability challenge has driven special attention to test structures [4-5]. The role of test structures in the development and monitoring of a technology and its applications has become ever more important as alternative hybrid technologies (i.e., CMOS combined with RRAM technologies) are introduced to go beyond Von Neumann architectures [6]. This is particularly true for Oxide-based RRAM technologies which have been applied to in-memory implementations of backpropagation algorithms to implement in-situ learning on edge systems [7].

RRAM devices are affected not only by the process variation but also by endurance degradation. It can cause drift in high and low resistance values, making the sensing difficult in the cell’s read process. The technology is ruled by stochastic mechanisms (ion generation, ion migration in the resistive layer, etc.), leading to variability [8]. Also, during the early phase of development, it is often difficult to obtain sufficient reliable data on RRAM memories as the process itself is not stabilized and fully functional devices are not yet available. Therefore, smart monitoring techniques are needed to track the RRAM electrical parameters of interest in order to recognize the reliable cells from the possible non-reliable ones.

In this work, we present a novel test structure referred to as STATE: StrucTure for rApid predicTion of RRAM Electrical parameter variability. The test structure is associated with an efficient characterization technique able to correctly measure electrical parameters temporal variations in RRAM. The STATE test chip is inspired from the STM-CAST structure presented in [9] which is extensively used in the floating gate memories. The circuit is very simple as it is an array of not addressable memory cells connected in parallel. Based on a straightforward measurement methodology, the test chip is designed to collect statistical data regarding RRAM critical electrical parameters: ON/OFF resistances and switching parameter distributions.

The contribution of the state-of-art in the field of test structures dedicated to RRAM technology is very limited. Most of the work focuses on the development of RRAM-dedicated test solutions. The process starts with the identification, characterization and development of accurate models of RRAM defects [10-11]. Based on these models, high quality and efficient test solutions are proposed [12]. None of these publications has investigated the design of test structures and their use for early reliability assessment of the technology or electrical parameter tracking during process maturity. The proposed work introduces a novel RRAM test structure which takes RRAM inline variability evaluation and analysis one step further. The main contributions of the paper are as follows:

- A novel test structure design allowing a tight monitoring of RRAM electrical parameters is introduced.
- A simple measurement methodology able to capture RRAM parameters is developed. The methodology is based on I-V transfer characteristics examination.
- A deep analysis of the I-V transfer characteristics is conducted, allowing to capture the RRAM switching kinetics variability in all operating conditions: FORMING (FMG), RESET (RST) and SET operations.

The remainder of this paper is organized as follows. Section II introduces the RRAM test structure. Section III is dedicated to experimental results. In section IV, a discussion and an analysis of the test structure results are provided. Section V concludes the paper.

II. RRAM TEST STRUCTURE

A. Background: RRAM technology

Fig. 1a shows the basic 1T-1R memory cell where one MOS transistor ($W = 0.8 \mu\text{m}$ and $L = 0.5 \mu\text{m}$) is connected in series with a RRAM cell. The RRAM cell consists of two electrodes, the top electrode (TE) and bottom electrode (BE), in between which a metallic Hafnium-based oxide is sandwiched [13]. A TiN BE is first deposited. Then, a 10nm-HfO₂/10nm-Ti/TiN stack is added to form a capacitor-like structure [14]. Fig. 1b presents a typical 1T-1R RRAM I-V characteristic in linear scale along with additional I-V curves

obtained over 15 programming cycles (light gray). Based on the I-V curve, the memory cell operation can be seen as follows: after an initial electro-FMG step [14], the memory element can be reversibly switched between the Low Resistance State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T-1R cell, i.e., V_{SET} to switch to LRS after a SET operation and V_{RST} to switch to HRS after a RST operation.

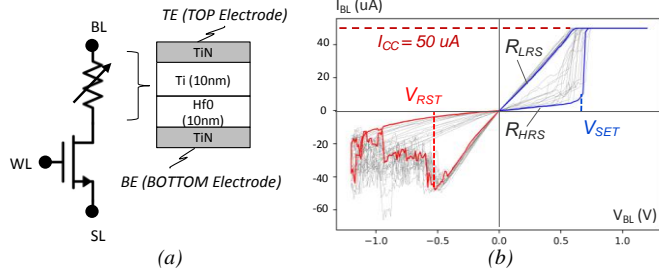


Fig. 1. (a) symbol view of a 1T-1R cell (b) RRAM I-V characteristics.

TABLE I. STANDARD CELL OPERATING VOLTAGES

	FMG	RST	SET	READ
WL	2V	2.5V	2V	2.5V
BL	3.3V	0V	1.2V	0.2V
SL	0V	1.2V	0V	0V
$R_{LRS/HRS}$	10 k Ω	240 k Ω	15 k Ω	-

In the 1T-1R configuration, the transistor controls the amount of current flowing through the cell according to its gate voltage bias. The clamping current allowed by the select transistor is called the compliance current and is referred to as I_{CC} in Fig. 1b. I_{CC} controls the LRS resistance value in the SET state as well as the maximal RST current. Table I presents the different voltage levels used during the different operating stages and the resulting nominal resistance values. Note that the FMG step, achieved once in the device life is a voltage-induced resistance switching from an initial virgin state with a very high resistance R_{FMG} to a conductive state and that voltages higher than V_{SET} and V_{RST} (> 1.2 V) are typically needed to reach the FMG threshold V_{FMG} . Based on the memory cell hysteresis presented in Fig. 1b, four critical reliability parameters can be considered: V_{SET} , V_{RST} , R_{HRS} and R_{LRS} . From a design point of view, any variation of these parameters can lead to reliability issues as V_{SET} and V_{RST} are the programming thresholds and R_{HRS}/R_{LRS} ratio guarantees the memory operation.

Although OxRAM-based devices have shown encouraging properties, challenges remain, among which device variability (or reproducibility) is the main one [15]. Indeed, the variability from cycle to cycle (C2C) and from device to device (D2D) can be very large, impacting directly the memory cell HRS/LRS resistance ratio as well as V_{SET}/V_{RST} switching parameters. RRAM variability is highlighted in Fig. 1b with gray I-V curves superimposed over the initial bold blue curve. From a physical point of view, when a voltage V_{Cell} is applied across the RRAM cell (i.e., between the TE and BE electrodes), depending upon the voltage polarity, one or more Conductive Filaments (CFs) made out of oxygen vacancies are either formed or ruptured. The variations of the CFs shape and size is believed to be the

root cause of variability [13]. Variability also affects the switching time. For this aspect, it has been demonstrated that switching time variability can severely degrade speed and energy consumption [16].

B. RRAM Test Structure Architecture

The proposed RRAM test structure is based on a simple array consisting of a not addressable RRAM cells with parallel connection of all the memory elements. In Fig. 2a, the test structure architecture is presented for a 16 \times 16 1T-1R

array (256 cells). Only three external nodes are needed to use the structure: WL, BL and SL. WL node is used to access the gates of all the select transistors of the memory cells in order to clamp the current flowing through each cell. BL and SL nodes are used to respectively SET and RST the whole memory array in a single shot for a given compliance current. The compact size of the structure allows an easy integration in the scribe lines.

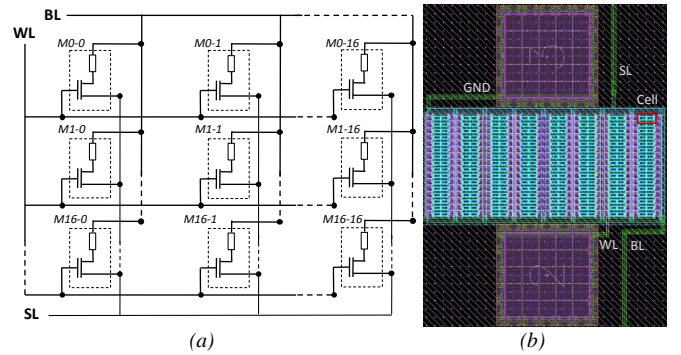


Fig. 2. (a) RRAM test structure architecture and (b) corresponding layout.

The measurement methodology is very simple. From the transfer characteristic measured under the select transistor clamping bias (V_{WL}), the test structure allows a fast evaluation of the R_{LRS} and R_{HRS} mean values. Also, it is possible to obtain accurate information on the RRAM switching parameters. More specifically, accurate information on V_{SET} and V_{RST} parameters can be obtained. If the V_{SET} parameter is considered, a simplest estimation of the RRAM SET threshold distributions can be extracted assuming a step-like current voltage characteristic for each RRAM cell, consequence of the select transistor clamping. Indeed, the clamping effect of the select transistor acts on every cell when the voltage across the structure increases during SET. During the measurement, as the voltage V_{BL} increases (SL node being grounded), the current I_{BL} in the structure is given by the sum of the N elementary contributions of the elementary cell currents I_{cell} in the array (1). I_{cell} reaches its maximum value I_{CC} when BL bias reaches the V_{SET} threshold of each elementary cell. This approach assumes that the cells turn on suddenly to the maximum clamping current in the case of V_{SET} distribution extraction which is a reasonable approximation regarding the literature [17] and Fig 1b. Based on this approximation, the global current derivative (i.e., transconductance) directly gives V_{SET} distribution (2). It is also possible to demonstrate that the array current is given by the convolution of a reference cell current I_{cell} with the V_{RST} distribution in the array [9].

$$I_{BL}(V_{WL}) = \sum_{i=1}^{i=N} I_{Celli}(V_{WL}) \quad (1)$$

$$G_{mSET} = \frac{\delta I_{BL}}{\delta V_{BL}} \quad (2)$$

Regarding V_{RST} parameter extraction, the SL voltage increases (BL node being grounded). During RST, the amplitude of cell current drops gradually after V_{RST} threshold is reached (see Fig. 1b). In contrast to the SET operation, no abrupt change of the current is observed and the final R_{HRS} value depends on the maximal amplitude of the SL voltage [17]. Hence, V_{RST} parameter distribution extraction is not relevant in this case. However, as the test structure acts as a smoothing function (i.e., 256 cumulative RST currents are considered), the RST process instability is mitigated, allowing an accurate extraction of V_{RST} value. This last point will be developed in the next section. It is worth noticing that in the literature V_{RST} parameter is extracted when the RST current reaches its absolute maximal value [18].

III. EXPERIMENTAL RESULTS

A. Experimental setup

The experimental setup is based on a Keysight B1500 semiconductor parameter analyzer [19]. The studied structure presented in section II.B is embedded in an 8-inch wafer, connected to the B1500 through a probe card. The probe card connects Source/Measure Units (SMUs) to the test structure during FMG, RST, SET and READ operations. All the experiments are performed using Python programs, controlling the equipment. RRAM electrical parameters are extracted based on the test chip I-V hysteresis transfer function. The extraction of V_{FMG} , V_{SET} , V_{RST} , R_{FMG} , R_{HRS} and R_{LRS} values is achieved using a 1ms DC staircase voltage sweep with a 0.02 V step: as the applied voltage increases step by step across the test structure, the current I_{BL} flowing through the structure is measured. The variability related to the switching parameters is also extracted based on the I-V curves analysis according to (1) and (2).

B. FMG operation

During FMG, the compliance current I_{CC} is set to 100 μ A for each cell resulting in a maximal clamping current of 25.6 mA as shown in Fig. 4a. The pre-forming resistance R_{HRS} is equal to 119 k Ω . This value includes the contributions of 256 cells arranged in parallel. Hence, the average cell pre-forming resistance value is evaluated to 30.4 M Ω . Note that this high resistance is usually difficult to measure for an isolated cell as it is close to most of test setup limits used in the literature [20]. After being formed, the test structure resistance R_{LRS} is equal to 35.2 Ω , which represents an equivalent cell resistance of 9 k Ω . Fig. 4b shows the current derivative versus the programming voltage during the FMG process in order to extract the switching voltage distribution. As the programming signal value increases, memory cells are formed gradually (i.e., abrupt current change up to 100 μ A), allowing the switched cells to be counted. The forming process starts from 1.2 V and ends at 1.55 V, resulting in a forming window of 0.35 V. Parameters extracted from Fig 4 are summarized in Table II.

From a design point of view, the FMG threshold voltage dispersion obliges to use high programming voltages or long programming pulses [18] to switch all the RRAM cells. Moreover, a compliance I_{CC} current strictly controlled for each cell is mandatory and needs to be high enough to reach an LRS resistance around 10 k Ω . Note that it can be detrimental if a too low or too large I_{CC} is used. In the first case, the cells could be stuck-at HRS. In the latter case, some fast formed cells could be stuck-at LRS, and when the following RST operation is performed, the fast formed cells would not be able to reach the HRS state.

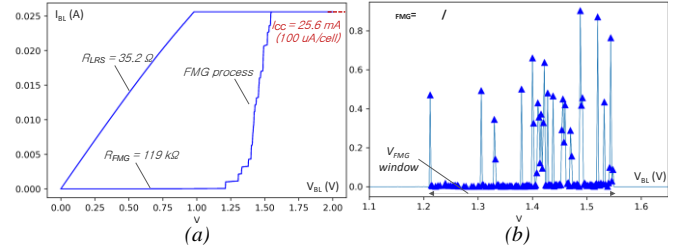


Fig. 4. (a) I-V hysteresis and (b) current derivative during the test structure FMG process.

TABLE II. FMG ELECTRICAL PARAMETERS

	STATE	Cell
R_{FMG}	119 k Ω	30.4 M Ω
R_{LRS}	35.2 Ω	9 k Ω
V_{FMG} window	0.35V	-

C. RST/SET operation

During RST/SET operations, the compliance current is set to 50 μ A for each cell, resulting in a maximal clamping current of 12.8 mA as shown in Fig. 5a. Before SET, the test structure resistance is equal to 918 Ω giving an average cell resistance value of 235 k Ω . After SET, the resistance is equal to 60 Ω , which represents an equivalent cell resistance of 15.3 k Ω . Fig. 5b shows the current derivative versus the programming voltage during the SET process. The SET process starts at 0.38 V and ends at 0.85 V, resulting in a large SET programming window of 0.47 V. Regarding V_{RST} parameter, its extraction is simplified due to the smoothing capability of the test structure (i.e., RST instability mitigation). V_{RST} value is evaluated to -0.70 V. Parameters extracted from Fig 5 are summarized in Table III.

From a design point of view, Table II results indicate that the maximal SET voltage required to set 100% of the cells is 0.85 V. Moreover, the read voltage should not exceed 0.38 V to not disturb the cells (i.e., unwanted SET operation). Alternatively, and according to the switching variability captured by the test chip and the targeted application, peripheral or assist circuits can be required to mitigate the chip-level SET voltage variability in order to maximize the technology yield.

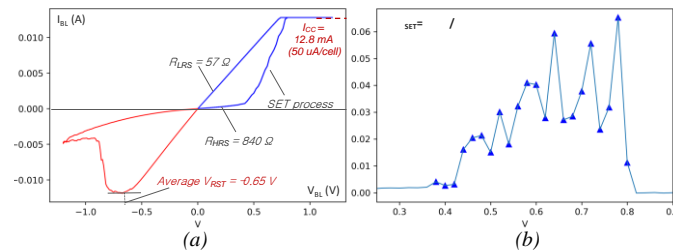


Fig. 5. (a) I-V hysteresis after RST/SET operations and (b) current derivative during the SET process.

TABLE III. SET/RST ELECTRICAL PARAMETERS

	STATE	Cell
R_{HRS}	918 Ω	235 k Ω
R_{LRS}	60 Ω	15.3 k Ω
V_{RST} Mean	-0.70 V	-
V_{SET} window	0.47 V	-

D. Test structure variability

The stability of the test structure electrical parameters is evaluated after 100 RST/SET cycles. Fig. 6a presents the resulting I-V transfer characteristics and Fig. 6b presents the current derivatives versus the programming voltage during the SET process.

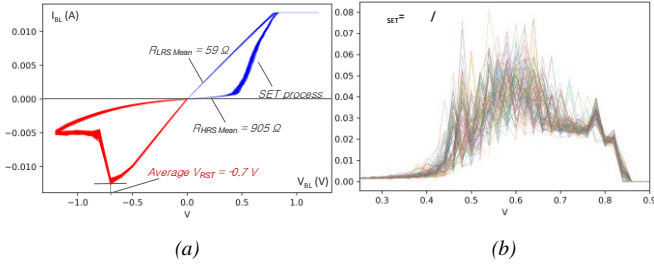


Fig. 6. (a) I-V hysteresis and (b) corresponding current derivatives during SET after 1000 RST/SET cycles.

Based on Fig. 6a, the average R_{LRS} is evaluated to 59 Ω and the average R_{HRS} to 905 Ω (average based on 100 I-V curves). These values are close to the ones extracted from a single transfer function (see Table III), which demonstrates the stability of the measurements performed using the test structure. The SET threshold variability obtained after 100 RST/SET cycles is included in the range [0.32 V, 0.85 V] with a V_{SET} window of 0.53 V. The latter is larger compared to the V_{SET} window obtained from the single transfer characteristic of Fig. 5a (0.47 V). This value encourages the use of assist circuits to contain the V_{SET} variability at the chip level. The smoothing function of the test structure is also validated, especially when the RST operation is concerned. An accurate extraction of V_{RST} is possible, which average value is evaluated to -0.70 V.

IV. DISCUSSION

The proposed test structure allows to get a first glance impression of the array switching kinetics between HRS and LRS and the HRS/LRS resistance mean values. These parameters can be evaluated in all operating programming conditions (FMG/RST/SET). To be confidently used for electrical parameter tracking, the test structure has to capture most of the important markers of RRAM technology. In this section, a peculiar attention is paid to the dependence of the resistance in LRS state against the maximum current allowed during the SET operations. As reported in previous works, the resistance in LRS state strongly depends on the maximum current I_{CC} allowed during the prior SET operation [21]. Fig. 7a shows the evolution of the LRS slope versus the compliance current. Table IV summarizes the different resistance levels obtained for different I_{CC} currents ranging from 10 to 50 μ A.

This modulation of the RRAM resistance is an important feature which needs to be verified experimentally. Indeed, integrating non-volatile, analogue weight storage on-chip, in

close proximity to CMOS-based neuronal circuits is essential for future large-scale energy-efficient neural networks that are trained online to respond to changing input data instantly like the human brain [6]. In addition to being able to check the multi-level capability of the RRAM technology, the test structure I-V characteristic also allows an easy analysis of the hysteresis due to its averaging capability (i.e., mitigation of brutal current/voltage variations due to its “smoothing effect”). This effect is clearly visible when considering Fig. 7b where the I-V curves of 50 isolated cells are plotted in the same graph (D2D variability), without setting any compliance current. As the total current measured at the external nodes of each isolated cell is 256 times lower compared to the STATE test structure current, variability is much more pronounced, complicating the analysis of the memory cells electrical parameters.

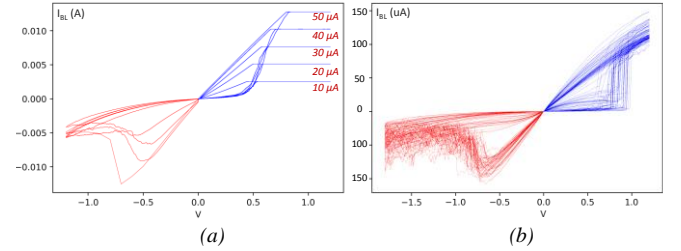


Fig. 7. (a) I-V test structure hysteresis for different compliance currents ranging from 10 μ A to 50 μ A (b) isolated RRAM cells variability.

TABLE IV. R_{LRS} VERSUS I_{CC}

I_{CC}	50 μ A	40 μ A	30 μ A	20 μ A	10 μ A
R_{LRS} State	61 Ω	69 Ω	84.5 Ω	117.4 Ω	221 Ω
R_{LRS} cell	15.6 k Ω	17.6 k Ω	21.6 k Ω	30 k Ω	56 k Ω

An interesting use case of the proposed test chip is related to marginal cells detection. Indeed, isolated cells or cells populations with electrical parameters far from nominal values can be easily detected. For instance, a memory cell with a low resistance will dominate the HRS resistance after a RST operation. Alternatively, the proposed characterization methodology can be used as a key enabler for RRAM models calibration. Model calibration can leverage on the parameters extracted from the proposed test chip instead of isolated cells characterized by an important variability [22]. Moreover, variability, including the switching variability, which is included in only a few compact models available in the literature [23-24], can be more accurately analyzed based on our test structure. Furthermore, beyond Oxide-based RRAM technology, the proposed test structure can be applied to other resistive memory technologies such as PCM or MRAM whose operation principle is based on resistive switching.

V. CONCLUSION

Intrinsic RRAM dispersion is a roadblock for industrialization of the technology, especially when high memory densities are required. In this context, a compact test structure combined with a smart characterization procedure is developed in order to tackle the RRAM variability issue. Based on a single I-V curve, the resistance margin between LRS and HRS, as well the multi-level capability of the technology can be quickly evaluated.

Moreover, the switching parameter dispersion of the technology can be captured based on a single measurement. Alternatively, marginal cell populations with resistance or switching parameter values far from nominal values can be detected.

ACKNOWLEDGMENT

The authors wish to acknowledge the support from the CEA- Leti (“Commissariat à l’énergie atomique-Laboratoire d’électronique et de technologie de l’information”). CEA-Leti provided the technology access as part of the Memory Advanced Demonstrators project (MAD200).

REFERENCES

- [1] Yu, Shimeng, and Pai-Yu Chen, “Emerging memory technologies: Recent trends and prospects,” *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 43-56, 2016.
- [2] J. M. Portal et al., “Design and simulation of a 128 kb embedded nonvolatile memory based on a hybrid RRAM (HfO₂)/28 nm FDSOI CMOS technology,” *IEEE Transactions on Nanotechnology*, 16(4), 677-686, 2017.
- [3] H. Aziza et al., “True Random Number Generator Integration in a Resistive RAM Memory Array Using Input Current Limitation,” in *IEEE Transactions on Nanotechnology*, vol. 19, pp. 214-222, 2020.
- [4] C. S. Chen et al., “A Compact Test Structure for Characterizing Transistor Variability Beyond 3 sigma,” in *IEEE Transactions on Semiconductor Manufacturing*, vol. 28, no. 3, pp. 329-336, 2015.
- [5] Y. Joly et al., “Impact of hump effect on MOSFET mismatch in the sub-threshold area for low power analog applications,” In 2010 10th IEEE International Conference on Solid-State and Integrated Circuit Technology, pp. 1817-1819, 2010.
- [6] H. Aziza, M. Moreau, A. Perez, A. Virazel and P. Girard, “A Capacitor-Less CMOS Neuron Circuit for Neuromemristive Networks,” 2019 IEEE International New Circuits and Systems Conference, pp. 1-4, 2019.
- [7] S. Yu et al., “Stochastic learning in oxide binary synaptic device for neuromorphic computing”, *Frontiers Neurosci.*, vol. 7, pp. 186, 2013.
- [8] H. Aziza et al., “ReRAM ON/OFF resistance ratio degradation due to line resistance combined with device variability in 28nm FDSOI technology,” Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, 2017.
- [9] F. Pio et al., “Select transistor modulated cell array structure test for EEPROM reliability”, *Microelectronic Test Structures, Proceedings of International Conference on*, pp. 217-222, 2000.
- [10] S. Kannan et al, “Modeling, Detection, and Diagnosis of Faults in Multilevel Memristor Memories,” in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 5, pp. 822-834, 2015.
- [11] H. Aziza et al, “Bipolar OxRRAM memory array reliability evaluation based on fault injection,” *IEEE 6th International Design and Test Workshop (IDT)*, pp. 78-81, 2011.
- [12] M. Fieback et al., “Device-Aware Test: A New Test Approach Towards DPPB Level,” *IEEE International Test Conference (ITC)*, pp. 1-10, 2019.
- [13] D. Ielmini, “Resistive switching memories based on metal oxides: mechanisms, reliability and scaling,” *Semiconductor Science and Technology*, vol. 31, no. 6, pp. 1-25, 2016.
- [14] A. Grossi et al., “Fundamental variability limits of filament-based RRAM,” *IEEE International Electron Devices Meeting (IEDM)*, 2016.
- [15] H. Aziza et al., “Evaluation of OxRAM cell variability impact on memory performances through electrical simulations”, *Non-Volatile Memory Technology Symposium Proceeding*, 2011.
- [16] H. Aziza et al., “An Energy-Efficient Current-Controlled Write and Read Scheme for Resistive RAMs (RRAMs),” in *IEEE Access*, vol. 8, pp. 137263-137274, 2020.
- [17] S. Yu, Ximeng Guan and H. - P. Wong, “On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, monte carlo simulation, and experimental characterization,” *International Electron Devices Meeting*, 2011, pp. 17.3.1-17.3.4., 2011.
- [18] A. Fantini et al., “Intrinsic switching variability in HfO₂ RRAM,” 2013 5th IEEE International Memory Workshop. IEEE, 2013.
- [19] V. Della Marca et al., “Quantitative correlation between Flash and equivalent transistor for endurance electrical parameters extraction,” *Microelectronics Reliability*, vol. 88-90, p.159-163, 2018.
- [20] A. Grossi et al., “Experimental Investigation of 4-kb RRAM Arrays Programming Conditions Suitable for TCAM,” in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 12, pp. 2599-2607, 2018.
- [21] H. Akinaga and H. Shima, “Resistive Random Access Memory (ReRAM) based on metal oxides,” *Proc. IEEE*, vol. 98, no. 12, pp. 2237–2251, 2010.
- [22] H. Bazzi et al., “Performances and Stability Analysis of a Novel 8T1R Non-Volatile SRAM (NVSRAM) versus Variability,” *J Electron Test* (2021).
- [23] B. Hajri et al., “RRAM Device Models: A Comparative Analysis With Experimental Validation,” in *IEEE Access*, vol. 7, pp. 168963-168980, 2019.
- [24] B. Hajri et al., “Oxide-based RRAM models for circuit designers: A comparative analysis,” in *IEEE International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS)*, pp. 1-6, 2017.