EEPROM endurance degradation at different temperatures: State of the art TCAD simulation

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***Abstract*— Electrically Erasable Programmable Read Only Memory (EEPROM) is a widely used memory device, nowadays implemented in submicron technology nodes. In this paper we show how the well-known trapping power law found in the literature can be retrieved by combining well calibrated state of the art Technology Computer Aided-Design (TCAD) simulations with a compact model for tunnel oxide degradation during EEPROM cycling. We pinpoint how this approach can be used to predictively assess the programming window closure and consequently, considerably reduce the time-consuming cycling test procedure. Finally, we show how this methodology can cover a wide range of temperatures, making it very attractive for high demanding applications such as automotive.**

Keywords—NVM, EEPROM, endurance degradation, TCAD simulation, programming window, bulk oxide trapping

I. Introduction

Although floating gate based Electrically Erasable Programmable Read Only Memory (EEPROM) was developed in the late '70s [1,2], this architecture is still widely used in microelectronics circuits thanks to its high reliability, the granularity of basics operations and low operating power requirement. STMicroelectronics is the world #1 in serial EEPROMs designing and manufacturing. It has recently announced a 110 nm-CMOS technology node based 4Mbit EEPROM with 40 years data retention [3]. Combining electrical characterizations with a realistic process flow simulation of this EEPROM device, this paper discusses the defects generated during endurance degradation, leading to programming window closure, and the way to take them into account in simulations.

In the literature, these defects have been identified as negative charges trapped within bulk oxide and their generation has been inferred using compact models [4-6]. However, a better simulation of bulk oxide charge trapping and its impact on state-of-the-art EEPROM devices, calls for a TCAD based approach. For instance, the authors in [7] correctly reproduced both the increase in the drain current consumption and the decrease in channel hot electron (CHE) injection in 90nm Flash memory after degradation, by introducing traps at the Si/SiO_2 interface. This paper follows a similar approach for EEPROM programming operations, in which only Fowler-Nordheim tunneling mechanism is involved.

In Section II, we describe the EEPROM simulated structure and provide a methodology for the calibration, leading up to a predicted programming window that is in good agreement with experiments. Section III focusses on endurance i.e., the number of write/erase cycles that can be endured before both programmed states are no longer distinguishable. By inserting negative trapped charge in the tunnel bulk oxide, the experimental programming window closure is reproduced. In support of such approach, we show that the total trapped charge density follows the commonly used Power Law [6]. As a practical application, we suggest using this predictive TCAD model to drastically reduce the experimental cycling test time. Finally, in Section IV we show how to extend this model to include high temperature impact on programming window closure.

II. EEPROM TCAD simulation and calibration

This study was carried out using Sentaurus™ Suite by SYNOPSYS®, for both process and electrical simulations [8].

A. Process and Electrical Calibration

Process simulation was based on a 110nm CMOS technology node. The obtained EEPROM cell structure is shown in Fig.1 and consists of Sense and Select transistors.

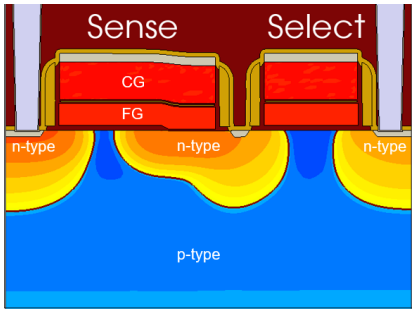

Figure 1: Simulated EEPROM structure.

In the Select transistor, the two polysilicon layers are electrically shorted (not shown in the picture) and the bottom layer is isolated from the bulk by a relatively thick thermal grown silicon oxide. In the Sense transistor, bottom polysilicon layer (the "floating gate", FG) is used for electric charge storage and therefore is electrically insulated from both the top polysilicon layer (the "control gate", CG) and silicon substrate. A dedicated thermally grown thin silicon oxide ("tunnel oxide") located in the Sense transistor is used for EEPROM programming by Fowler-Nordheim mechanism.

Calibration procedure starts with capacitance-voltage (C-V) electrical simulation of 1D plate capacitors. Process simulated doping profiles and oxide physical parameters for the MOS capacitors are fine-tuned to yield C-V curves matching the experimental ones (Fig.2). In Fig.2 a), The mismatch is observed for thin oxide and at high applied voltage (-7 V < Vg < - 5 V). In this simulation we have used very simple models for since we were mainly interested in oxide thickness (in accumulation region) and substrate doping (at depletion/inversion). A better agreement may be obtained with more advanced models. In Fig.2 b), the experimental data are perfectly reproduced by the TCAD simulation.

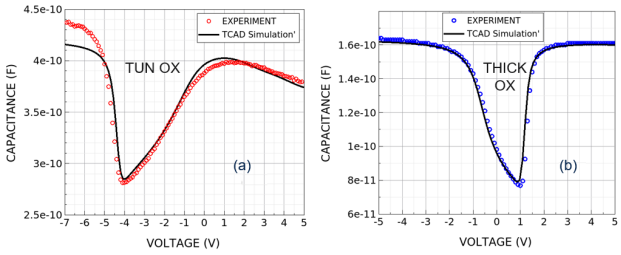

Figure 2: Capacitance vs Gate Voltage for (a) tunnel oxide (n-type substrate) and (b) thick oxide (p-type substrate).

Moving to 2D calibration, Fig.3 shows the simulated I-V characteristics of the EEPROM structure when a voltage ramp is applied simultaneously to the Control and Floating Gates of the Sense transistor (equivalent transistor), with the Select transistor turned on by applying suitable gate and drain voltages. A dedicated test structure, in which the Control and Floating Gates are shorted, is used for the experiments. Again, a good agreement is found between TCAD and experiments suggesting a correct simulation of Sense 2D doping profiles. The mismatch between TCAD and experimental data for Vgs < -0.25 V is due to a measurement site with an unusually high leakage current (an outlier). Since the typical currents we will be interested in are about 1 µA (for constant current threshold voltage definition) such difference is irrelevant.

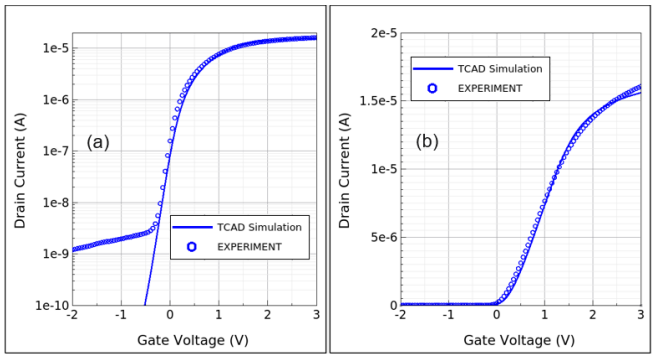

Figure 3: Drain current vs Gate voltage on equivalent transistor (both gates are shorted). (a) Log scale and (b) Lin scale.

As mentioned in the introduction, the physical mechanism taking place during write/erase operations in the EEPROM is Fowler-Nordheim (FN) tunneling [9]. In Sentaurus™ Device FN current density J_{FN} is modeled as:

$$J_{FN} = AF^2 \exp\left(-{}^{B}/_{F}\right) \quad (1)$$

where F is the insulator electric field at the interface and A, B are physical related parameters, but can be independently set to match experimental data in write and erase operations [10]. In this article, we use a slightly more general model developed by Schenk [11] which considers image force effect and the effective mass of electron (or hole) in the insulator. If necessary, these parameters can be fine-tuned to match experimental data [10]. In Fig.4 we compared experimental and simulated tunneling currents as measured on a large plate capacitor (Fig. 4(a)) and a 10k equivalent transistor Cell Array Stress Test (CAST) structure [12] (Fig. 4(b)) with an area of 100 000 µm² and ~3000 µm², respectively. The CAST structure is made of many memory cells connected in parallel. When gates are shorted, it is typically used to study Fowler-Nordheim tunneling currents [13]. Concerning the CAST simulation, since this structure is periodic, we only simulated a single cell and applied a multiplying factor corresponding to the total area.

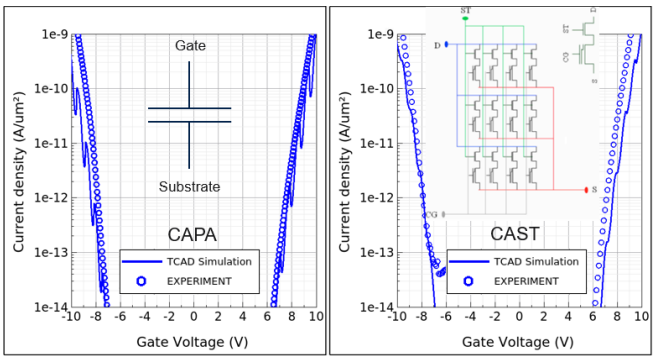

Figure 4: Gate Current density vs Gate voltage for (a) MOS capacitor with tunnel oxide (n-type substrate) and (b) 10k equivalent transistor CAST structure.

A good agreement is obtained for both positive and negative applied gate voltages by setting the electron effective mass in the oxide to half its value for the free electron. The oscillations observed on simulated gate current curves are due to interference in the FN regime as already explained in the literature [11].

B. EEPROM dynamic operations simulation at 25°C

The I-V curves for the written and erased states are shown in Fig. 5. Here, we have adopted the commonly used EEPROM naming convention in which low state is labeled “written”, whereas high state is called “erased” (in contrast with Flash memory, for which the names are reversed) [14].

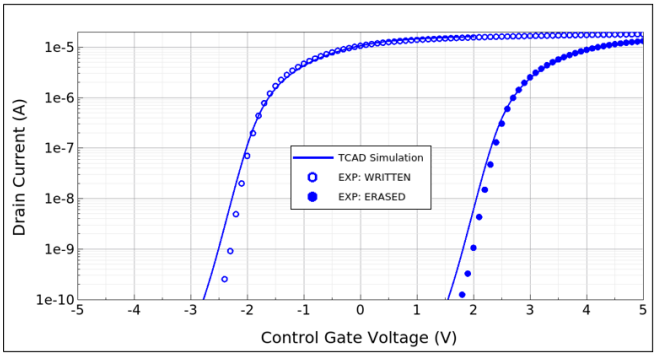

Figure 5: EEPROM programming window at 25°C.

The good agreement between simulated and experimental curves was obtained by fine-tuning the floating gate capacitive coupling ratio, a mandatory step for a 2D simulated device.

In Fig. 6 we show the programming dynamics of the cell for erase and write operations. This threshold voltage kinetics are obtained by successively applying an erasing or writing short pulse and measuring the corresponding threshold voltage by a read operation. The simulated curves were obtained following exactly the same protocol and using time-dependent features of the simulating tool. Moreover, assuming oxide integrity (virgin state) no defects whatsoever were included in the simulation.

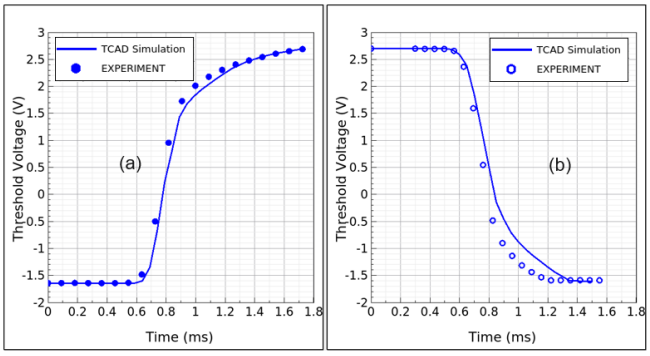

Figure 6: (a) Erasing and (b) Writing kinetics of a virgin cell at 25°C

Threshold voltage V_T was extracted at constant drain current of 1 µA, drain voltage at 0.8 V and Select transistor gate voltage at 3 V. A very good agreement, especially in erase mode, is obtained between experiments and TCAD simulations.

III. Endurance Degradation and Defect Extraction at 25°C

A. EEPROM endurance degradation defects

We briefly review some of the physical phenomena that contribute to oxide degradation and that have an impact on EEPROM device reliability. Firstly, the breaking of Si bonds at Si/SiO_2 interface during electrical stress leads to the generation of interface traps which in turn shift the device threshold voltage and reduce its transconductance due to Coulomb scattering [15]. Secondly, the generation of bulk oxide traps which results from Fowler-Nordheim stress favors charge trapping and induces leakage current (SILC) [16]. Positive charges trapped in bulk oxide by anode holes injection [17] contribute to data retention efficiency loss, slight threshold voltage negative shift at low injected charge density and, possibly, to oxide breakdown (this last assertion is still controversial) [18-19]. On the other hand, negative charges trapped in bulk oxide reduce the efficiency of tunneling current injection and are widely recognized as the main contributor to programming window closure [4-6]. In addition to reduce the programming window during cycling, these charges also contribute to a positive threshold voltage shift. Therefore, we often observe a larger shift in absolute value on V_T-write than on V_T-erase. Assuming no re-emission of trapped electrons, the electron capture process in thermal oxides can be described by first-order kinetics as [20]:

$$\frac{dn_{tp}(t)}{dt} = \frac{J(t)}{q_e}\,\sigma_p\left(N_0 - n_{tp}(t)\right) \qquad (2)$$

where n_{tp} is the volumetric trapped electron density, $J(t)$ the injected current density, N_0 the trap density (which can be considered constant in first approximation), σ_p the trap capture cross section and q_e the elementary charge. The solution of equation (2) can be expressed as [6]:

$$n_{tp}(t) = -q_e N_0\left[1 - \exp\left(\frac{-Q_{inj}(t)\,.\,\sigma_p}{q}\right)\right] \qquad (3)$$

and the trapped charge density can be expressed as:

$$Q_{ox} = \int_0^{T_{ox}} n_{tp}(x)\,dx \qquad (4)$$

where x is the distance from the $Poly/SiO_2$ interface and T_{ox} the oxide thickness. In the literature Q_{ox} and Q_{inj} have been correlated with a power law empirical equation [6]

$$Q_{ox} = \int_0^{T_{ox}} n_{tp}(x)\,dx \approx A.\,{Q_{inj}}^{v} \qquad (5)$$

where A and v are fitting parameters. Compact modelling usually assumes a uniform distribution of negative trapped charge within the oxide [5] or a charge centroid close to mid-oxide thickness [4-6] since injection processes involve both Si/SiO_2 (erase operation) and $PolySi/SiO_2$ (write operation) interfaces.

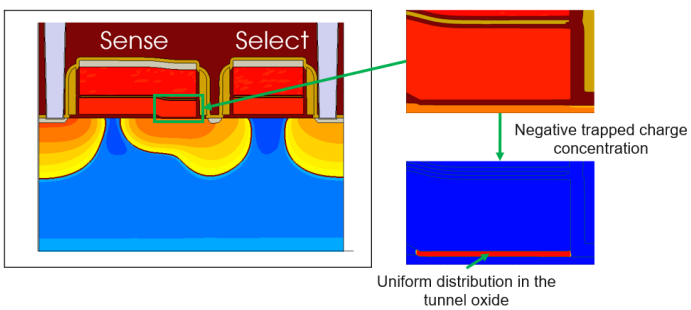

Figure 7: Uniform distribution of negative charges trapped in the tunnel oxide

In TCAD simulations, for simplicity's sake, we used a uniform tunnel oxide charge distribution (Fig.7). Other

spatial distributions (gaussian, exponential) could also be implemented.

B. *Extraction of negative trapped charges density Q_{ox} in tunnel oxide at 25°C*

Endurance measurement at 25°C up to 10M cycles is shown in Fig. 8. In the first 1k cycles, there is no significant change in the programming window. Then from 1k cycles to 10M cycles the threshold voltage shift of the erase state is 0.7 V, whereas the shift of the write state is 0.95 V. This is typically due to the electrostatic influence of negative trapped charges, as previously explained in Section III-A. The injection efficiency loss during erase and write operations is the main factor inducing threshold voltage shift [4]. Another significant contributor is the electrostatic influence of trapped negative charge during the read operation, leading to a positive threshold voltage shift for both erased and written states.

Since the programming window closure is not significatively modified before 1k cycles, our Q_{ox} determination starts beyond this threshold value. For each point from 1 k to 10M cycles of endurance test in Fig.8, the charge density Q_{ox} is set to correctly simulate the experimental programming window closure.

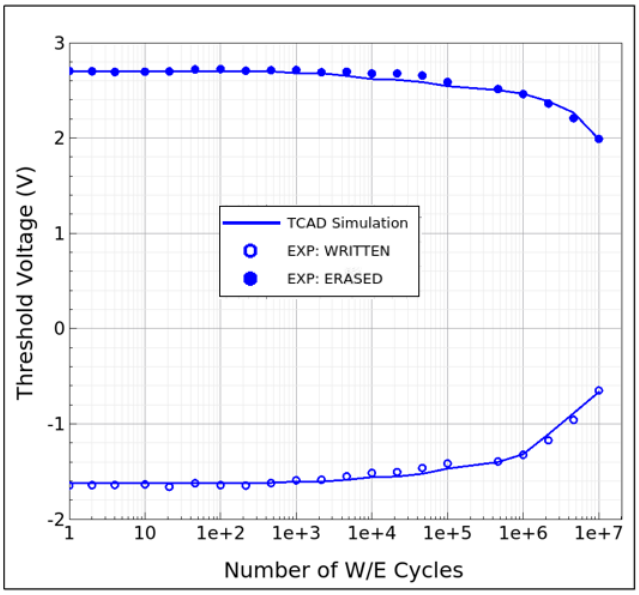

Figure 8: EEPROM cycling at 25°C.

In Fig. 9, the TCAD-simulated trapped charge density Q_{ox} is plotted versus the total injected charge density in the Floating Gate Q_{inj}. The injected charge Q_{inj} can be deduced from measurements using the formula:

$$Q_{inj}(n) = 2 * C_{ONO} * \sum_{k=0}^{k=n} \left(V_{TH_k} - V_{TL_k}\right) \qquad (6)$$

where C_{ONO} is the interpoly capacitance, n the number of cycles, V_{TH} and V_{TL} the threshold voltages of the erase and the write states.

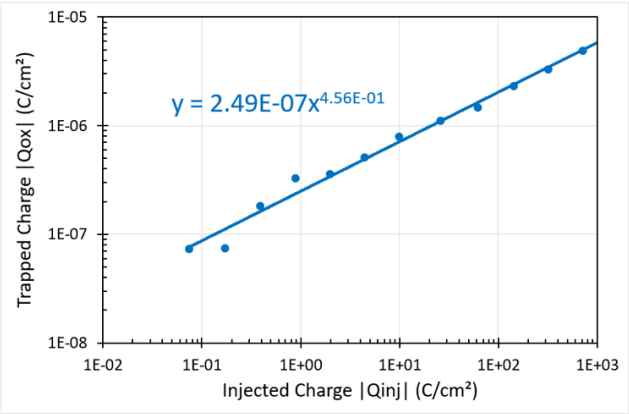

Figure 9: Oxide trapped charge density (simulated) vs Injected charge density (measurement); the curve follows the power law at 25°C (solid line).

Interestingly, the Q_{ox} - Q_{inj} curve follows an empiric power law and the parameters A, v are very close to the ones found in the literature [6,21], though slightly higher (v = 0.3-0.4). It is worth mentioning that previously published results were obtained for different test structures (planar capacitor [6] and CAST [21]) under constant current stress. In our case, the stress was generated by repeated high voltage pulses, which we believe are more degrading. Hence inducing a slightly higher v.

To sum it up, the methodology followed consisted in; (a) TCAD program calibration on plate capacitors and dummy cell, (b) Floating Gate Coupling factor tweaking on Erased et Written states, (c) dynamic characteristics benchmarking, (d) Q_{ox} setting for TCAD simulation of experimental cycling curves, (e) Q_{inj} computation using formula (6) on cycling data, and finally (f) Q_{ox}-Q_{inj} plotting and power law parameters extraction.

To further assess the relevance of our TCAD simulation, in Fig.10 we compare the experimental dynamic threshold voltage kinetics after 10M cycles to the simulated ones, that is after the device underwent significant degradation.

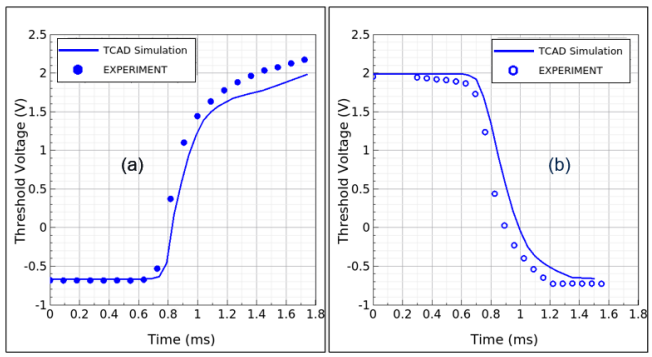

Figure 10: (a) Erasing and (b) Writing kinetics for a cell after 10M cycles at 25°C.

Even after 10M cycles and almost 2 V in programming window closure, simulated writing and erasing kinetics are close to the experimental measurement.

C. *Predictive simulation for endurance test time saving at 25°C*

This TCAD model can be used as a predictive tool, once the power law and the correponding parameters are obtained from a set of experimental data. To illustrate the method, three cycling datasets 1k to 10k cycles, 1k to 100k cycles, 1k to 1M cycles are selected and the corresponding *A, v* parameters are extracted. These will then be used to predict the programming window closure up to 10M cycles. In Fig.11 we plotted the $Q_{ox} - Q_{inj}$.

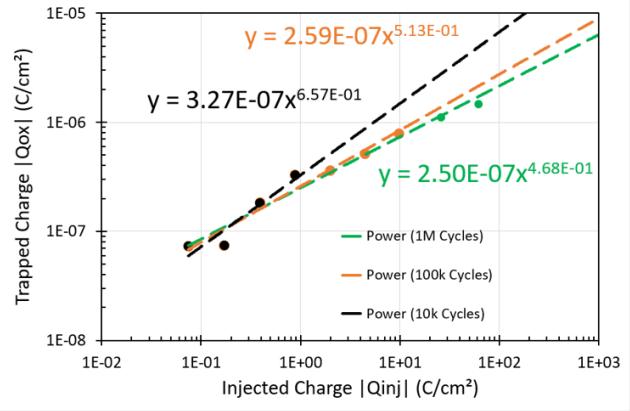

Figure 11: Power law with 3 different parameter sets determined from 1k to 10k cycles, 1k to 100k cycles and 1k to 1M cycles at 25°C.

We can readily see that *v* parameter is signifcantly different for the three considered cases. This will lead to an overestimation of the trapped charge for the 10k and 100k cycles datasets.

Indeed, in Fig.12 we can see three very different programming window closure simulation results. For the first dataset (1k to 10k Cycles - power law A=3.27e-7, v=0.657) overestimation of the oxide trapped charge leads to a premature window closure, a consequence of tunneling current decrease, followed by a simultaneous sharp increase in both Vth-erase and Vth-write due to an electrostatic effect.

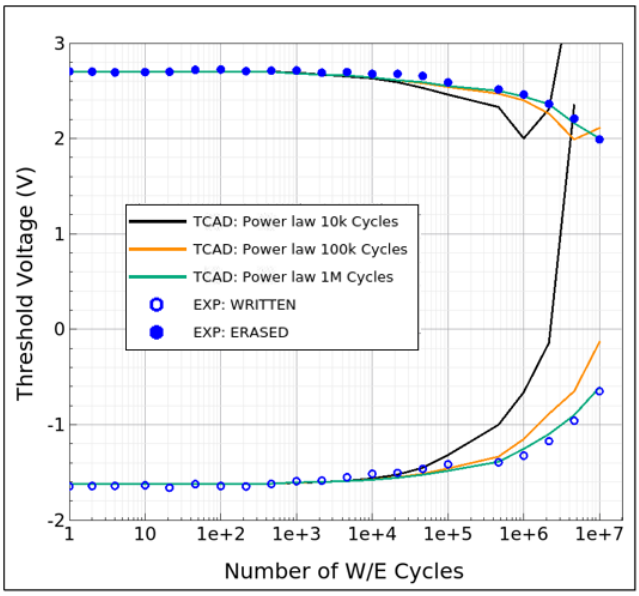

Figure 12: Programming window closing at 25°C with the 3 sets of trapped charge density

The second dataset (1k to 100k cycles - power law A=2.59e-7, v=0.513) predicts a faster programming window closure than observed. In fact, beyond 500k cycles simulation and experiments are appreciably different. The last dataset (1k to 1M cycles - power law A=2.50e-7, v=0.468) is remarkably predictive in both Vth-erase ans Vth-write up to 10M cycles, with less than 5% error. Using this simulated data instead of performing the 10M cycling experiment would reduce test time by a factor 10 and would made the equipement available for other use.

IV. High Temperature Simulation

It is well known that a temperature increase accelerates degradation mecanisms [22]. During endurance tests, for instance, the programming window closure and the number of cycles to breakdown are temperature dependent. In our experiments, endurance test was performed at 150°C to evaluate our model over a large temperature range and to meet the requirements for automotive applications.

A. Tunneling current temperature dependence

In the classical paper by Lenzlinger and Snow, tunnelling current increase with temperature was attributed to a decrease in the Al-SiO2 barrier height [9]. Others authors, AvRon et al. [23] using photoemission spectroscopy on MOS capacitors found that the Al-SiO2 barrier height lowering due to temperature increase was significatively lower than expected by previous models. Thus the tunneling current increase could not be explained by barrier height decrease only. A temperature increase would also change the carrier energy distribution in Silicon and Polysilicon which would rise the carriers quantity availabe for the tunneling process. The higher the doping concentration, the lower the influence of temperature on carrier distribution and then on the tunneling current [24]. As suggested in [23], oxide quality would also change the temperature dependence of the tunneling current. Different impureties such as alkali ions or interface traps with activation temperature dependence could also have an effect. Globally, the temperature influence on tunneling current has many sources and possible physical explanations. To keep a quite simple approach, we assumed that the tunneling current enhancement due to temperature increase is mainly caused by barrier height reduction, an assumption commonly made in the literature [25-27].

B. EEPROM dynamic operations simulation at 150°C

After a calibration step which consisted in reducing the Si-SiO2 barrier height from 3.02 eV (at 25°C) to 2.82 eV (at 150°C), a variation range close to the one found in the literature [9][27], we obtained a good agreement for the programming dynamics (Fig.13).

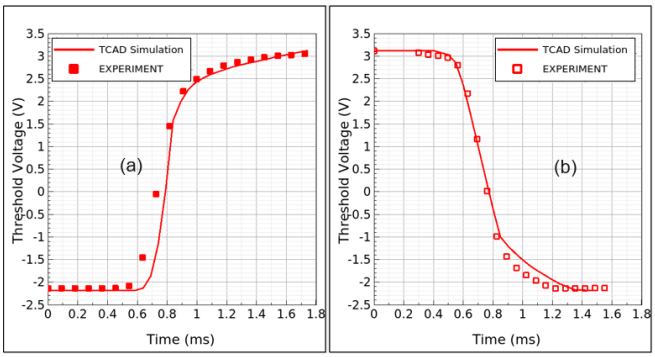

Figure 13: (a) Erasing and (b) Writing kinetics of a virgin cell at 150°C.

C. *Extraction of negative trapped charges density Q_{ox} in tunnel oxide at 150°C*

In Fig. 14, we show cycling test results at 150°C and 25°C. Initially, programming window is larger at higher temperature by approximatively 1 V. After 100k cycles programming window closure is faster at 150°C and oxide breakdown occurs around ~ 2M cycles. Following the method presented in section III.B, for each Write/Erase cycle, the density Q_{ox} is extracted to correctly reproduce the experimental behavior. At 150°C, beyond 1M cycles the sharp decrease in the programming window indicates severe degradation of oxide integrity eventually leading to its breakdown. Since such phenomena are not included in our TCAD model we were not able to corrrectly simulate experimental data.

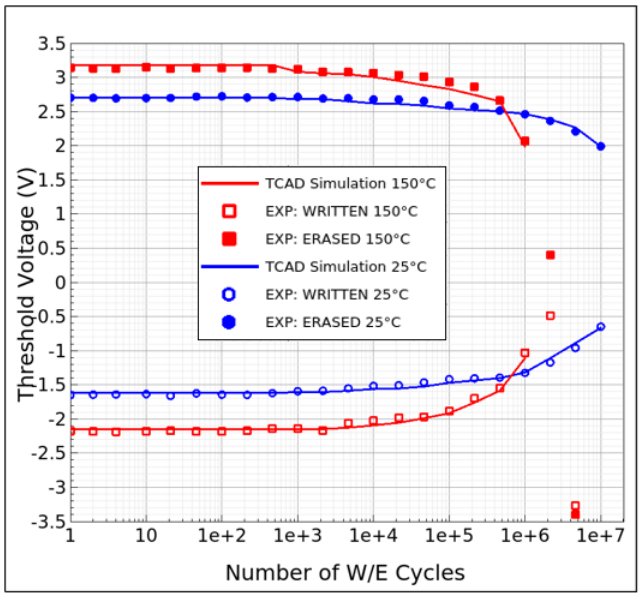

*Figure 14: EEPROM cycling at **25°C** and **150°C**.*

The power law obtained from cycling test at 150°C is shown in Fig.15 along with the one previously obtained at 25°C.

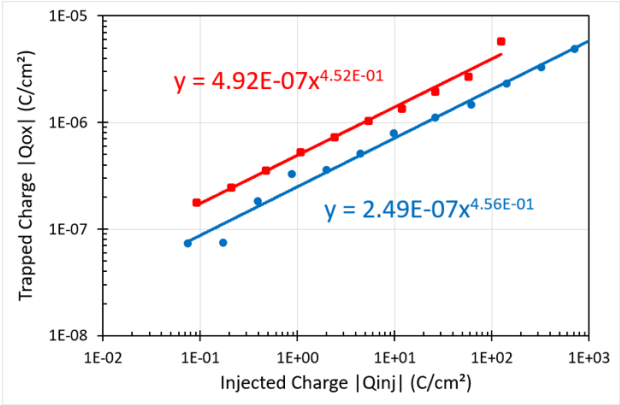

*Figure 15: Oxide trapped charge density (simulated) vs Injected charge density (measurement), at **25°C** and **150°C**.*

The two power laws exhibit linear behavior, in a log-log scale, with approximatively same slopes. Globally, more charge is trapped in the oxide at higher temperature, the curve at 150°C being shifted upward with respect to the one at 25°C. This is in agreement with the literature [28]. Furthermore, since the injection current increases with temperature, the combinations of these effects lead to a faster programming window closure at 150°C.

D. *Predictive simulation for efficient endurance test and time saving at 150°C*

Finally, the paper is concluded by the predictive attempt at 150°C presented in Fig.16. The parameter set determined from 1k cycles to 10k cycles leads to a good prediction up to 500k cycles. It is interesting to note that the model shows a good predictability at 10k cycles at 125°C, which was not observed at 25°C. This is a direct consequence of a temperature inducing higher negative charges trapping. Indeed, the faster a significative trapped charge concentration is generated, the less a cycle number is necessary to reproduce the programming window closure.
The mismatch after 500k cycles could be explained by the fact that the tunnel oxide is close to breakdown which induces additional physical phenomena not implemented in this study.

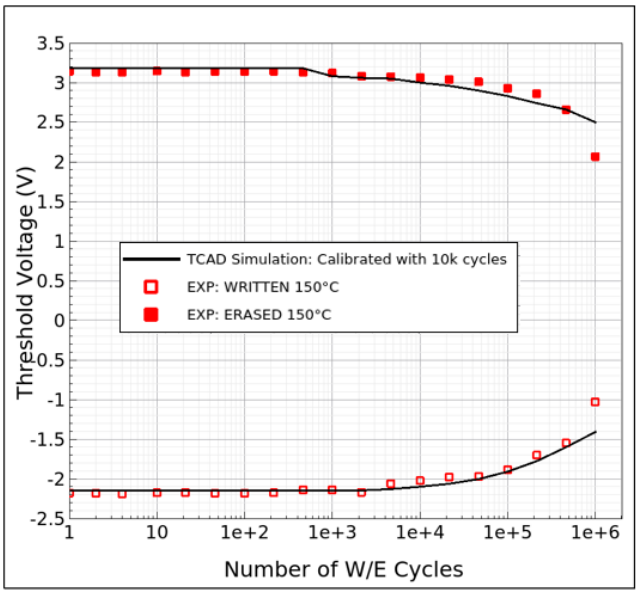

Figure 16: Programming window closure at 150°C with trapped charge density calibrated from 1k to 10k cycles.

V. Conclusion

We performed TCAD simulation of a state of the art 110 nm technology node EEPROM cell. Following a calibration methodology based on standard electrical characterizations, we obtained programming kinetics in good agreement with experiments. Using a novel approach combining injected charge density extraction and TCAD simulation of negative trapped charges in bulk oxide during cycling, we were able to retrieve a well-known trapping power law. This predictive simulation of the programming window closure could be used to reduce the time-consuming cycling test procedure. Finally, we showed how this approach can be extended in a temperature range typical of automotive applications. This approach is directly transposable to NAND Flash-EEPROM and possibly to NOR Flash-EEPROM, provided that Hot Carrier degradation mechanism are correctly included for the latter device. Other improvements of the model may include a non-uniform oxide charges distribution as well as 3D simulation.

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