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STATE: A Test Structure for Rapid and Reliable Prediction of Resistive RAM Endurance

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***Abstract*— Characterizing and quantifying the endurance of Resistive RAM devices is critical to assess their reliability for integration in electronic systems. This paper proposes a novel characterization methodology for rapid detection of RRAMs reliability issues during endurance tests. A test structure consisting of an array of non-addressable RRAM memory cells with parallel connection of all the memory elements is used for this purpose. The test structure fills the gap between isolated cells and circuit level endurance tests as it combines the test speed of an isolated cell while providing at the same time data from multiple devices. Endurance tests are conducted while monitoring RRAM electrical parameters of interest for each switching cycle. Experimental results show that most studies that claimed high endurance without capturing all switching cycles, or by considering an isolated cell, lead to an overestimation of the endurance. Finally, an endurance failures mitigation scheme based on RRAM current sensing in the RESET direction is presented to improve the endurance.**

Keywords*— *RRAM, OxRAM, Test structure, Endurance, Cycling, Reliability, Electrical parameters.

I. Introduction

Emerging technologies such as Resistive RAMs (RRAMs) are attracting considerable attention due to their tempting characteristics such as high scalability, CMOS compatibility and non-volatility [1]. Bipolar Oxide-based Resistive RAM (so-called OxRAM) is focusing strong interests as a candidate for densely packed cross-point 3D-arrays, high performance Storage Class Memory (SCM), as well as a new component able to unlock the full potential of disruptive computing architecture such as edge-Artificial Intelligence [2]. For any application, one of the most important properties of RRAMs is their cycling endurance, defined as the maximum number of programming cycles (one RESET (RST) transition followed by one SET transition) that the device can undergo before its electrical characteristics start to deviate, until failure [3]. Moreover, during cycling, the RRAM resistance can get unpredictably stuck at one resistance state for some time and suddenly recover the normal operation [4]. Therefore, characterizing the endurance of RRAM devices in an accurate manner is a strong requirement.

However, the state-of-the art regarding endurance tests suffers from several limitations. First, most of the publications that claimed high endurance (>10^6) are based on endurance plots considering very few cycles (in many cases even <50) [5]. Which means that RRAM electrical parameter extraction is performed considering less than 50 cycles out of 10^6 cycles. This approach is unreliable as the cycling endurance of RRAM devices requires measuring their electrical properties for each cycle. Otherwise, the incapacity of the RRAM to switch correctly for some cycles can be missed, which leads to an overestimation of the actual endurance. Secondly, most studies only consider one single device, masking the intrinsic variability of the technology [6][7]. Indeed, it is known that the standard qualification procedure for memory endurance in the industry requires statistical results from a sufficiently large memory array [8]. And, most of the time, an array-level analysis with many devices is typically not available in the early development stage, especially for emerging technologies. Even though large memory array circuits are available, systematic cycling induces important test time overheads (address-program-read operation for each memory word). Therefore, and for all the above-mentioned reasons, there is an urgent need for a smart monitoring technique able to track in a reliable manner the correct switching of the RRAM device over time.

In this work, a lightweight test structure, presented for the first time in [9], and referred to as STATE (StrucTure for rApid predicTion of RRAM Electrical parameter variability) is used to allow a rapid and reliable prediction of endurance failures. The proposed use case of the test structure allows the development of a full framework dedicated to cycling failures detection and analysis. To the authors' knowledge, this is the first work which presents an alternative to current RRAM cycling tests.

The main contributions of the paper are as follows:

- The STATE test structure is processed to monitor and speed up RRAM parameters extraction during cycling.
- As the test structure is made of devices connected in parallel, with only three external nodes, multiple devices are considered during a single measurement.
- Targeting a large number of cells, in a single shot, allows to detect more quickly one defective device among a whole population, making cycling tests faster.
- Fast execution of the endurance test allows to extract the RRAM electrical parameters for each cycle. This aspect is largely neglected in many studies related to endurance [5].

The remainder of the paper is organized as follows. Section II introduces the RRAM test structure. In section III, experimental endurance results are presented and discussed. In section IV, an endurance failure mitigation scheme is proposed. Finally, section V concludes the paper.

II. RRAM Test structure

A. RRAM Technology Background

Fig. 1a shows a basic 1T1R memory device where one MOS transistor (W = 0.8 µm and L = 0.5 µm) is connected in series with one RRAM cell. The RRAM resistive element, depicted in Fig. 1b, is integrated in the BEOL of a 130nm technology, between M4 and M5 layers [10]. The stack is deposited using Physical Vapor Deposition (PVD) where a 10nm Hafnium dioxide (HfO_2) layer is placed on the top of a TiN Bottom electrode (BE). A Ti/TiN bilayer stack is then deposited as a top electrode (TE) to form a capacitor-like structure. Fig. 1c shows a typical 1T1R I-V characteristic. Based on this I-V curve, the memory cell operation can be seen as follows: after an initial electro-Forming (FMG) step

[11], the memory element can be switched in a reversible manner between the Low Resistance State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T1R cell, i.e., V_{SET} to switch to LRS after a SET operation and V_{RST} to switch to HRS after an RST operation.

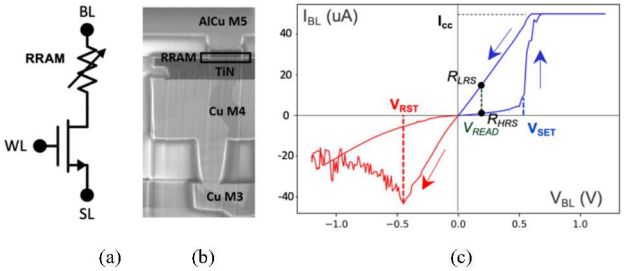

Fig. 1. (a) Symbol view of a 1T1R cell. (b) SEM cross section of the RRAM, integrated on top of Metal 4 [10]. (c) RRAM I-V characteristic.

The voltage levels used during the different operating stages are presented in Table I, along with the resulting nominal resistance values. Based on the memory cell hysteresis presented in Fig. 1c, four critical reliability parameters can be considered: V_{SET}, V_{RST}, R_{HRS} and R_{LRS}. From a design point of view, any variation of these parameters can lead to reliability issues. Note that R_{HRS} and R_{LRS} are extracted at V_{BL}=0.1 V during a READ operation, in the forward or SET direction (blue curve in Fig. 1c, with V_{BL}>0). Also, in the 1T1R configuration, the transistor controls the current level flowing through the cell according to its gate voltage bias. This clamping current allowed by the select transistor is called the compliance current and is referred to as I_{CC}.

TABLE I. STANDARD CELL OPERATING VOLTAGES

	FMG	RST	SET	READ
WL	2 V	2.5 V	2 V	2.5 V
BL	3.3 V	0 V	1.2 V	0.1 V
SL	0 V	1.2 V	0 V	0 V
$R_{LRS/HRS}$	10 kΩ	240 kΩ	15 kΩ	-

One of the most important challenges of RRAM technology is the control of the device variability (temporal and spatial) in both LRS and HRS states [12][13]. In fact, variations of R_{HRS}/R_{LRS} and V_{SET}/V_{RST} are so unpredictable that they have been employed as an entropy source in True Random Number Generators (TRNG) [14][15]. Indeed, variance from Cycle to Cycle (C2C) and from Device to Device (D2D) is very large, impacting directly the memory R_{HRS} and R_{LRS} resistances. This intrinsic drawback of the technology, combined with aging, has a straight impact on the RRAM technology reliability [5]. To assess the impact of variability on the HRS/LRS resistance ratio, an 8x8 (64 cells) elementary 1T1R array [14] is considered for measurements. A FMG operation is first applied to the memory array. Then, each memory cell is RST to extract R_{HRS}. After RST, cells are SET to extract R_{LRS}. The effect of variability (combining D2D and C2C) is highlighted in the cumulative probability plot presented in Fig. 2 obtained after 500 consecutive RST/SET cycles applied to the memory array (500x64 cells). A 0.1 V READ bias voltage is used to extract R_{LRS} and R_{HRS} distributions. Note that the HRS distribution spread is more pronounced compared to the LRS spread, which is a common feature of OxRAM technologies [16].

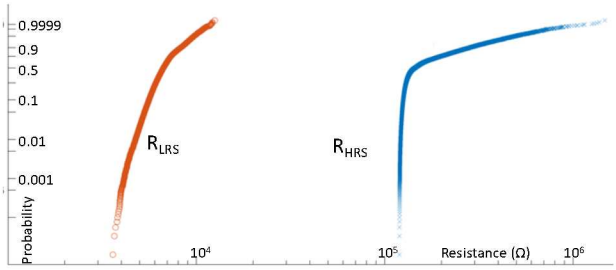

Fig. 2. HRS and LRS resistance distribution measurement results based on an OxRAM memory array fabricated in a 130 nm CMOS technology.

In addition to variability, over time, most of RRAM devices fail during cycling because of the degradation of their atomic structure, often associated with the formation of oxygen vacancies in the insulator for HfO_2-based devices [17]. It has been demonstrated in [6], for Ti/HfO_x/TiN devices, that the values of R_{HRS} and R_{LRS} experienced a progressive drift until the two states became indistinguishable. Findings from other studies have reported that the resistances of the device can also get erratically stuck in one state in some cycles and recover the normal functioning suddenly [4]. This unpredictable behavior clearly indicates that endurance tests must be conducted by checking that the device effectively switches in each cycle.

B. *RRAM Test Structure Architecture*

During the early phase of development, it is often difficult to obtain sufficient reliable data on RRAM memories. The process itself is not stabilized and fully functional devices are not yet available. At this stage, test structures can play an important diagnostic role in climbing the yield learning curve and in providing valuable reliability data [18][19]. The proposed RRAM test structure is based on a basic array consisting of not addressable RRAM cells with parallel connection of all the memory elements.

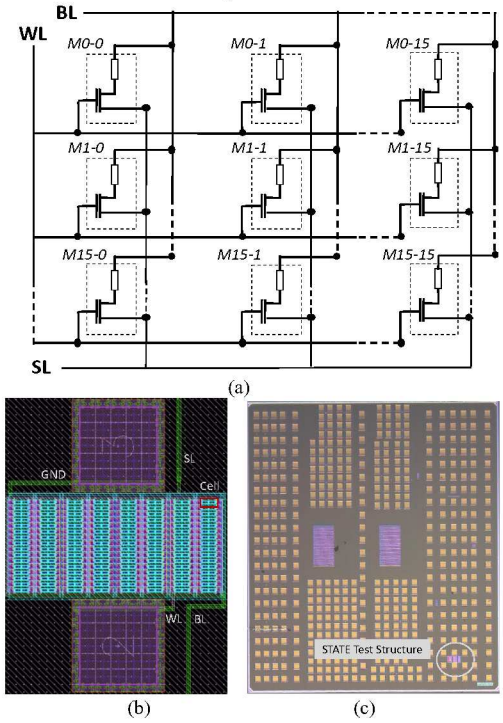

Fig. 3. (a) RRAM test structure architecture, (b) corresponding layout and (c) microchip view.

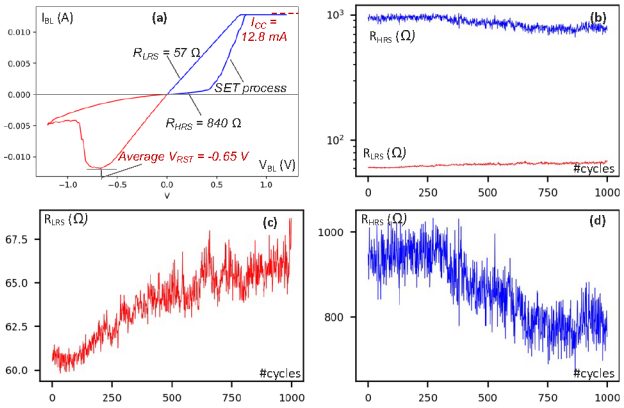

Fig. 4. (a) Test structure I-V hysteresis. (b) R_{HRS}/R_{LRS} in log scale (c) R_{LRS} and (d) R_{HRS} evolution in linear scale, all over 1,000 cycles.

In Fig. 3a, the test structure architecture is presented for a 16×16 1T1R array (256 cells). Its layout view is presented in Fig. 3b. The microchip view, embedding the STATE test chip, is presented in Fig. 3c. Note that the 16x16 STATE test structure differs from a classical memory array (such as the 8x8 1T1R elementary array used to characterize the variability of the technology in Section II.A) as all the cells are connected in parallel.

Only three external nodes are required to use the structure: WL, BL and SL. WL node is used to access the gates of all the select transistors of the memory cells to clamp the current flowing through each cell. BL and SL nodes are used to respectively SET and RST the whole memory array in a single shot and for a given compliance current.

The measurement methodology is very simple. From the transfer characteristic measured under the select transistor clamping bias (V_{WL}), the test structure allows a quick evaluation of the R_{LRS} and R_{HRS} average values. Also, it is possible to obtain accurate information regarding V_{SET} and V_{RST} thresholds. If the V_{SET} parameter is considered, a simple estimation of the RRAM SET threshold distribution can be extracted assuming a step-like current voltage characteristic for each RRAM cell, consequence of the select transistor clamping. Indeed, the clamping effect acts on each cell when the voltage across the structure increases during SET: as the voltage V_{BL} increases (SL node being grounded), the current I_{BL} in the structure is given by the sum of the N elementary contributions of the elementary cell currents I_{cell} in the array. I_{cell} reaches its maximum value I_{CC} when BL bias reaches the V_{SET} threshold of each elementary cell. This approach assumes that the cells turn on suddenly to the maximum clamping current in the case of V_{SET} distribution extraction, which is a reasonable approximation regarding the literature [20] and Fig. 1c. Based on this approximation, the global current derivative (i.e., transconductance) directly gives V_{SET} distribution according to (1).

$$G_{mSET} = \frac{\delta I_{BL}}{\delta V_{BL}} \quad (1)$$

This property of the test structure will be used during cycling tests to track the evolution of the SET voltages and detect early switching cells (fast cells or over-SET cells). Detecting fast cells is critical as these cells can be prone to failure. For instance, if the SET switching event occurs too early during one cycle, for a given cell, the latter will undergo an over-SET until the end of the programming signal. The following RST signal voltage might not be high enough to get back to the LRS state and, in such case, reaching the HRS may require several cycles. Additionally, fast cells make short pulse programming difficult, and can lead to failures at high operating speed. Thus, tracking early SET switching is a strong requirement during cycling.

From a practical perspective, it is expected that any variation of R_{HRS}, R_{LRS} and V_{SET} of an isolated cell of the test structure will be reflected in the I-V transfer characteristic of the test structure during endurance tests (i.e., one marginal cell impacts the behavior of the whole population of cells). This last point will be developed in the next section.

III. Experimental Results

A. Experimental setup

The experimental setup is based on a Keysight B1500 semiconductor parameter analyzer. During characterization, 1ms DC staircase voltage sweeps with a 0.02 V step are applied to the BL (SET) or the SL (RST) node of the test structure. As the applied voltage increases step by step the current IBL flowing through the structure is measured. Collecting I−V characteristics is a relatively slow process, compared to short voltage pulse programming approaches, however, we believe that this is the best way to precisely extract VSET threshold as well as RHRS and RLRS in each cycle. Moreover, having I-V hysteresis plots available for each cycle will ease the diagnosis in the case of endurance failures. Most importantly, and as already mentioned, if we consider a test structure made of N cells connected in parallel, the probability to catch a failure is N times higher (256 times in our case) compared to an isolated cell, which makes the test virtually 256 times faster.

B. Preliminary test results

For the first set of measurements, the compliance current is set to 50 µA for each cell, resulting in a maximal clamping current of 12.8 mA as shown in Fig. 4a. In these conditions, and before any cycle, the test structure HRS resistance is equal to 840 Ω giving an average isolated cell resistance of 215 kΩ, as cells are connected in parallel. After SET, the resistance is equal to 57 Ω, which represents an equivalent isolated cell resistance of 14.6 kΩ. Note that before any SET/RST operation, all the cells in the test structure have been formed, according to Table I bias voltages, with a compliance current set to 100 µA, resulting in a post-forming resistance of 38 Ω and an equivalent cell resistance of 9.7 kΩ. To have a first glance at the behavior of the test chip over cycles, 1,000 RST/SET cycles are applied to the circuit. Fig. 4b presents the variation of the HRS/LRS resistance window in log scale. Fig. 4c and Fig. 4d focus on the LRS and the HRS variations respectively.

Regarding the V_{SET} threshold, Fig. 5a shows the current derivative of the test structure I-V curve of Fig. 4a versus the programming voltage during the SET process. As the programming signal V_{BL} increases, memory cells are SET gradually.

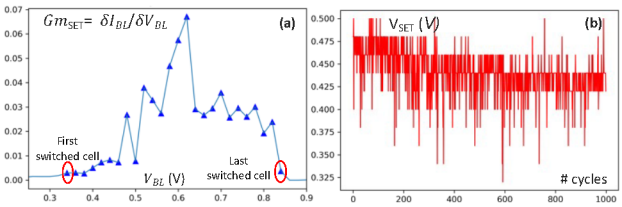

Fig. 5. (a) Current derivative during the SET process. (b) V_{SET} (fast cells) evolution over 1,000 cycles.

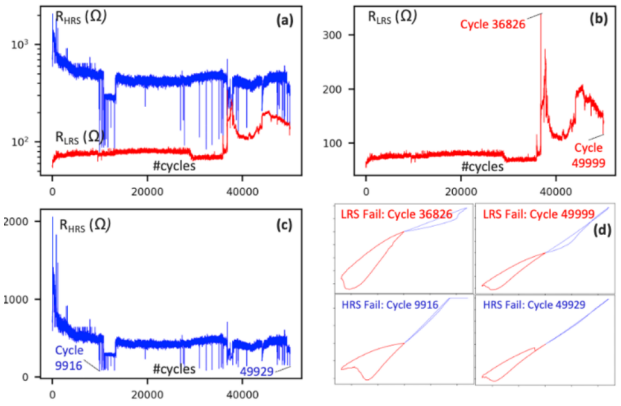

Fig. 6. (a) R_{LRS}/R_{HRS} resistances in log scale. (b) R_{LRS} in linear scale. (c) R_{HRS} in linear scale. (d) I-V characteristics extraction for specific cycles.

The presence of the resistive switching is detected by an increase in the current (i.e., abrupt current change up to 50 µA), allowing the switched cells to be counted. The SET process starts at 0.36 V (first switched cell) and ends at 0.84 V (last switched cell), resulting in a large SET programming window of 0.48 V. Fig. 5b shows the evolution of the SET voltage of the first switched cell in each cycle (fast cells) over 1000 cycles. Due to variability, fast cell thresholds range from 0.32 V to 0.5 V. Regarding VRST, its extraction is simplified due to the smoothing capability of the test structure (i.e., RST instability mitigation). According to Fig. 4a, VRST mean value is evaluated to -0.65 V.

C. *Endurance test results*

Endurance tests are conducted up to 50,000 cycles. Fig 6 shows the evolution of the HRS and LRS resistances in log (Fig. 6a) and linear scales for LRS (Fig. 6b) and for HRS (Fig. 6c). During cycling, an overall trend is observed. RHRS decreases, whereas RLRS increases. After some cycles, the characteristics of the RRAM devices start to deviate until failure (i.e., HRS and LRS levels overlap). It happens either because at least one cell stops matching its nominal characteristics or because at least one cell is stuck at a resistance state for several cycles or permanently. According to Fig. 6a and Fig. 6c, the endurance achieved is only 9,916 cycles which is much lower than the endurance results compiled in [5] where endurance claims larger than 106 cycles are reported for the same technology, while considering very few cycles in the endurance plots (<50) or an isolated cell or even both.

Regarding the marginal cell detection potential of the proposed approach, as RRAM cells are connected in parallel, the test structure overall resistance is dominated by memory cells with low resistance values. Hence, the numerous drops in the HRS are associated with memory cells having reached a low final HRS value after RST. So, an increase in the LRS is more difficult to detect as it is related to numerous memory cells having reached high LRS values after SET.

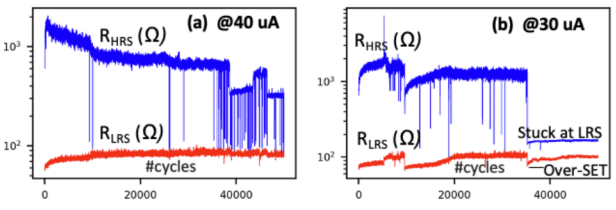

Fig. 7. R_{HRS}/R_{LRS} plots for (a) 40 µA and (b) 30 µA compliance currents.

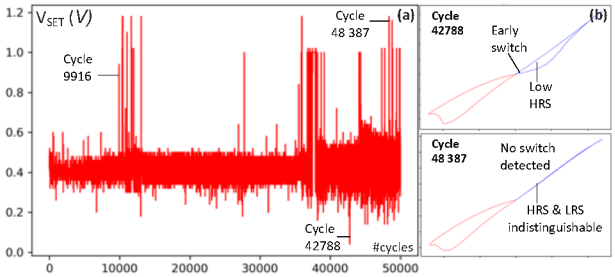

Fig. 8. (a) SET threshold variation over 50,000 cycles. (b) I-V characteristics extracted at cycles 42,788 and 48,387.

However, as SET and RST operations are related, an incorrect SET operation would be reflected in the HRS state associated with the next RST operation. A deep analysis of the cycles providing resistance values far from the nominal ones is conducted. I-V characteristics of cycles 36,826 and 49,999 (pointed out in Fig. 6b) are presented in Fig. 6d for diagnosis purposes. Compared to Fig 4a (golden curve), a reduction in the RHRS/RLRS ratio is detected. Fig. 6d also shows that the HRS/LRS gap is further reduced to a value close to zero when HRS fails are considered (cycles 9,916 and 49,929 pointed out in Fig. 6c).

The same analysis is performed for different test structures considering compliance currents of 40 µA and 30 µA (Fig. 7a and Fig. 7b). The same trend is observed with brutal changes in the HRS resistance values and a reduction of the HRS/LRS ratio. For a 30 µA compliance current, a stuck at LRS is observed around cycle 36,000. This can be attributed to over-SET cells unable to reach high HRS levels after RST.

Fig. 8a shows the evolution of the VSET voltage of fast cells during 50,000 cycles for a 50 µA compliance current per cell, usually targeted in this technology. An interesting observation can be made. VSET evolution is correlated with RHRS and RLRS evolution (see Fig. 6a). Indeed, RHRS drops are correlated with high VSET values. The first significant RHRS drop reported in Fig. 6c matches the first VSET significant increase detected in Fig. 8a. Both are detected at cycle 9,916. Some I-V characteristics of failing cycles are extracted and presented in Fig. 8b. Cycle 42,788 (lowest VSET value, detected at 0.05 V) and cycle 48,387 (large VSET value, detected at 1.18 V) are considered. For these two cycles, a correlation between marginal fast cells and a low HRS (i.e., high RHRS slope) can also be established.

It is worth noting that this methodology can be extended to any RRAM technology providing a hysteresis in its I-V characteristic at the cell level, such as CuOx-based RRAMs [21] or even subquantum CBRAM devices [22].

IV. Endurance Failures Mitigation Technique

Electrical parameter tracking during cycling considers positive current (positive part of the I-V characteristics [23]). Indeed, typically, RHRS and RLRS are extracted at 0.1 V. Fig. 6d and Fig. 8b provide some insight regarding the benefits of reading at -0.1V instead (negative part of the I-V characteristics), where the HRS/LRS ratio seems less affected by cycling. This observation is supported by the HRS and LRS plots versus cycling presented in Fig. 9a, where resistance values are extracted at -0.1V for a 50 µA compliance current. Although the classical RHRS/RLRS variation trend is observed, HRS drops are contained. An acceptable operating window with a resistance ratio >10 is observed up to 35,000 cycles, whereas, for a 0.1 V read voltage, the maximum reported endurance was 9,916 cycles.

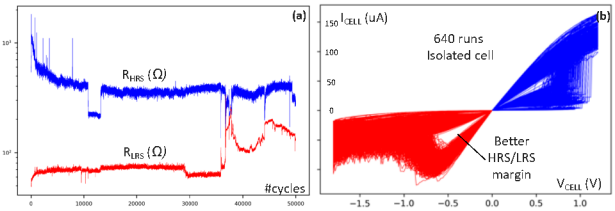

Fig. 9. (a) R_{HRS}/R_{LRS} plots extracted at -0.1 V (b) 640 I-V hysteresis extracted from an 8x8 memory array cycled 100 times.

To confirm this finding, 640 I-V characteristics extracted from an 8x8 memory array [14] cycled 100 times are presented in Fig. 9b where a better HRS/LRS window is detected in the RST direction (negative part of the curve). Thus, reading the RRAM cell is the RST direction at the design level, for the considered technology, would alleviate the effect of cycling combined with variability. This technique is particularly relevant as RRAM technology also suffers from classical defects related to memory arrays [24] as well as unique defects such as Intermittent Undefined State Fault (IUSF) [25][26]. Combined with variability, these defects can even more reduce the endurance of the technology.

V. Conclusion

Characterizing and quantifying the endurance of RRAM devices in an accurate manner is critical to assess their reliability. R_{HRS} and R_{LRS} as well as the switching voltages measurement in every cycle is particularly important to not overestimate the device lifetime. The proposed endurance evaluation methodology is based on a dedicated test structure comprising 256 OxRAM cells connected in parallel and allows a rapid and reliable prediction of endurance failures. For each cycle, a large number of cells is characterized during a single measurement, which allows to detect one defective cell among a whole population. Most of the important markers of RRAM technology, including HRS/LRS resistance levels and V_{SET} switching voltages are captured. The proposed study confirms the limitation of using a single cell during cycling tests which leads to an overestimation of the endurance.

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STATE: A Test Structure for Rapid and Reliable Prediction of Resistive RAM Endurance

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***Abstract*— Characterizing and quantifying the endurance of Resistive RAM devices is critical to assess their reliability for integration in electronic systems. This paper proposes a novel characterization methodology for rapid detection of RRAMs reliability issues during endurance tests. A test structure consisting of an array of non-addressable RRAM memory cells with parallel connection of all the memory elements is used for this purpose. The test structure fills the gap between isolated cells and circuit level endurance tests as it combines the test speed of an isolated cell while providing at the same time data from multiple devices. Endurance tests are conducted while monitoring RRAM electrical parameters of interest for each switching cycle. Experimental results show that most studies that claimed high endurance without capturing all switching cycles, or by considering an isolated cell, lead to an overestimation of the endurance. Finally, an endurance failures mitigation scheme based on RRAM current sensing in the RESET direction is presented to improve the endurance.**

Keywords*— *RRAM, OxRAM, Test structure, Endurance, Cycling, Reliability, Electrical parameters.

I. Introduction

Emerging technologies such as Resistive RAMs (RRAMs) are attracting considerable attention due to their tempting characteristics such as high scalability, CMOS compatibility and non-volatility [1]. Bipolar Oxide-based Resistive RAM (so-called OxRAM) is focusing strong interests as a candidate for densely packed cross-point 3D-arrays, high performance Storage Class Memory (SCM), as well as a new component able to unlock the full potential of disruptive computing architecture such as edge-Artificial Intelligence [2]. For any application, one of the most important properties of RRAMs is their cycling endurance, defined as the maximum number of programming cycles (one RESET (RST) transition followed by one SET transition) that the device can undergo before its electrical characteristics start to deviate, until failure [3]. Moreover, during cycling, the RRAM resistance can get unpredictably stuck at one resistance state for some time and suddenly recover the normal operation [4]. Therefore, characterizing the endurance of RRAM devices in an accurate manner is a strong requirement.

However, the state-of-the art regarding endurance tests suffers from several limitations. First, most of the publications that claimed high endurance (>10^6) are based on endurance plots considering very few cycles (in many cases even <50) [5]. Which means that RRAM electrical parameter extraction is performed considering less than 50 cycles out of 10^6 cycles. This approach is unreliable as the cycling endurance of RRAM devices requires measuring their electrical properties for each cycle. Otherwise, the incapacity of the RRAM to switch correctly for some cycles can be missed, which leads to an overestimation of the actual endurance. Secondly, most studies only consider one single device, masking the intrinsic variability of the technology [6][7]. Indeed, it is known that the standard qualification procedure for memory endurance in the industry requires statistical results from a sufficiently large memory array [8]. And, most of the time, an array-level analysis with many devices is typically not available in the early development stage, especially for emerging technologies. Even though large memory array circuits are available, systematic cycling induces important test time overheads (address-program-read operation for each memory word). Therefore, and for all the above-mentioned reasons, there is an urgent need for a smart monitoring technique able to track in a reliable manner the correct switching of the RRAM device over time.

In this work, a lightweight test structure, presented for the first time in [9], and referred to as STATE (StrucTure for rApid predicTion of RRAM Electrical parameter variability) is used to allow a rapid and reliable prediction of endurance failures. The proposed use case of the test structure allows the development of a full framework dedicated to cycling failures detection and analysis. To the authors' knowledge, this is the first work which presents an alternative to current RRAM cycling tests.

The main contributions of the paper are as follows:

- The STATE test structure is processed to monitor and speed up RRAM parameters extraction during cycling.
- As the test structure is made of devices connected in parallel, with only three external nodes, multiple devices are considered during a single measurement.
- Targeting a large number of cells, in a single shot, allows to detect more quickly one defective device among a whole population, making cycling tests faster.
- Fast execution of the endurance test allows to extract the RRAM electrical parameters for each cycle. This aspect is largely neglected in many studies related to endurance [5].

The remainder of the paper is organized as follows. Section II introduces the RRAM test structure. In section III, experimental endurance results are presented and discussed. In section IV, an endurance failure mitigation scheme is proposed. Finally, section V concludes the paper.

II. RRAM Test structure

A. RRAM Technology Background

Fig. 1a shows a basic 1T1R memory device where one MOS transistor (W = 0.8 µm and L = 0.5 µm) is connected in series with one RRAM cell. The RRAM resistive element, depicted in Fig. 1b, is integrated in the BEOL of a 130nm technology, between M4 and M5 layers [10]. The stack is deposited using Physical Vapor Deposition (PVD) where a 10nm Hafnium dioxide (HfO_2) layer is placed on the top of a TiN Bottom electrode (BE). A Ti/TiN bilayer stack is then deposited as a top electrode (TE) to form a capacitor-like structure. Fig. 1c shows a typical 1T1R I-V characteristic. Based on this I-V curve, the memory cell operation can be seen as follows: after an initial electro-Forming (FMG) step

[11], the memory element can be switched in a reversible manner between the Low Resistance State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T1R cell, i.e., V_{SET} to switch to LRS after a SET operation and V_{RST} to switch to HRS after an RST operation.

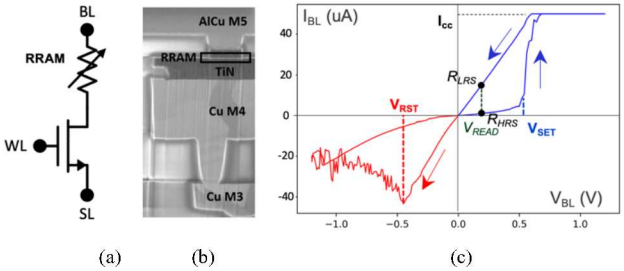

Fig. 1. (a) Symbol view of a 1T1R cell. (b) SEM cross section of the RRAM, integrated on top of Metal 4 [10]. (c) RRAM I-V characteristic.

The voltage levels used during the different operating stages are presented in Table I, along with the resulting nominal resistance values. Based on the memory cell hysteresis presented in Fig. 1c, four critical reliability parameters can be considered: V_{SET}, V_{RST}, R_{HRS} and R_{LRS}. From a design point of view, any variation of these parameters can lead to reliability issues. Note that R_{HRS} and R_{LRS} are extracted at V_{BL}=0.1 V during a READ operation, in the forward or SET direction (blue curve in Fig. 1c, with V_{BL}>0). Also, in the 1T1R configuration, the transistor controls the current level flowing through the cell according to its gate voltage bias. This clamping current allowed by the select transistor is called the compliance current and is referred to as I_{CC}.

TABLE I. STANDARD CELL OPERATING VOLTAGES

	FMG	RST	SET	READ
WL	2 V	2.5 V	2 V	2.5 V
BL	3.3 V	0 V	1.2 V	0.1 V
SL	0 V	1.2 V	0 V	0 V
$R_{LRS/HRS}$	10 kΩ	240 kΩ	15 kΩ	-

One of the most important challenges of RRAM technology is the control of the device variability (temporal and spatial) in both LRS and HRS states [12][13]. In fact, variations of R_{HRS}/R_{LRS} and V_{SET}/V_{RST} are so unpredictable that they have been employed as an entropy source in True Random Number Generators (TRNG) [14][15]. Indeed, variance from Cycle to Cycle (C2C) and from Device to Device (D2D) is very large, impacting directly the memory R_{HRS} and R_{LRS} resistances. This intrinsic drawback of the technology, combined with aging, has a straight impact on the RRAM technology reliability [5]. To assess the impact of variability on the HRS/LRS resistance ratio, an 8x8 (64 cells) elementary 1T1R array [14] is considered for measurements. A FMG operation is first applied to the memory array. Then, each memory cell is RST to extract R_{HRS}. After RST, cells are SET to extract R_{LRS}. The effect of variability (combining D2D and C2C) is highlighted in the cumulative probability plot presented in Fig. 2 obtained after 500 consecutive RST/SET cycles applied to the memory array (500x64 cells). A 0.1 V READ bias voltage is used to extract R_{LRS} and R_{HRS} distributions. Note that the HRS distribution spread is more pronounced compared to the LRS spread, which is a common feature of OxRAM technologies [16].

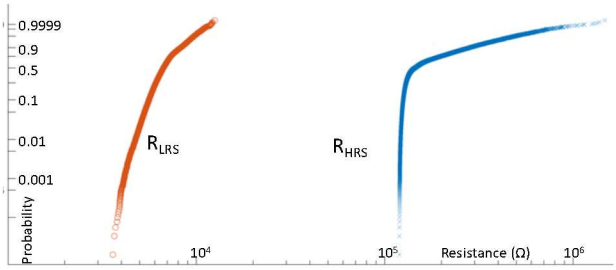

Fig. 2. HRS and LRS resistance distribution measurement results based on an OxRAM memory array fabricated in a 130 nm CMOS technology.

In addition to variability, over time, most of RRAM devices fail during cycling because of the degradation of their atomic structure, often associated with the formation of oxygen vacancies in the insulator for HfO_2-based devices [17]. It has been demonstrated in [6], for Ti/HfO_x/TiN devices, that the values of R_{HRS} and R_{LRS} experienced a progressive drift until the two states became indistinguishable. Findings from other studies have reported that the resistances of the device can also get erratically stuck in one state in some cycles and recover the normal functioning suddenly [4]. This unpredictable behavior clearly indicates that endurance tests must be conducted by checking that the device effectively switches in each cycle.

B. *RRAM Test Structure Architecture*

During the early phase of development, it is often difficult to obtain sufficient reliable data on RRAM memories. The process itself is not stabilized and fully functional devices are not yet available. At this stage, test structures can play an important diagnostic role in climbing the yield learning curve and in providing valuable reliability data [18][19]. The proposed RRAM test structure is based on a basic array consisting of not addressable RRAM cells with parallel connection of all the memory elements.

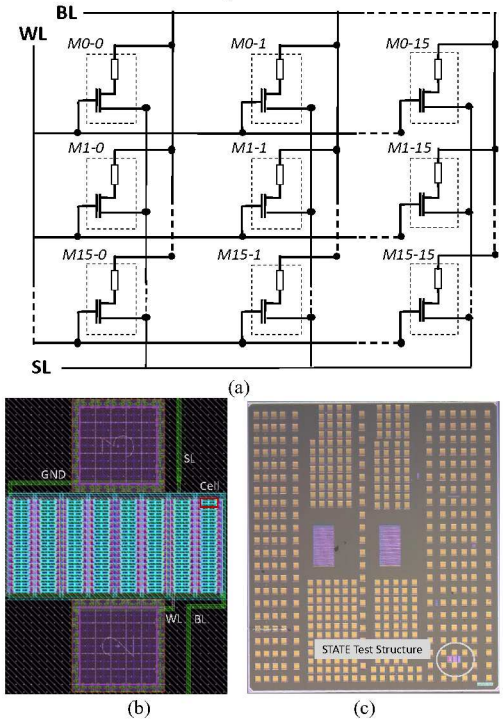

Fig. 3. (a) RRAM test structure architecture, (b) corresponding layout and (c) microchip view.

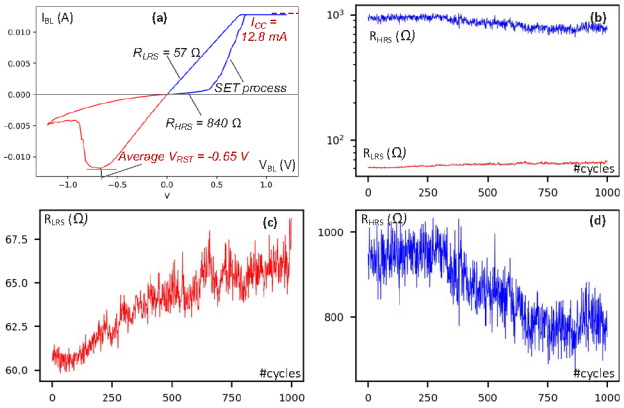

Fig. 4. (a) Test structure I-V hysteresis. (b) R_{HRS}/R_{LRS} in log scale (c) R_{LRS} and (d) R_{HRS} evolution in linear scale, all over 1,000 cycles.

In Fig. 3a, the test structure architecture is presented for a 16×16 1T1R array (256 cells). Its layout view is presented in Fig. 3b. The microchip view, embedding the STATE test chip, is presented in Fig. 3c. Note that the 16x16 STATE test structure differs from a classical memory array (such as the 8x8 1T1R elementary array used to characterize the variability of the technology in Section II.A) as all the cells are connected in parallel.

Only three external nodes are required to use the structure: WL, BL and SL. WL node is used to access the gates of all the select transistors of the memory cells to clamp the current flowing through each cell. BL and SL nodes are used to respectively SET and RST the whole memory array in a single shot and for a given compliance current.

The measurement methodology is very simple. From the transfer characteristic measured under the select transistor clamping bias (V_{WL}), the test structure allows a quick evaluation of the R_{LRS} and R_{HRS} average values. Also, it is possible to obtain accurate information regarding V_{SET} and V_{RST} thresholds. If the V_{SET} parameter is considered, a simple estimation of the RRAM SET threshold distribution can be extracted assuming a step-like current voltage characteristic for each RRAM cell, consequence of the select transistor clamping. Indeed, the clamping effect acts on each cell when the voltage across the structure increases during SET: as the voltage V_{BL} increases (SL node being grounded), the current I_{BL} in the structure is given by the sum of the N elementary contributions of the elementary cell currents I_{cell} in the array. I_{cell} reaches its maximum value I_{CC} when BL bias reaches the V_{SET} threshold of each elementary cell. This approach assumes that the cells turn on suddenly to the maximum clamping current in the case of V_{SET} distribution extraction, which is a reasonable approximation regarding the literature [20] and Fig. 1c. Based on this approximation, the global current derivative (i.e., transconductance) directly gives V_{SET} distribution according to (1).

$$G_{mSET} = \frac{\delta I_{BL}}{\delta V_{BL}} \quad (1)$$

This property of the test structure will be used during cycling tests to track the evolution of the SET voltages and detect early switching cells (fast cells or over-SET cells). Detecting fast cells is critical as these cells can be prone to failure. For instance, if the SET switching event occurs too early during one cycle, for a given cell, the latter will undergo an over-SET until the end of the programming signal. The following RST signal voltage might not be high enough to get back to the LRS state and, in such case, reaching the HRS may require several cycles. Additionally, fast cells make short pulse programming difficult, and can lead to failures at high operating speed. Thus, tracking early SET switching is a strong requirement during cycling.

From a practical perspective, it is expected that any variation of R_{HRS}, R_{LRS} and V_{SET} of an isolated cell of the test structure will be reflected in the I-V transfer characteristic of the test structure during endurance tests (i.e., one marginal cell impacts the behavior of the whole population of cells). This last point will be developed in the next section.

III. Experimental Results

A. Experimental setup

The experimental setup is based on a Keysight B1500 semiconductor parameter analyzer. During characterization, 1ms DC staircase voltage sweeps with a 0.02 V step are applied to the BL (SET) or the SL (RST) node of the test structure. As the applied voltage increases step by step the current IBL flowing through the structure is measured. Collecting I−V characteristics is a relatively slow process, compared to short voltage pulse programming approaches, however, we believe that this is the best way to precisely extract VSET threshold as well as RHRS and RLRS in each cycle. Moreover, having I-V hysteresis plots available for each cycle will ease the diagnosis in the case of endurance failures. Most importantly, and as already mentioned, if we consider a test structure made of N cells connected in parallel, the probability to catch a failure is N times higher (256 times in our case) compared to an isolated cell, which makes the test virtually 256 times faster.

B. Preliminary test results

For the first set of measurements, the compliance current is set to 50 µA for each cell, resulting in a maximal clamping current of 12.8 mA as shown in Fig. 4a. In these conditions, and before any cycle, the test structure HRS resistance is equal to 840 Ω giving an average isolated cell resistance of 215 kΩ, as cells are connected in parallel. After SET, the resistance is equal to 57 Ω, which represents an equivalent isolated cell resistance of 14.6 kΩ. Note that before any SET/RST operation, all the cells in the test structure have been formed, according to Table I bias voltages, with a compliance current set to 100 µA, resulting in a post-forming resistance of 38 Ω and an equivalent cell resistance of 9.7 kΩ. To have a first glance at the behavior of the test chip over cycles, 1,000 RST/SET cycles are applied to the circuit. Fig. 4b presents the variation of the HRS/LRS resistance window in log scale. Fig. 4c and Fig. 4d focus on the LRS and the HRS variations respectively.

Regarding the V_{SET} threshold, Fig. 5a shows the current derivative of the test structure I-V curve of Fig. 4a versus the programming voltage during the SET process. As the programming signal V_{BL} increases, memory cells are SET gradually.

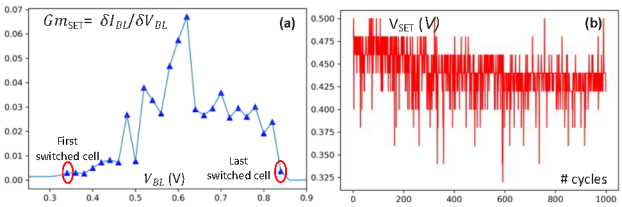

Fig. 5. (a) Current derivative during the SET process. (b) V_{SET} (fast cells) evolution over 1,000 cycles.

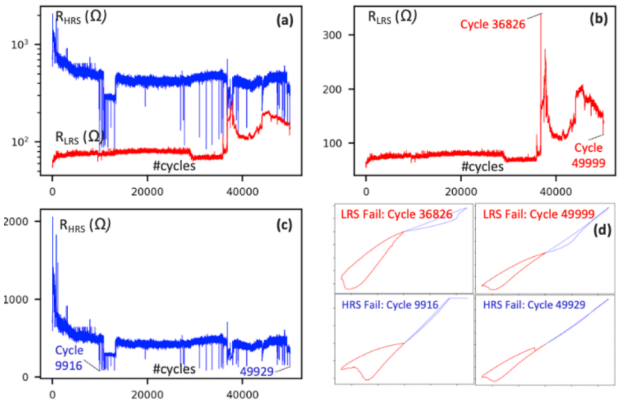

Fig. 6. (a) R_{LRS}/R_{HRS} resistances in log scale. (b) R_{LRS} in linear scale. (c) R_{HRS} in linear scale. (d) I-V characteristics extraction for specific cycles.

The presence of the resistive switching is detected by an increase in the current (i.e., abrupt current change up to 50 µA), allowing the switched cells to be counted. The SET process starts at 0.36 V (first switched cell) and ends at 0.84 V (last switched cell), resulting in a large SET programming window of 0.48 V. Fig. 5b shows the evolution of the SET voltage of the first switched cell in each cycle (fast cells) over 1000 cycles. Due to variability, fast cell thresholds range from 0.32 V to 0.5 V. Regarding VRST, its extraction is simplified due to the smoothing capability of the test structure (i.e., RST instability mitigation). According to Fig. 4a, VRST mean value is evaluated to -0.65 V.

C. *Endurance test results*

Endurance tests are conducted up to 50,000 cycles. Fig 6 shows the evolution of the HRS and LRS resistances in log (Fig. 6a) and linear scales for LRS (Fig. 6b) and for HRS (Fig. 6c). During cycling, an overall trend is observed. RHRS decreases, whereas RLRS increases. After some cycles, the characteristics of the RRAM devices start to deviate until failure (i.e., HRS and LRS levels overlap). It happens either because at least one cell stops matching its nominal characteristics or because at least one cell is stuck at a resistance state for several cycles or permanently. According to Fig. 6a and Fig. 6c, the endurance achieved is only 9,916 cycles which is much lower than the endurance results compiled in [5] where endurance claims larger than 106 cycles are reported for the same technology, while considering very few cycles in the endurance plots (<50) or an isolated cell or even both.

Regarding the marginal cell detection potential of the proposed approach, as RRAM cells are connected in parallel, the test structure overall resistance is dominated by memory cells with low resistance values. Hence, the numerous drops in the HRS are associated with memory cells having reached a low final HRS value after RST. So, an increase in the LRS is more difficult to detect as it is related to numerous memory cells having reached high LRS values after SET.

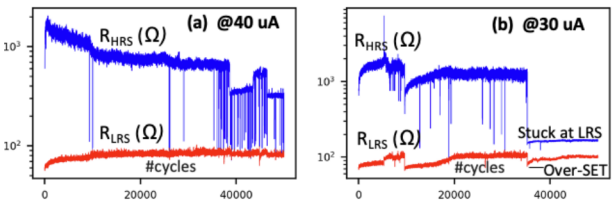

Fig. 7. R_{HRS}/R_{LRS} plots for (a) 40 µA and (b) 30 µA compliance currents.

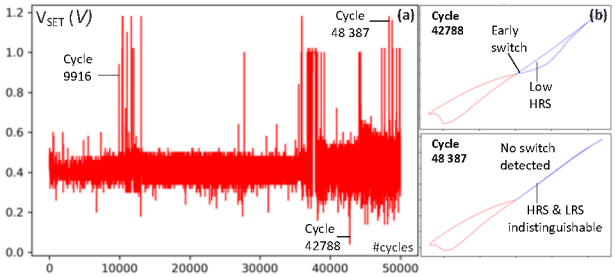

Fig. 8. (a) SET threshold variation over 50,000 cycles. (b) I-V characteristics extracted at cycles 42,788 and 48,387.

However, as SET and RST operations are related, an incorrect SET operation would be reflected in the HRS state associated with the next RST operation. A deep analysis of the cycles providing resistance values far from the nominal ones is conducted. I-V characteristics of cycles 36,826 and 49,999 (pointed out in Fig. 6b) are presented in Fig. 6d for diagnosis purposes. Compared to Fig 4a (golden curve), a reduction in the RHRS/RLRS ratio is detected. Fig. 6d also shows that the HRS/LRS gap is further reduced to a value close to zero when HRS fails are considered (cycles 9,916 and 49,929 pointed out in Fig. 6c).

The same analysis is performed for different test structures considering compliance currents of 40 µA and 30 µA (Fig. 7a and Fig. 7b). The same trend is observed with brutal changes in the HRS resistance values and a reduction of the HRS/LRS ratio. For a 30 µA compliance current, a stuck at LRS is observed around cycle 36,000. This can be attributed to over-SET cells unable to reach high HRS levels after RST.

Fig. 8a shows the evolution of the VSET voltage of fast cells during 50,000 cycles for a 50 µA compliance current per cell, usually targeted in this technology. An interesting observation can be made. VSET evolution is correlated with RHRS and RLRS evolution (see Fig. 6a). Indeed, RHRS drops are correlated with high VSET values. The first significant RHRS drop reported in Fig. 6c matches the first VSET significant increase detected in Fig. 8a. Both are detected at cycle 9,916. Some I-V characteristics of failing cycles are extracted and presented in Fig. 8b. Cycle 42,788 (lowest VSET value, detected at 0.05 V) and cycle 48,387 (large VSET value, detected at 1.18 V) are considered. For these two cycles, a correlation between marginal fast cells and a low HRS (i.e., high RHRS slope) can also be established.

It is worth noting that this methodology can be extended to any RRAM technology providing a hysteresis in its I-V characteristic at the cell level, such as CuOx-based RRAMs [21] or even subquantum CBRAM devices [22].

IV. Endurance Failures Mitigation Technique

Electrical parameter tracking during cycling considers positive current (positive part of the I-V characteristics [23]). Indeed, typically, RHRS and RLRS are extracted at 0.1 V. Fig. 6d and Fig. 8b provide some insight regarding the benefits of reading at -0.1V instead (negative part of the I-V characteristics), where the HRS/LRS ratio seems less affected by cycling. This observation is supported by the HRS and LRS plots versus cycling presented in Fig. 9a, where resistance values are extracted at -0.1V for a 50 µA compliance current. Although the classical RHRS/RLRS variation trend is observed, HRS drops are contained. An acceptable operating window with a resistance ratio >10 is observed up to 35,000 cycles, whereas, for a 0.1 V read voltage, the maximum reported endurance was 9,916 cycles.

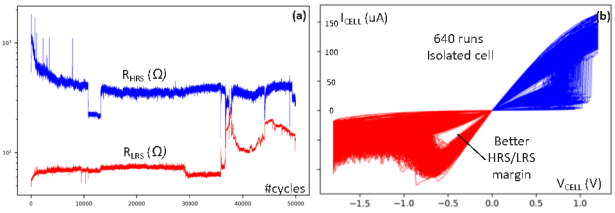

Fig. 9. (a) R_{HRS}/R_{LRS} plots extracted at -0.1 V (b) 640 I-V hysteresis extracted from an 8x8 memory array cycled 100 times.

To confirm this finding, 640 I-V characteristics extracted from an 8x8 memory array [14] cycled 100 times are presented in Fig. 9b where a better HRS/LRS window is detected in the RST direction (negative part of the curve). Thus, reading the RRAM cell is the RST direction at the design level, for the considered technology, would alleviate the effect of cycling combined with variability. This technique is particularly relevant as RRAM technology also suffers from classical defects related to memory arrays [24] as well as unique defects such as Intermittent Undefined State Fault (IUSF) [25][26]. Combined with variability, these defects can even more reduce the endurance of the technology.

V. Conclusion

Characterizing and quantifying the endurance of RRAM devices in an accurate manner is critical to assess their reliability. R_{HRS} and R_{LRS} as well as the switching voltages measurement in every cycle is particularly important to not overestimate the device lifetime. The proposed endurance evaluation methodology is based on a dedicated test structure comprising 256 OxRAM cells connected in parallel and allows a rapid and reliable prediction of endurance failures. For each cycle, a large number of cells is characterized during a single measurement, which allows to detect one defective cell among a whole population. Most of the important markers of RRAM technology, including HRS/LRS resistance levels and V_{SET} switching voltages are captured. The proposed study confirms the limitation of using a single cell during cycling tests which leads to an overestimation of the endurance.

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H. AZIZA received his B.S. and M.S. degrees in Electrical Engineering, both from University of Marseille, France. He received his Ph.D. degree in 2002 from the University of Marseille, France. Hassen Aziza is currently associate professor at Aix-Marseille University-IM2NP laboratory (Institute of materials, microelectronics and nanosciences of Provence). His research fields cover design, test and reliability of conventional non-volatile memories (Flash & EEPROM) as well as emerging memories (Resistive RAM). He is (co)author of more than 120 papers in international conferences and journals and is (co)inventor of 5 patents. Hassen AZIZA was involved the French National Research Agency project DIPMEM dedicated to hybrid circuit design (CMOS-ReRAM). Since 2017, Hassen AZIZA is the IM2NP's "Memory Team" leader. IM2NP's "Memory Team" is composed of 12 permanents. Research thematics conducted by the group are fully dedicated to Resistive RAM technology, Design and Test.

M. J. Postel-Pellerin was born in 1982. He received M.S. and Ph.D. degrees from Aix-Marseille University, Marseille, France, in 2005 and 2008, respectively. He joined the Memory Team of the Institut Matériaux Microélectronique Nanosciences de Provence (IM2NP), Marseille, France, in 2009 and became an Associate Professor with Aix-Marseille University. His current research interests include the electrical characterization, the modeling and the TCAD simulation of Flash memories, especially for reliability and security studies. He is also working on the development of innovative floating-gate NVM architectures for low-energy applications.

M. Moreau received the Master of Science and Ph.D. degrees in micro and nanoelectronics from Aix-Marseille University, France, respectively in 2007 and 2010. His doctoral research at the Institute of Materials Microelectronics and Nanosciences of Provence (IM2NP) covered numerical simulation and compact modeling of advanced nano-devices, like FinFET, based on new materials (high-k and III-V semiconductors). From 2010 to 2011, he was teaching assistant at polytech'Marseille and work on compact modeling of organic thin film transistors (OTFT). Since 2012, he is associate professor at Aix-Marseille University and conducts his research at IM2NP in the field of hybrid circuit design based on emerging non-volatile memories (ReRAM, MRAM, …). He is recipient of the Newcas 2013 Best Paper Award and the 2017 IEEE Transactions on Circuits and Systems Guillemin-Cauer Best Paper Award.

Reviewer: 1

1. Using STATE in the title I find confusing, especially since STATE is not defined in the text. Do the letters stand for anything, or is it just the name you gave the structure? Please clarify and update the manuscript.

STATE stands for: A Test Structure for Rapid Prediction of Resistive RAM Electrical Parameter Variability.
It is defined in the third paragraph of the first section: “In this work, a lightweight test structure, presented for the first time in [9], and referred to as STATE (A Test Structure for Rapid Prediction of Resistive RAM Electrical Parameter Variability)”.

The sentence has been rephrased to better highlight the meaning of the acronym:
“In this work, a lightweight test structure, presented for the first time in [9], and referred to as STATE (StrucTure for rApid predicTion of RRAM Electrical parameter variability)”

2. In the 1st paragraph of the introduction, endurance is defined as the max number of SET & RESET cycles. But in the 2nd paragraph of the introduction, you write that "...claimed high endurance (>10^6)...few cycles (in many cases even <50)[5][6]". I don't understand that statement. Are you saying that some authors are measuring <50 cycles and claim 10^6?
At least in [6] Fig.5 it seems that endurance was tested for >1.5x10^5 cycles. Please clarify and update the manuscript.
Thanks for the feedback. Indeed, the sentence creates confusion.
What I mean is that some authors are only plotting electrical parameters for less than 50 cycles in the endurance plots, while the endurance test lasts 10^6 cycles (i.e., electrical parameter extraction is performed once in a while during the endurance test). Thus, some potential electrical parameter drifts are missed during the test. To accurately monitor RRAM parameter evolution, electrical parameters have to be extracted 10^6 times (i.e., after each cycle).
The sentence has been rephrased:
“First, most of the publications that claimed high endurance (>10^6) are based on endurance plots considering very few cycles (in many cases even <50) [5]. Which means that RRAM electrical parameter extraction is performed considering less than 50 cycles out of 10^6 cycles”.

Indeed, in [6], endurance was tested for >1.5x10^5 cycles, but it is not clear if resistances have been extracted for each cycle.
Anyway, to be compliant with Ref [6] findings, Ref [6] has been moved here:
Secondly, most studies only consider one single device, masking the intrinsic variability of the technology [6][7].

3. For most figures the symbols, axis titles and labels are too small (especially Fig. 2, 4, 5, 6, 8, 9). For better readability, especially after printing, please improve.
Fig.2 and Fig.4 to Fig.9 improved
As well as Fig. 3a
Figure locations rearranged for better readability.

4. You mention 8x8 cells, 16x16 cells and an array of 500x64 cells. From the text it is not clear why different cells were used and which test was done on which cell. Please add that info.

- To characterize the variability of the technology and assess the impact of variability on the HRS/LRS resistance ratio, a 8x8 1T-1R classical array is used (64 cells). Measurement results are presented in section II.A. As this elementary array is cycled 500 times, 500x60 measurements points are plotted in Fig.2 of Section II.A.

- The STATE test structure, which architecture is different from a classical memory array (all the cells are connected in parallel), is presented and processed in Section II.B. This is 16x16 array of cells connected in parallel.

Text added in Section II.B:
"Note that the 16x16 STATE test structure differs from a classical memory array (such as the 8x8 1T1R elementary array used to characterize the variability of the technology in Section II.A) as all the cells are connected in parallel."

5. In section III-A it is mentioned that slow IV ramp is preferred instead of pulses. Since the RRAM properties LRS, RHRS, endurance and retention depend on the FRM/SET/RESET condition (voltage, time), can the authors comment (ideally in the manuscript) on how the results are applicable to real products which most likely use pulses in the few us range?
Thanks for this valuable feedback.
Indeed, real products use pulses for programming operation (FRM/SET/RESET), which is different from the programming signals used in the proposed methodology.

However, the proposed methodology is dedicated to test chips, not to real products. As mentioned in the text (Section II.B), "during the early phase of development, it is often difficult to obtain sufficient reliable data on RRAM memories. The process itself is not stabilized and fully functional devices are not yet available. At this stage, test structures can play an important diagnostic role in climbing the yield learning curve and in providing valuable reliability data."

This methodology is intended to become a standard for high-speed endurance tests for a given technology. Each technology/process optimization trial would provide a test chip for endurance evaluation. Different technologies/recipe can be benchmarked regarding endurance based on the proposed test chip.

6. In section III-C the authors compare their endurance results to [5]. Are you both using the same RRAM process and hardware? If not, couldn't the difference in endurance just be due to different stack properties?

In fact, different stacks are benchmarked in [5]. Among these stacks, two are considered for comparison (same technology as the one proposed in this paper: TiN/Hf/HfO2/TiN stack):

- Chen, Y. Y.; Goux, L.; Clima, S.; Govoreanu, B.; Degraeve, R.; Kar, G. S.; Fantini, A.; Groeseneken, G.; Wouters, D. J.; Jurczak, M. Endurance/Retention Trade-Off on HfO2/Metal Cap 1T1R Bipolar RRAM. IEEE Trans. Electron Devices 2013, 60, 1114–1121.
- Chen, Y. Y.; Govoreanu, B.; Goux, L.; Degraeve, R.; Fantini, A.; Kar, G. S.; Wouters, D. J.; Groeseneken, G.; Kittl, J. A.; Jurczak, M.; et al. Balancing SET/RESET Pulse for 1010 Endurance in HfO2/ Hf 1T1R Bipolar RRAM. IEEE Trans. Electron Devices 2012, 59, 3243–3249.

7. The authors misspelled their names in the cover page (Hassan instead of Hassen) and in the bio section (M. Postel-Pellerin instead of J. Postel-Pellerin).
Fixed

Reviewer: 2

1. Is this method only suitable for OxRAM-type devices? How about the consideration of the other emerging devices, CBRAM type, and subquantum type devices (10.1109/IEDM.2005.1609463; https://www.nature.com/articles/s41467-018-07682-0; Electronics 9 (6), 1029, 2020)?

This methodology is dedicated to any Resistive RAM technology providing a hysteresis at the cell level in its I-V characteristic. CBRAM types and subquantum type devices falls into this category.
Text added (end of Section III.C):
"It is worth noting that this methodology can be extended to any technology providing a hysteresis in its I-V characteristic at the cell level, such as CBRAM [21] or even subquantum CBRAM devices [22]"

2. Revise the references to increase the visibility of this work.

All references rewritten with full information.

4 references added:
[21] Y. Shi et al., "A Neuromorphic Brain Interface Based on RRAM Crossbar Arrays for High Throughput Real-Time Spike Sorting," in IEEE Transactions on Electron Devices, vol. 69, no. 4, pp. 2137-2144, 2022.
[22] Shi Y., Nguyen L., Oh S. et al. , "Neuroinspired unsupervised learning and pruning with subquantum CBRAM arrays," Nat Commun 9, 5312 2018.
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[25] M. Fieback, G. C. Medeiros, A. Gebregiorgis, H. Aziza, M. Taouil and S. Hamdioui, "Intermittent Undefined State Fault in RRAMs," 2021 IEEE European Test Symposium (ETS), 2021, pp. 1-6, doi: 10.1109/ETS50041.2021.9465401.
[26] M. Fieback et al., "Defects, Fault Modeling, and Test Development Framework for RRAMs," ACM Journal on Emerging Technologies in Computing Systems (JETC), 18(3), 1-26, 2022.
With additional text:
"This technique is particularly relevant as RRAM technology also suffers from classical defects related to memory arrays [24] as well as unique defects such as Intermittent Undefined State Fault (IUSF) [25][26]. Combined with variability, these defects can even more reduce the endurance of the technology."

3. Improve the figure quality.
Fixed
Fig.2 and Fig.4 to Fig.9 improved
Figure locations rearranged for better readability.