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Abstract: One of the important features of Resistive RAM (RRAM) is its conductance modulation, which makes it suitable for neuromorphic computing systems. In this paper, the conductance modulation of Oxide-based RAM (OxRAM) devices is evaluated based on experimental data to reveal its inherent analog synaptic behavior. A test chip made of a classical 1T-1R elementary memory array is used to demonstrate the conductance modulation. Using an array of cells, as opposed to an isolated cell, allows to catch temporal as well as spatial variabilities. Thus, the multiple resistance levels capability of OxRAMs is assessed in a more realistic context. Two different programming techniques are used to program the OxRAM cells. The first approach leverages on RESET (RST) voltage control. The second approach relies on compliance current control during the SET operation. In both approaches, although multiple resistance levels can be easily obtained, it is demonstrated that a successful implementation of a reliable conductance modulation scheme mainly depends on the ability to precisely control the impact of variability on the different conductance levels obtained after the programming operation.

Keywords: memristor; RRAM; OxRAM; synapses; conductance modulation; neuromorphic circuits; neural networks

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1. Introduction

Conventional computing technology based on Von Neumann (VN) architecture is facing fundamental limits, such as poor energy efficiency and latency [1]. This is particularly true when dealing with the vast amount of data generated by IoT devices, self-driving cars, cloud computing, etc. [2]. This situation, known as the "memory wall", encourages the investigation of different processing information paradigms considered as non-Von Neumann (non-VN) architectures [3]. Over the last few years there has been a lot of activity across research groups proposing efficient hybrid "CMOS-nanodevice" computing hardware architectures, such as Artificial Neural Networks (ANNs) [4]. Indeed, ANNs have demonstrated impressive performances in recognition tasks where classical VN hardware architectures have difficulties classifying or organizing data, something that the human brain seems to accomplish efficiently.

ANNs are meant to mimic biological neural networks. ANNs architectures are based on a large collection of units that are interconnected in some pattern to allow communication between the units. These units are referred to as nodes or neurons. Each node is connected with other neurons through a connection link or synapse associated with a weight. Weights usually excite or inhibit the signal that is being communicated over the network. Thus, ANN can be seen as a complex adaptive system, which can change its internal structure based on the information passing through it [5]. Emerging Back-End-of-Line (BEOL) resistive memory devices [6,7] are considered as the optimum candidates to emulate biological synaptic behavior at nanometer scale as they offer the possibility to modulate their conductance in addition to being easily integrated with CMOS-based neuron circuits [8,9]. Among these emerging technologies, Oxide-based RAM (OxRAM) have proven to be very effective in implementing some aspects of synaptic plasticity [10].

A recent advance in the field of OxRAM memories is related to the possibility of Multi Level Cell (MLC) conductance, needed for the implementation of synaptic weight quantization. According to this approach, more than two data conductance states are made possible, simply by finely controlling the programming of the cell. Thus, OxRAMs can be considered as a time variable resistor, which makes the technology a potential candidate for implementing conventional ANNs.

At a circuit level, different conductance modulation techniques can be adopted. Conductance modulation can be achieved by (i) applying an increasing number of identical voltage pulses across the OxRAM—in this case, conductance levels are a function of the number of pulses [11]; (ii) directly modulating the programming voltage levels [12]; (iii) modulating the compliance current of the memory cell during programming operations [13]. The first approach requires an embedded pulse generator, while the two others require analog voltage levels generated from a specific circuitry.

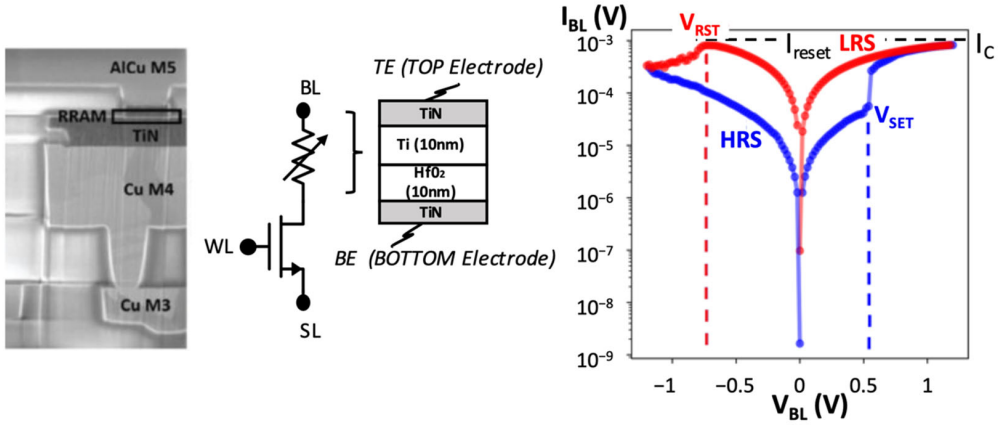
Despite the advances made in this field, there are still open issues that are currently under investigation. The most important one is related to the variability of the OxRAM technology, which leads to synaptic weight precision reduction [14,15].

In this paper, we present how OxRAM memory devices can be used for synaptic plasticity functions with respect to variability. The conductance modulation of the OxRAM cell is demonstrated (i) by controlling the voltage applied across the cell during a RESET (RST) operation or (ii) by controlling the current flowing through the cell during a SET operation. In Section 2, OxRAM technology is introduced along with the basic concepts of memristor-based neural networks. In Section 3, the test chip considered for measurement is presented and characterized. In Section 4, the conductance modulation capability of the OxRAM technology is evaluated experimentally versus different programming conditions and discussed. Finally, Section 5 concludes the paper.

2. Background

2.1. OxRAM Technology

An OxRAM memory cell consists of two metallic electrodes that sandwich a thin dielectric layer serving as a permanent storage medium. This Metal-Insulator-Metal (MIM) structure, denoted as RRAM in Figure 1a, can be easily integrated in the BEOL on top of the CMOS subsystem. The MIM structure is integrated on top of the Metal 4 copper layer (Cu). A TiN Bottom Electrode (BE) is first deposited. Then, a 10 nm-HfO_2/10 nm-Ti/TiN stack is added to form a capacitor-like structure [16]. Figure 1b shows the basic 1T-1R memory cell schematic where one nMOS transistor (W = 0.8 µm and L = 0.5 µm) is connected in series with an OxRAM cell. Figure 1c presents a typical 1T-1R OxRAM I-V characteristic in logarithmic scale. Based on the I–V curve, the memory cell operation can be seen as follows: after an initial electro-FORMING (FMG) step [17], the memory element can be reversibly switched between the Low Resistance State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T-1R cell (Table 1), i.e., V_{SET} to switch to LRS and V_{RST} to switch to HRS. In the 1T-1R configuration, the transistor controls the amount of current flowing through the cell according to its gate voltage bias. The maximum current allowed by the select transistor is called the compliance current and is referred to as I_C in Figure 1c. The compliance current I_C controls the LRS resistance value in the SET state as well as the maximal RST current I_{reset}.



(**a**) (**b**) (**c**)

Figure 1. (**a**) TEM cross-section of an OxRAM device; (**b**) symbol view of a 1T-1R cell; (**c**) OxRAM I–V characteristic in log scale.

Table 1. Standard operating voltages (cell level, presented in Figure 1b).

	FMG	RST	SET	READ
WL	2 V	2.5 V	2 V	2.5 V
BL	3.3 V	0 V	1.2 V	0.1 V
SL	0 V	1.2 V	0 V	0 V

Table 1 presents the different voltage levels used during the different operating stages. Note that the FMG step, achieved once in the device life, is a voltage-induced resistance switching from an initial virgin state with a very high resistance to a conductive state, and that high voltages are typically needed during FMG [17].

2.2. OxRAM as Synapses

The synapse is a crucial element in biological neural networks, but a simple electronic equivalent is not possible, thus, complicating the development of hardware that reproduces biological architectures [18]. However, the recent progress in the experimental realization of memristive devices has reinforced the interest in ANNs as these devices have the ability to mimic brain synapses. Memristive devices, especially OxRAMs, have demonstrated the ability to be used as a synapse within hybrid analog circuits [17,18]. Indeed, since the conductance of OxRAMs can be electrically and incrementally increased or decreased [11], it is a potential candidate for realizing an electronic equivalent of a biological synapse. In a neural network context, OxRAM devices can act as synaptic weights to store information and process input signals.

2.3. Neuromemristive Systems

Neuromemristive systems are based on a design approach with closely coupled resistive memory and processing, resulting in high area and energy efficiency [19]. The neuromemristive network topology that has been mostly investigated in the literature is the fully connected neural network [20]. In this configuration, each neuron [8] of a layer is connected to every neuron of the previous layer. For simplicity, a two-layer, fully connected neural network, presented in Figure 2a, is considered. It is a feed-forward network that can be used to make classification tasks based on a linear predictor function combining a set of weights W_{ik} with the input vector X_i. Outputs Y_k are computed by implementing a vector–matrix multiplication as shown in Equation (1).

$$Y_k = \sum_{i=1}^{n} W_{ik} \cdot X_i \quad 1 < k \leq m \tag{1}$$

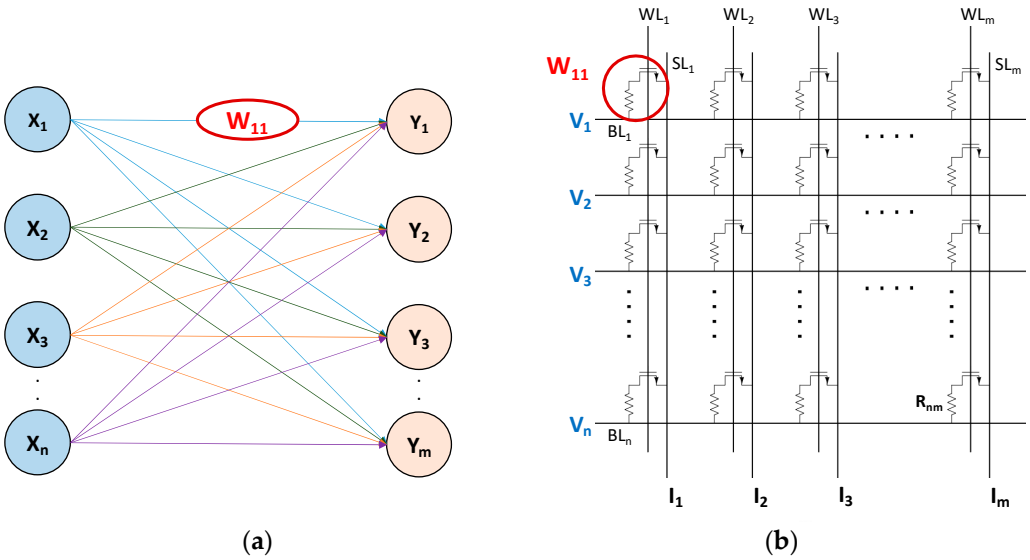


Figure 2. (**a**) Two-layer feed-forward neural network; (**b**) matrix–vector multiplication in a 1T-1R OxRAM array.

The output layer Y_k can represent class scores in classification applications [12]. An array of OxRAM cells could naturally accomplish matrix–vector multiplications within one step by collecting the accumulative output current of the array. This approach has been fully demonstrated experimentally in [21] using 1T-1R arrays for pattern recognition with metal-oxide resistive devices. Figure 2b describes how the neural network can be mapped to a 1T-1R array of OxRAMs. The cells in a row are organized by connecting the transistor sources to the Source Line (SL) and connecting transistor gates to the same Word Line (WL), while the cells in a column are organized by connecting the top electrode of the resistive memory to the Bit Line (BL). Input vectors (X_x) are mapped to input voltages (V_x) and weight matrix (W_{ik}) is mapped to memory cell resistance values R_{ik}, assuming that the ON state resistance of select transistors can be neglected compared to the OxRAM cell resistances. This structure can implement a vector–matrix multiplication as shown in Equation (2).

$$I_k = \sum_{i=1}^{n} \frac{1}{R_{ik}} \cdot V_i \quad 1 < k \leq m \tag{2}$$

The weighted sum is obtained by measuring the total current I_k and applying an activation function (not presented here) to the total current. The key point of this approach is the ability of the OxRAM cell to provide multiple resistance values. Indeed, before performing a vector–matrix multiplication (inference stage), different weights are loaded into the matrix. During weight loading, each OxRAM is programmed to a specific conductance value to reflect the targeted weight. In this context, the primary objective of this paper is to evaluate the conductance modulation capability of OxRAM devices.

3. Test Chip Presentation

3.1. T-1R Memory Array Architecture

Figure 3a presents the memory array considered for measurements, which is basically a classical 1T-1R array. Memory cells are grouped to form eight 8-bit memory words. Word Lines (WL_X) are used to select the active row, Bit Lines (BL_X) are used to select active columns during a SET operation, and Source Lines (SL_X) are used to RESET a whole memory word or an addressed cell. To allow a full flexibility during characterization, BL, WL, and SL nodes are externally available.

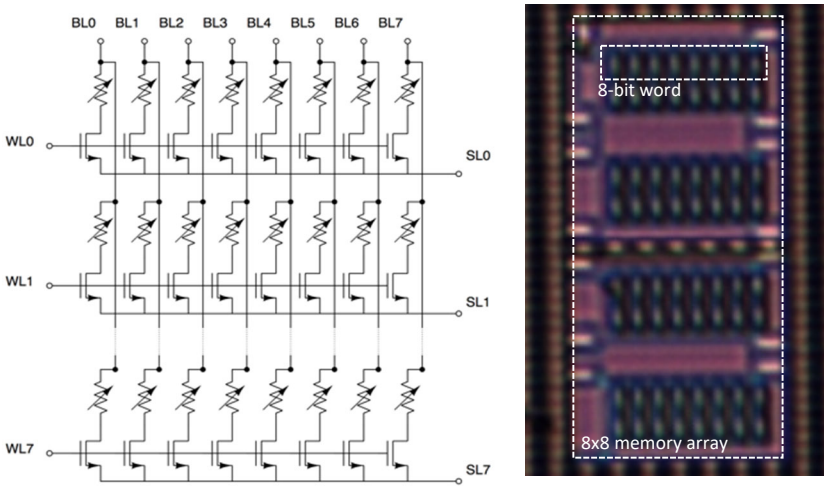


Figure 3. (**a**) 8 × 8 OxRAM memory array and (**b**) corresponding micrograph of the memory array test chip fabricated in a 130 nm CMOS technology.

Figure 3b presents a view of the memory array. Due to the limited pin out of the probe card used in the experimental phase, only a 7 × 7 memory array is available for our experiments (subset of the 8 × 8 array).

3.2. Experimental Setup

Figure 4 describes the experimental setup, which is based on a Keysight B1500 semiconductor parameter analyzer. The studied structure is embedded on an 8-inch wafer, connected to the B1500 through a probe card and a low-resistance switching matrix Keithley 708A. The matrix connects the Source/Measure Units (SMUs) to the memory array pads during the FMG, SET, RST, and READ operations. All the experiments are conducted through Python programs, controlling the equipment.

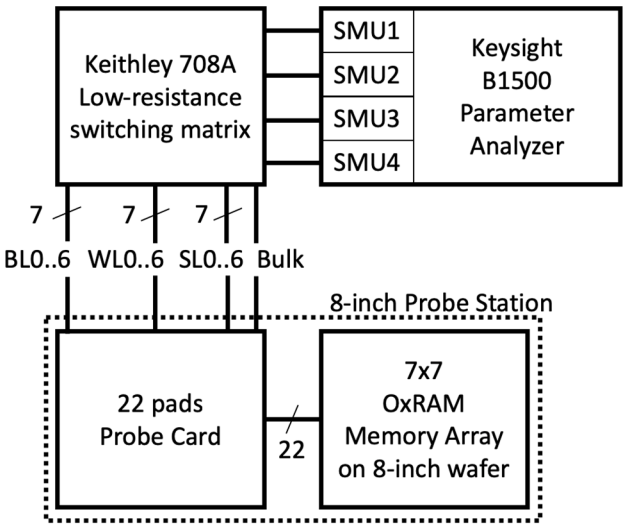


Figure 4. Experimental setup used for the memory array characterization.

3.3. Preliminary Experimental Results: Variability Analysis

Although OxRAM-based devices have shown encouraging properties, challenges remain, among which device variability (or reproducibility) is the main [22]. In fact, variations of R_{HRS}. and R_{LRS} can be so unpredictable that they have been employed as an entropy source in True Random Number Generators (TRNG) [23,24]. Indeed, the variance from cycle to cycle (C2C) and from device to device (D2D) can be very large,

directly impacting the memory cell HRS and LRS resistances. This inherent drawback of the technology has to be investigated to assess the multiple resistance levels capability of the considered OxRAM technology. To highlight the impact of variability on HRS and LRS resistances, a set of preliminary measurements are conducted. Before any SET/RST operations, the memory array is first formed. Then, memory cells are RST one by one to extract their HRS resistance. After RST, cells are SET to extract their LRS resistance. Figure 5 shows the cumulative probability plots obtained after 500 consecutive RST/SET cycles applied to the memory array (500 × 49 cells). As the same memory array is programed 500 times, both D2D and C2C variabilities are captured. A 0.1 V READ bias voltage is used to extract R_{LRS} and R_{HRS} distributions. Figure 5 shows that variability has a huge impact on HRS and LRS resistances. The HRS distribution spread is more pronounced compared to the LRS spread, which is a common feature of OxRAM technologies [25]. These experimental results clearly indicate that the variability of the OxRAM technology needs to be accounted to implement multilevel cell operations.

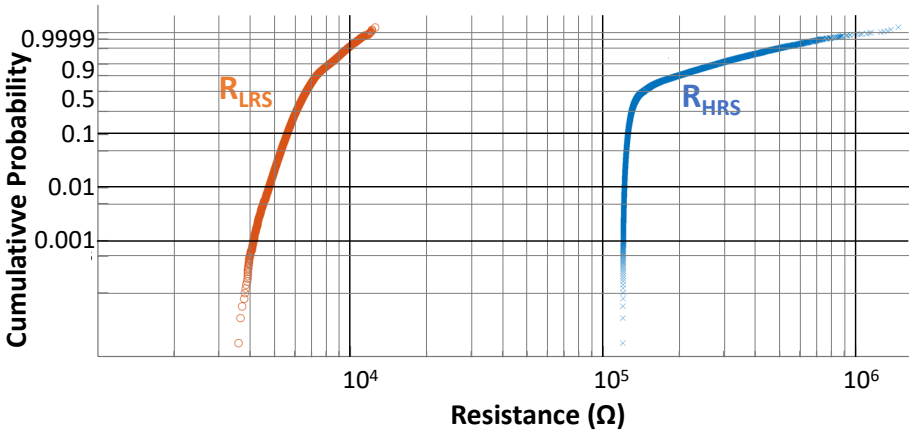


Figure 5. HRS and LRS resistance distribution measurement results after cycling the memory array 500 times.

4. OxRAM Conductance Modulation

To modulate the OxRAM conductance, the following two methods are commonly used: (i) controlling the maximum voltage during the RST operation [26] and (ii) changing the compliance current during the SET operation [27]. Indeed, the RST operation is a voltage dependent process, whereas the SET operation is a current controlled process [27]. An alternative method consisting in varying the pulse width of RST/SET voltages is also employed [28] but is not considered in this study.

4.1. Reset Voltage Control

In this approach, OxRAM conductance modulation is obtained by controlling the maximum RST voltage. To program the memory cells and precisely track the HRS resistance change, 1 ms DC staircase voltage sweeps are used. A strict measurement protocol, depicted in Figure 6a, is used. Memory cells are first RST (RST_1) at 1.8 V to start from a fresh HRS state. The RST operation is followed by a SET operation to reach the LRS state. After that, a second RST operation (RST_2) with a variable maximum voltage V_{stop} is applied across the cells. V_{stop} ranges from 0.6 V to 1.75 V and increases by a 0.05 V step in each iteration, resulting is 24 different maximum V_{stop} voltages. For each iteration, the HRS resistance change is measured during a READ operation at 0.1 V. In Figure 6b, I–V characteristics are presented for a single cell located in the center of the elementary memory array (this is an arbitrary choice as no significant behavior changes have been reported according to the cell position in the array during RST end SET operations). I–V curves are obtained after applying the above-mentioned RST_1-SET-RST_2 programming sequence with an arbitrary value of V_{stop} = 1.1 V. We can see that the cell starts from an intermediate RST state before

the first RST_1 operation, which results in a narrow hysteresis (black curve 1). From the resulting initial HRS state (170 kΩ), a SET operation (blue curve 2) brings the cell in the LRS state (8 kΩ). Finally, a "weak" RST operation, with V_{stop} = 1.1 V is applied to bring back the cell in an intermediate final HRS state (red curve 3). Indeed, as V_{stop} is clamped to 1.1 V, the RST process is not fully completed, leading to an intermediate HRS resistance level (80 kΩ). Note that no compliance current is set during the SET operation to only consider the impact of a variable maximum RST voltage on the final HRS resistance.

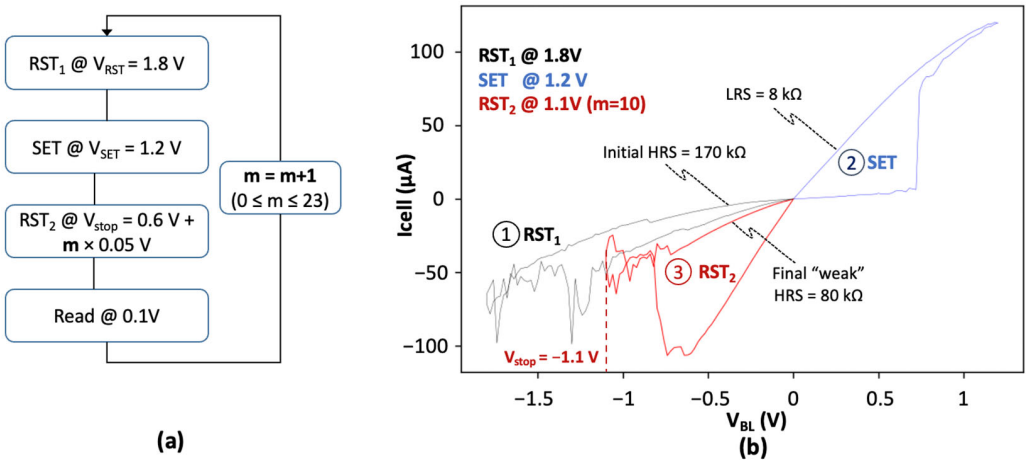


Figure 6. (**a**) R_{HRS} conductance modulation measurement protocol and (**b**) resulting I–V curves.

Results presented in Figure 6b are actually impacted by variability. C2C variability is clearly visible in Figure 7a where the programming sequence is repeated 10 times for an isolated cell (10 I–V hysteresis superimposed for V_{stop} = 1.1 V). In Figure 7b, D2D variability is demonstrated by applying the programming sequence one time to each cell of the memory array (49 I–V hysteresis superimposed for V_{stop} = 1.1 V). In Figure 7c, both C2C and D2D variabilities are captured after applying the programming sequence 10 times to the whole memory array.

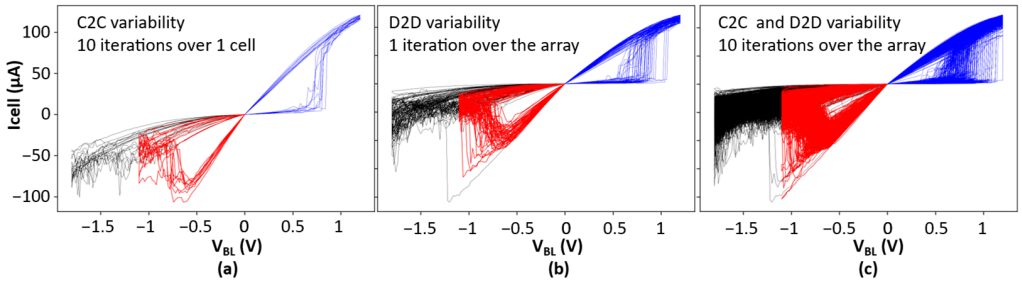


Figure 7. I–V curves extraction after the RST_1-SET-RST_2 operation highlighting (**a**) C2C variability, (**b**) D2D variability, and (**c**) both C2C and D2D variability.

D2D variability is confirmed in Figure 8a–c bitmaps, extracted after RST_2 operation for 3 different V_{stop} values (0.6 V, 1.1 V, and 2 V). Resistance values are represented by a color gradient from white (for the highest resistance values) to black (for the lowest resistance values). For V_{stop} = 0.6 V, the resistance window is [5.8–13 kΩ], with an average value of 7.5 kΩ. For V_{stop} = 1.1 V, the resistance window increases to [30–180 kΩ], with an average value of 88 kΩ. The resistance window is even more increased for higher V_{stop} values: the deeper we enter the HRS state, the higher the variability [27]. For V_{stop} = 1.6 V, a resistance window of [92–496 kΩ] is measured, with an average value of 237 kΩ.

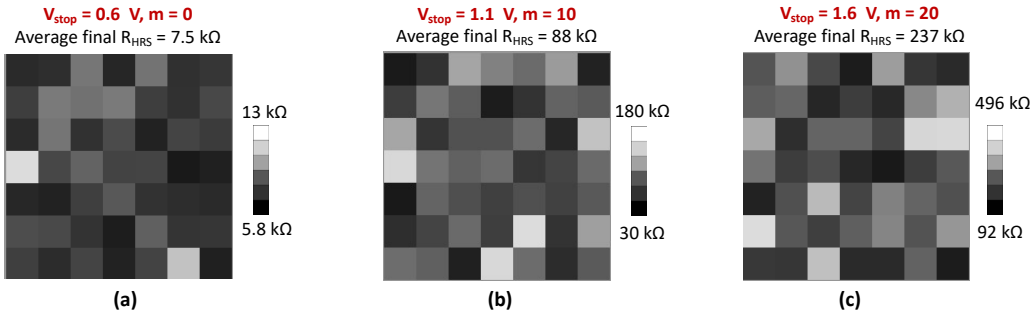


Figure 8. R_{HRS} bitmaps extraction after RST_2 operation for 3 different V_{stop} values: (**a**) V_{stop} = 0.6 V; (**b**) V_{stop} = 1.1 V et; (**c**) V_{stop} = 1.6 V.

The evolution of the HRS resistance versus V_{stop} is presented in Figure 9a (V_{stop} ranging from 0.6 V to 1.75 V). We can see that R_{HRS} evolution is not a monotonically increasing function of V_{stop} and shows some resistance drops (blue curve). However, if we consider a subset of the measurements (dot point of the red dashed curve), a monotonically increasing function can be obtained. In Figure 9b, the non-monotonic evolution of R_{HRS} versus V_{stop} is confirmed for 5 different cells of the array.

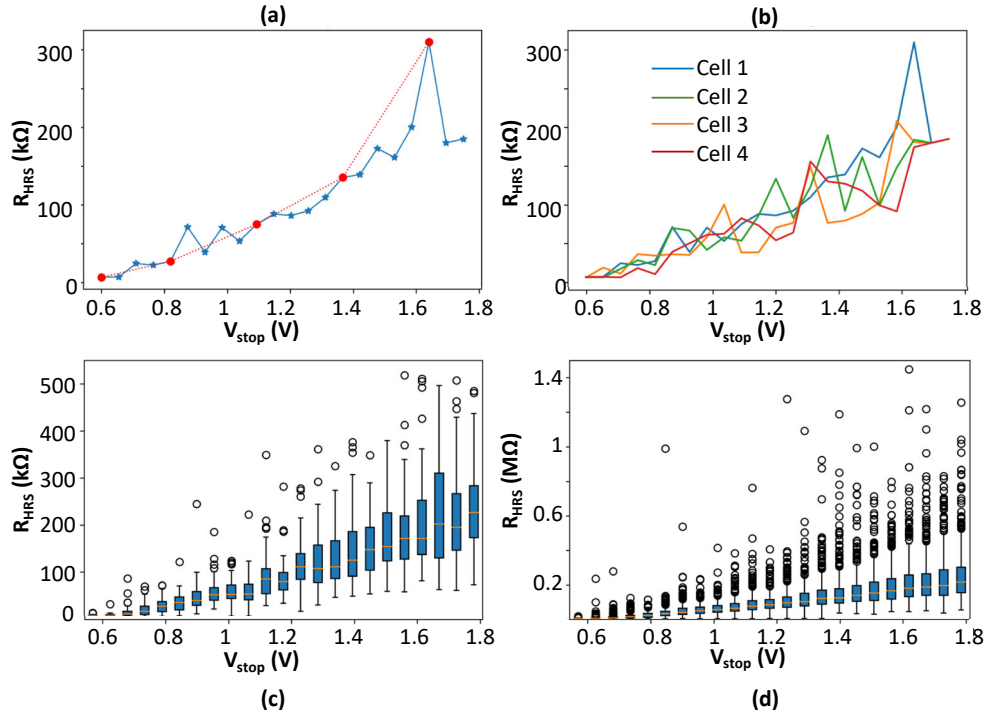


Figure 9. (**a**) R_{HRS} vs. V_{stop} steps for an isolated cell (center of the array). (**b**) R_{HRS} vs. V_{stop} steps for 4 isolated cells. (**c**) R_{HRS} box plots vs. V_{stop} steps. Each box plot gathers 49 measurements (D2D). (**d**) R_{HRS} box plots vs. V_{stop} steps. Each box plot gathers 490 measurements (D2D and C2C). The circles represent outliers showing the strong variability.

A statistical analysis of the HRS resistance distribution was also conducted. For each V_{stop} value, the measurement protocol of Figure 6a is applied to each cell of the 7 × 7 memory array to catch the D2D variability and repeated 10 times for the whole array to catch the C2C variability. Figure 9c shows a box plot representation of R_{HRS} versus V_{stop} steps for all the memory array cells (49 measurements for each V_{stop} step). In Figure 9d, box plots are related to the same memory programmed 10 times for each V_{stop} step value (49 × 10 measurements). Interestingly, for this latter case, a smoothing effect alleviates the

effect of the variability: the evolution of the median value of R_{HRS} versus V_{stop} is turned monotonic (i.e., the median R_{HRS} value strictly increases with increasing V_{stop} values).

Based on Figure 9 measurement results, it clearly appears that variability of the technology is a key parameter to consider in order to use OxRAMs in an ANN context: the impact of variability on the ANN parameters, such as accuracy, need to be checked against the variability of the OxRAM technology.

4.2. Compliance Current Modulation during SET

Another approach to achieve conductance modulation is to change the compliance current (I_C) during the SET operation. Indeed, it has been demonstrated that the final cell resistance is a function of the maximal current allowed through the cell [29,30]. In the considered 1T-1R configuration, the SET current can be controlled by varying the voltage applied to the gate of the transistor, referred to as V_{WL} (see Figure 1b). The measurement protocol is depicted in Figure 10a. Memory cells are first RST to start from a fresh HRS state. The RST operation is followed by a SET operation with a variable V_{WL} voltage ("weak" SET) to reach the LRS state. V_{WL} ranges from 1 V to 2 V and increase by a 0.1 V step in each iteration, resulting in 11 different V_{WL} voltages ('m' ranging from 0 to 10). For each iteration, the LRS resistance change is measured during a READ operation at 0.1 V. Figure 10b shows the impact of 3 different V_{WL} voltages (1 V, 1.5 V, and 2 V) on an isolated OxRAM cell. When V_{WL} increases, the maximum current allowed through the cell increases, resulting in 3 different LRS levels (13 kΩ, 15 kΩ, and 34 kΩ), whereas the HRS resistance remains in the same range (approximately 300 kΩ).

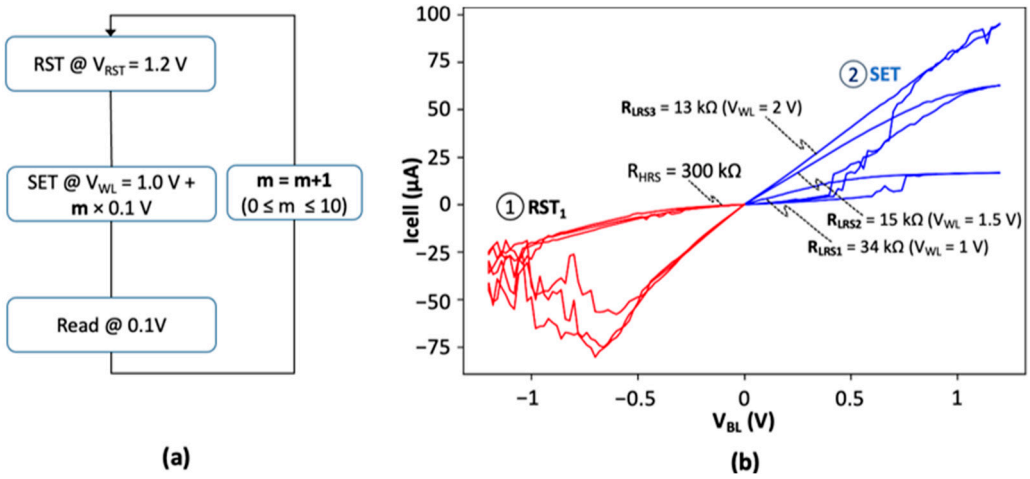


Figure 10. (**a**) R_{LRS} conductance variation measurement protocol and (**b**) R_{HRS} vs. V_{WL} for 3 different V_{WL} values (1 V, 1.5 V and 2 V).

The evolution of the LRS resistance versus V_{WL} voltage is presented in Figure 11a for the 11 pre-defined V_{WL} values and by considering 4 different cells. Figure 11a shows that R_{LRS} evolution is not a monotonic function of V_{WL}. However, resistance drops are less pronounced compared to the RST voltage control approach (see Figure 9b).

A statistical analysis of the LRS resistance distribution was also conducted. The measurement protocol of Figure 10a is applied to each cell of the 7 × 7 memory array to catch the D2D variability. Figure 11b shows a box plot representation of R_{LRS} versus V_{WL} voltage for all the memory array cells (49 measurements for each V_{WL} step). We can observe that the higher the select transistor gate voltage, the lower the resistance after SET. Moreover, when the maximal allowed current decreases, the resistance values are more spread. Conversely, when the current limitation is high, all the cells are correctly SET, resulting in tight distributions [31]. A region of resistance variation has been identified (between 12.5 kΩ and 40 kΩ, see Figure 11a,b) where the conductance modulation in the

LRS state can be exploited. Beyond this resistance range, the resistance variation slope is too important to consider conductance modulation.

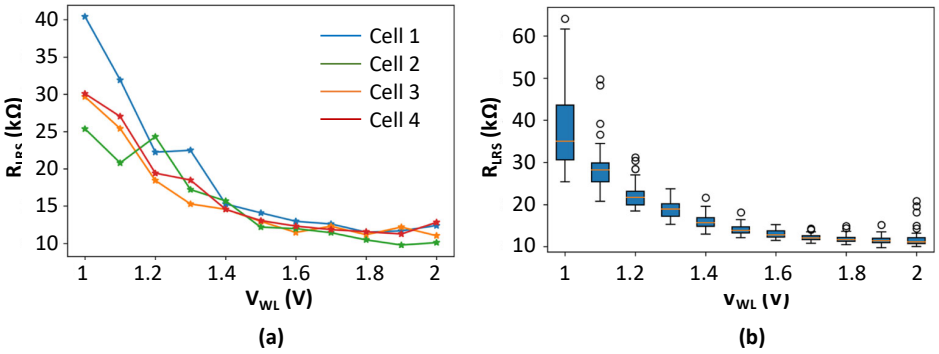


Figure 11. (**a**) R_{LRS} versus V_{WL} for 4 different cells and (**b**) R_{LRS} box plots versus V_{WL} voltage steps. Each box plot gathers 49 measurements.

4.3. Discussion

In both RST voltage and compliance current control approaches, the idea was to define a relationship between the RST voltage or the SET compliance current, on the one hand, and the HRS or LRS resistances on the other hand. LRS and HRS resistance variations were required to follow a monotonic variation to confidently implement the proposed conductance modulation strategy in a neuromorphic computing system. However, we have demonstrated that the variability of the technology results in uncontrolled resistance changes.

At the OxRAM device level, the conductance modulation strategy can be seen as a segmentation of the I–V plane by several I–V characteristics, as shown in Figure 12. For clarity, only eight different characteristics are considered. Each characteristic is associated with a single conductance resistance state and has a slope of $G_x = 1/R_x$, where x is the number of HRS/LRS states ranging from 0 to n. The precision required in the conductance modulation operation is not only limited by the programming operation; it is also necessary to develop an accurate and robust READ mechanism. The READ operation is typically implemented by applying a low bit line voltage to the memory cell select transistor (V_{Read}), and resulting currents (I_0 to I_n) are sensed to reflect the memory cell conductance value [32]. Although multiple resistance levels can be easily obtained using the above-mentioned programming methods (i.e., RST voltage and SET current control), the successful implementation of a reliable conductance modulation scheme mainly depends on the ability to precisely control the conductance margin between two conductance levels. Indeed, various factors, including variability in the first place, can degrade the conductance margin and eventually lead to I–V characteristic overlaps. In order to take into account the variability of the n resistance states, the conductance margin ΔG is represented in Figure 12 by the shaded area encompassing each characteristic. Hence, it clearly appears that the variability parameter is the key parameter to consider to achieve a reliable conductance modulation strategy.

In the next analysis, the standard deviation metric is used to track the HRS and LRS variability. Figure 13a shows the evolution of the HRS distribution standard deviation σ_{RHRS} versus the RST voltage. The standard deviation is related to box plot distributions presented in Figure 9c. We can see that the standard deviation evolution follows a trend close to a linear law: HRS standard deviation is more pronounced for high V_{stop} values, which is associated with important HRS values. When normalized with respect to the mean HRS distribution value μ_{RHRS}, the coefficient of variation (σ/μ ratio) evolution is turned constant for high enough V_{stop} values (>0.8 V, see Figure 13b). Figure 13c shows the evolution of the LRS distribution standard deviations versus the V_{WL}. Here, standard derivations are related to box plot distributions presented in Figure 11b. In this case, LRS standard deviation is a strong function of V_{WL} and increases exponentially with decreasing V_{WL} values. When normalized with respect to the mean LRS distribution value μ_{RLRS}, the

σ/μ ratio evolution keeps its exponential behavior (Figure 13d), making the R_{LRS} variability difficult to control for low V_{WL} values. To mitigate the dependence of the variability on the programming conditions (i.e., programming voltages or select transistor gate voltage), a workaround would be to leave sufficient margin between the memory states (HRS or LRS) more impacted by variability. In practice, the idea would be to increase V_{stop} steps for increasing V_{stop} voltages, or to increase V_{WL} steps for decreasing V_{WL} voltages. Indeed, to obtain a monotonic variation of R_{HRS} (resp. R_{LRS}) versus V_{stop} (resp. V_{WL}), V_{stop} (resp. V_{WL}) steps have to be carefully chosen to avoid unwanted resistance variations, as shown in Figure 9a.

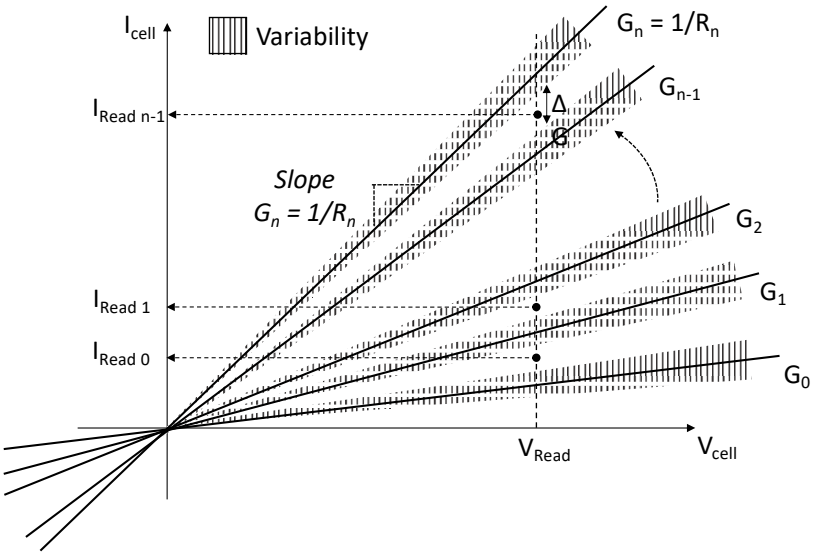


Figure 12. I–V plane segmentation and subsequent READ operation after the memory cell programming operation. The cell is read at V_{Read}, and different currents are sensed to reflect the memory cell conductance value.

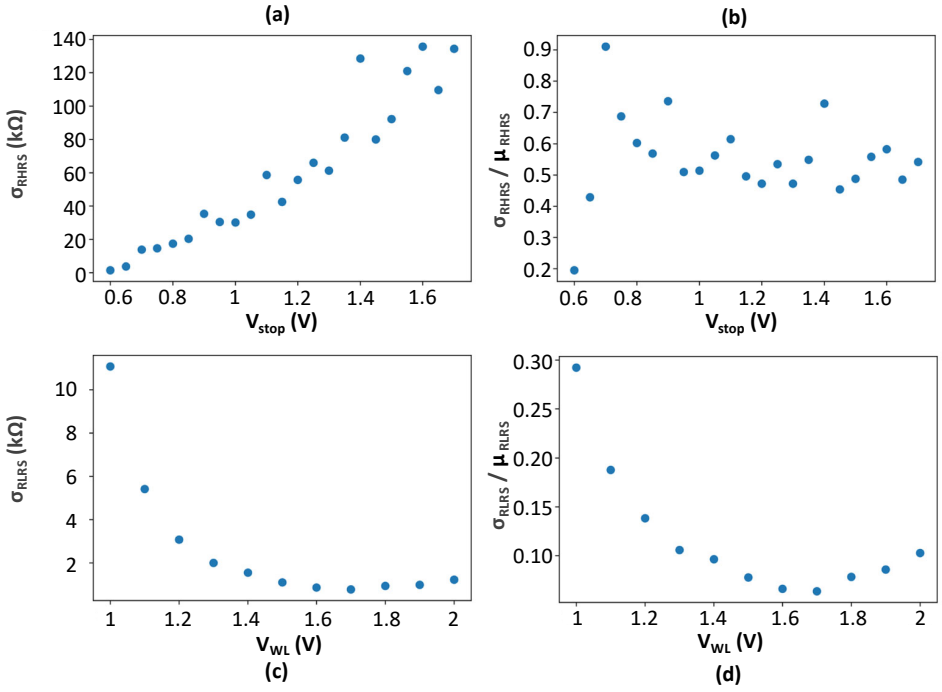


Figure 13. (**a**) HRS standard deviation versus V_{stop} voltage steps and (**b**) σ/μ ratio variation versus V_{stop}. (**c**) LRS Standard deviation versus V_{WL} voltage steps and (**d**) σ/μ ratio variation versus V_{WL}.

5. Conclusions

In the past few years, neuromemristive systems based on the emerging resistive memories have made notable progress. However, the research on the ability of a resistive device to emulate a synapse is still in its early stage. In this context, this paper assesses the capability of OxRAM devices to achieve multilevel cell operations. The study targets two programming techniques: (i) RST voltage control and (ii) SET current control. Experimental results show that both techniques provide conductance levels highly impacted by variability, making the strict control of OxRAM conductance difficult in an ANN context. The RST voltage control approach shows high variability. However, the variability remains constant with respect to the median value of the HRS distributions. The SET current control approach shows more contained variability. However, in this approach, the variability grows exponentially with respect to the median value of the LRS distributions.

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