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# Comparison of losses in different topologies of step-up/step-down inverters

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## Keywords

« Uninterruptible Power Supply (UPS) », « Device modeling », « Efficiency », « Simulation », « Estimation technique »

## Abstract

Standard Voltage Source Inverters (VSI) operates with a DC voltage source greater than the peak voltage of the AC source and Current Source Inverters (CSI) with a DC voltage source lower than the peak voltage of the AC source. This paper shows how several topologies of reversible AC/DC buck-boost inverters which do not suffer from such constraints can be compared on the basis of semiconductor and inductor losses. The main quantities in these converters, such as average current, RMS current, etc. are derived from an analytical analysis and they are combined to semiconductor loss models to derive losses and efficiency of each topology for different working conditions.

## Introduction

Uninterruptible Power Supply (UPS) protect critical loads by giving them a stable supply, shielding them from perturbations. Several architectures of UPS are available as commercial products: (on-line, off-line, DC, etc...). This paper focuses on off-line UPS (Fig. 1); the efficiency from line to load is optimal because connection is almost direct, and from battery to load it is also very good because unlike other UPS configurations, power flows through a single converter. Such a UPS mainly consists of a reversible AC/DC converter.

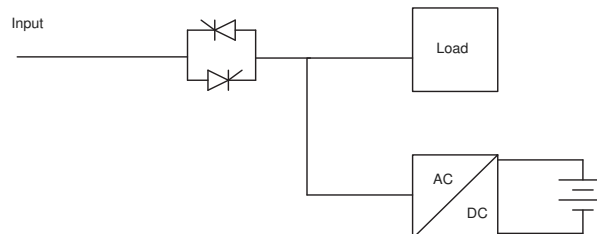


Figure 1 : Typical off-line configuration

When standard voltage source inverters (resp. current source inverters) are used, the DC voltage must be greater (resp. lower) than the peak value of the line voltage, and accounting for crossed variations of these sources (low/high line and accounting for 0 to 100% depth of discharge) makes this condition an important constraint. It becomes even worse when the same UPS is designed

for an international market and must be made compatible with different line voltages lying between  $250V_{RMS}$  and  $525V_{RMS}$  and a DC bus voltage imposed by the battery varying between  $396 V_{DC}$  and  $568V_{DC}$ .

Therefore, the goal of this paper is to find the best buck-boost inverter topology able to operate on a wide range of voltage. Semiconductor and inductor losses will be used as the main criteria for this comparison. We chose to neglect the capacitor losses in front of the other losses.

## Topology

In this paper we will first analyze and compare the SC losses of the three topologies illustrated in Figures 2, 3 and 5. These topologies have already been described in the literature so we will only present here a quick explanation of their operation and control.

The first converter is the combination of an AC chopper [1] and a voltage source inverter [2] as illustrated in (Fig. 2). When the input voltage ( $V_i$ ) is greater than the output voltage ( $V_o$ ) the voltage source inverter is saturated and the chopper is switching, if  $V_i$  is less than  $V_o$  the chopper is saturated and the inverter is switching.

The topology in Fig. 3 can be seen as a 5-level voltage source inverter (boost) followed by a step-down chopper (buck), but it also provides a direct path from line to battery when the line voltage is less than the battery voltage (the chopper is used only when the line voltage is greater than the battery voltage to maintain a constant voltage  $V_{dc}$  of 894V), see [3] for more details.

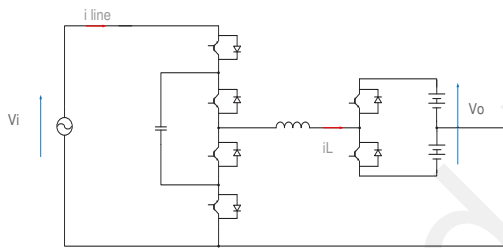


Figure 2 : AC/DC voltage-source inverter + AC/AC chopper

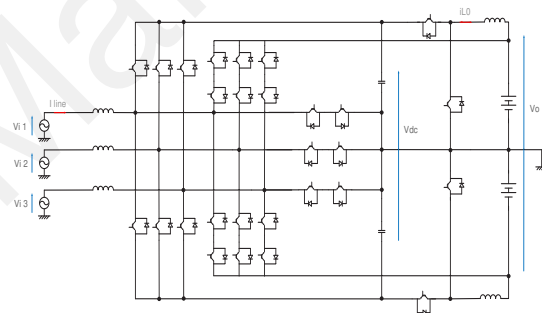


Figure 3 : 5 level Chopper + inverter

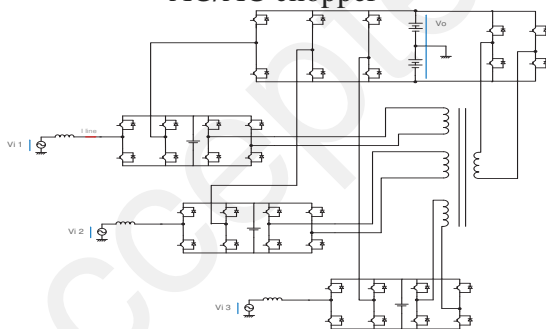


Figure 4 : Full schematic of H-Bridge and inverter

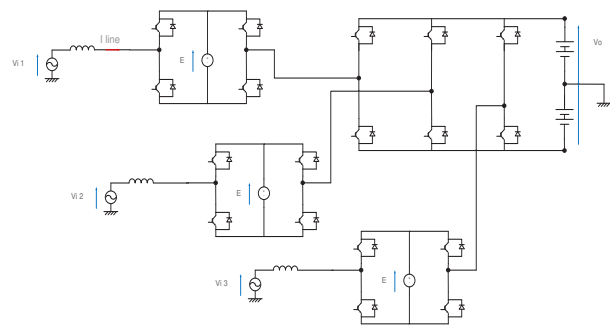


Figure 5 : simplified schematic of H-Bridge and inverter

A third topology illustrated in Figure 4 was studied in [4]. We can decompose it in two parts; the first part is composed of three H-bridge converters and a three-phase inverter, the H-bridges are used to generate a voltage level greater than the peak input voltage when the output voltage is too low. The second part of the converter uses H-bridges and a transformer to control the input H-bridge capacitor voltage.

In order to simplify the model and its control we chose to replace the input capacitor H-Bridge by a constant voltage supply which depends on the operation point ( 1) and to consider that the second part has an efficiency of 97.5%, which gave us the schematic in Figure 5.

$$E = 1.2 \left( \hat{V}_i - \frac{V_o}{2} \right) \quad (1)$$

## Method of study

For this study we first apply an analytic approach by developing the equations of the average values of the state variables (inductor currents and capacitor voltages) of each topology. To provide meaningful insight on the operation and design of these buck–boost converters, the power factor must be taken into account in this analysis. As a second step, the average and RMS currents in the switches must be determined to calculate conduction losses and the characteristic quantities of the voltages and currents of all switches must be determined to derive switching losses. These quantities result of both the variation of state variables and the modulation of duty cycle and make analytic study quite complex.

To avoid this we use a hybrid approach. Analytic equations are used to drive simplified Simulink simulations. The input and output voltages are imposed to describe a given point of operation, the appropriate open-loop control pattern and the average values of state variables determined by the analytical model are imposed via controlled sources. For example, in case of the chopper-inverter converter the schematic for Simulink is as shown in Figure 6.

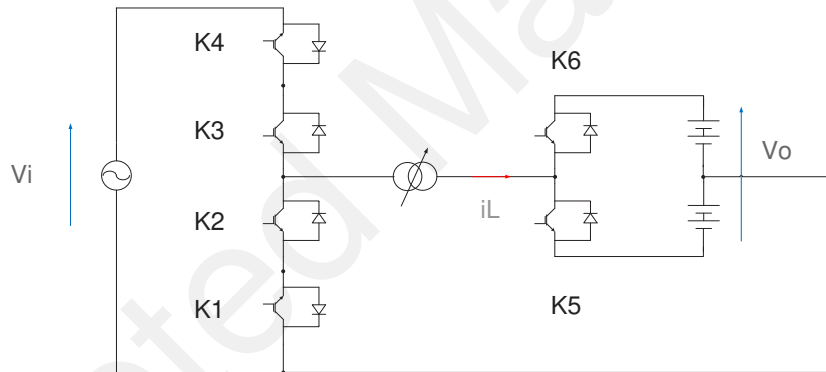


Figure 6 : Simplified Simulink model of the AC/DC voltage-source inverter + AC/AC chopper

Simulink is run to generate the voltage and current waveforms of all switches and the voltage slope and the low frequency current of the inductance (imposed by the power to be converted and the input voltage). Then the waveforms are sent and processed in Matlab to obtain the characteristic quantities (average, RMS and sampled at switching times) of all components and allow determining the constraints for each of them at all points of operation. Then, the inductors are designed and their cost is estimated, and for each switch a semi-conductors withstanding the maximum voltage and current is selected and conduction and switching losses are derived.

This method simplifies the study of topologies and allows users to calculate the losses and constraints of most elements (SC, inductors) for each topology, point of operation and control strategy. It is thus possible to study multiple topologies and their response to frequency, power or phase variation under different working mode.

## Semiconductor

Our goal is to design a UPS addressing the requirements of an international market which means that it must be able to operate on 400V European or 480V American three-phase networks with a large tolerance leading to an operating voltage lying between  $250V_{RMS}$  and  $525V_{RMS}$ . The DC bus voltage is fixed by the battery and will vary between  $368V_{DC}$  and  $568V_{DC}$ .

Considering these voltages we think of using recent IGBTs with a voltage rating lying between 600V and 1200V to compare the losses in the different topologies. Other kind of component such as MOSFET could be used, but to simplify this study we chose to only calculate losses with IGBTs.

### Loss calculation

IGBT loss calculation was addressed in other papers such as [5] and [6] the main numerical calculation effort is to express the IGBT losses as a polynomial function of the current. The current ripple is neglected as previously described in [5] and the switching losses are calculated using the average value of the current over a switching period. Thus we can express the conduction losses over one period of modulation as:

$$P_{cond} = F_{sw} \int_0^{T_{mod}} (vi(t) + Ri(t)^2) dt \quad (2)$$

and the switching losses are expressed as shown in (3) where  $k$  represents the index of the commutation instants, and  $v_{swk}$  and  $i_{swk}$  the voltage and the current at the switching instants.

$$P_{sw} = \frac{F_{sw}}{V_{def}} \sum_k v_{swk} (A + Bi_{swk} + Ci_{swk}^2) \quad (3)$$

### Component

Different families of IGBT exist and each family is optimized for a specific application; a detailed analysis of conduction and switching losses allows choosing the most suitable IGBT for each switch position and optimizing the choice of the semiconductor technology.

All the parameters of the semiconductor models used in this study are obtained using the information provided in the datasheet and in order to complete our comparison we add to each semiconductor model a cost. This cost is calculated based on the nominal current of the component and their voltage rating. The 600 and 1200 volts components are given respectively a price of 0.0524 \$/A and 0.0916 \$/A (dollar per Ampere). The parameters of the semiconductor model used are summarized in Table I.

**Table I: S.C. model parameters**

reference	Component 1	Component 2	Component 3	Component 4	Component 5	Component 6
A	$8.378 \times 10^{-3}$	$-8.18 \times 10^{-6}$	0	$6.125 \times 10^{-6}$	$7.383 \times 10^{-3}$	$6.843 \times 10^{-4}$
B	$5.08 \times 10^{-5}$	$3.774 \times 10^{-5}$	$8.997 \times 10^{-5}$	$1 \times 10^{-5}$	$1.405 \times 10^{-4}$	$2.992 \times 10^{-5}$
C	$2.626 \times 10^{-8}$	$2.433 \times 10^{-7}$	0	$1.25 \times 10^{-7}$	$5.286 \times 10^{-8}$	$2.323 \times 10^{-6}$
Vt (V)	0.8	0.5	1	1.25	0.85	1.22
Rt ( $\Omega$ )	$1.48 \times 10^{-3}$	0.02	0.01	0.0114	$2.5 \times 10^{-3}$	$21.6 \times 10^{-3}$
$A_{rec}$	$2.236 \times 10^{-3}$	$4.562 \times 10^{-5}$	$2.003 \times 10^{-5}$	$2.003 \times 10^{-5}$	$10.09 \times 10^{-3}$	$3.63 \times 10^{-5}$
$B_{rec}$	$1.378 \times 10^{-5}$	$1.634 \times 10^{-5}$	$1.061 \times 10^{-5}$	$1.061 \times 10^{-5}$	$1.1 \times 10^{-4}$	$4.76 \times 10^{-6}$
$C_{rec}$	$-4.75 \times 10^{-9}$	$-8.72 \times 10^{-8}$	$-4 \times 10^{-8}$	$-4 \times 10^{-8}$	$-5.63 \times 10^{-8}$	$-3.91 \times 10^{-8}$
$V_d$ (V)	0.94	1.045	1	1	1	1.75
$R_d$ ( $\Omega$ )	$9.2 \times 10^{-2}$	$19.1 \times 10^{-3}$	$11 \times 10^{-3}$	$11 \times 10^{-3}$	$1.46 \times 10^{-3}$	$21.4 \times 10^{-3}$
$I_{nom}$ (A)	600	40	75	75	450	40
$V_{nom}$ (V)	600	600	600	600	1200	1200
$V_{def}$ (V)	300	400	400	400	600	600
Raw material Price (\$)	31.44	2.096	3.93	3.93	41.22	3.664

### Comparison with Psim simulation

In order to verify the SC losses obtained by this hybrid method we compared the results obtained with results given by the simulation tool Psim using the IGBT thermal module. This verification is made on the SC losses of the AC/DC voltage-source inverter + AC/AC chopper represented on the Figure 6 :. The semiconductors are chosen to respect the constraints imposed by operation at line voltage lying between  $250V_{RMS}$  and  $525V_{RMS}$ . The DC bus voltage is fixed by the battery and will vary between  $396V_{DC}$  and  $568V_{DC}$ ; a constant power of 125kW is assumed for the 3-phase converter.

To facilitate this comparison, the verification will only be for the performance at the nominal point of operation ( $400V_{RMS}$  and  $480V_{DC}$ .) Given the symmetry of the inverter and the electrical signal we consider only one phase and assume that losses in  $K_5$  and  $K_6$  are the same. The Psim model uses an inductance of  $150\mu H$  and is controlled by a PI regulator ( $I=220.10^{-6}$  and  $P=0.3$ ) and an anti-windup ( $K=100$ ).

Regarding the results presented in Table II we can observe a difference between the results of conduction losses, it is due to the difference of model:

- in Psim the thermal module uses the characteristics given by the manufacturer,
- in Matlab we use a polynomial approach which tend to overestimate the conduction losses for the low current.

For the switching losses the difference is due on the one hand to the fact that Psim uses the instantaneous turn-on and turn-off currents while we use the average current in the model and on the other hand to the polynomial representation of the variation of the switching energy vs current. It can be seen that the maximum error between the two methods correspond to an overestimation of 13.9% (5.2W) which seem reasonable given the difference in the calculation method.

**Table II: Comparison of Matlab and Psim results**

name	Component	Method	Transistor		Diode	
			Conduction [W]	Switching [W]	Conduction [W]	Switching [W]
K1	Component 1	Matlab	16.8	0	17.2	13.7
		Psim	16.2	0	15.5	13.9
		Error %	-3.7	0	-10.9	1.43
K2	Component 1	Matlab	17.7	0	16.4	13.7
		Psim	16	0	15.5	14.1
		Error %	-10.6	0	-5.81	2.84
K3	Component 1	Matlab	94.4	60.1	94	0
		Psim	92.7	63.8	91.2	0
		Error %	-1.83	5.8	-3.07	0
K4	Component 1	Matlab	93.5	60.1	94.8	0
		Psim	92.3	62.3	91.2	0
		Error %	1.3	3.53	-3.95	0
K5	Component 5	Matlab	4.54	46.8	125	42.7
		Psim	4.65	53.1	119	37.5
		Error %	2.36	11.9	-5.04	-13.9

### Inductor design and cost estimation

In order to better compare the different topologies the losses in the inductors and their price cannot be neglected. But to determine these criteria a full design process must be implemented to determine the numbers of turns and strands, the geometry and the characteristic dimensions of the core. A simplified design method for toroidal inductance based on [7] and [8] allows using an analytical model to describe the behavior of the magnetic material for a given design and point of operation.

### Constraints

Independently of the topology we chose to limit the high frequency current ripple equal to 20% of the peak value of the low frequency current (*high frequency* means the switching frequency or a multiple of the switching frequency when interleaved control is used, and *low frequency* means the grid frequency i.e. typically 50 or 60Hz). In some cases calculation of the maximum current ripple to determine the required inductance is not trivial; a first Matlab calculation is made to first estimate the

current ripple for a given inductance, then a proportionality rule is applied to obtain a better estimate of the desired inductance value to respect the chosen current ripple constraint.

By using Matlab we can determine, for each point of operation and each topology, the minimum inductance value, the maximum current value and the RMS current in each inductor. Then the number of strand is determined considering the maximum RMS current, the prescribed RMS current density and a given strand diameter. This determination of the number of strand is simple and does not take into account the frequency dependence of the resistance of the winding.

Magnetic core manufacturers generally give the standard dimensions of cores [8] to help the design of inductors. In the method presented below we chose to not use these discrete dimensions to design inductors, and to allow continuous variations of the core dimensions. But to make sure that the design is realistic we specify maximum values for the inner and outer diameters (corresponding to the biggest toroidal core in [8]), and for the fill factor. Based on the maximum inner diameter, a maximum value of the number of turns is derived from the prescribed fill factor and current density. The maximum values of the RMS current and peak current and the minimum required inductance are then used to design the inductors of each topology so they match the requirements over all points of operation.

### Loss calculation

In order to do a quick comparison of the losses in the different topologies we chose to simplify the calculation of conduction losses in the windings by only considering the losses generated by the DC resistance of the winding at 90°C.

$$P_{winding} = R_{dc} \times I_{rms}^2 \quad (4)$$

The core loss density is calculated using a Steinmetz model [7]

$$P_{core} = \left( \frac{\hat{B}}{2} \right)^{cp_1} (cp_2 f + cp_3 f^{cp_4}) \quad (5)$$

### Design method

We previously explained the determination of the characteristic value, loss calculation and the determination of the maximum number of turns; we will now detail the method corresponding to the algorithm described in Figure 7.

For each number of turns from 1 to the maximum number of turns and considering a fill factor an inner diameter value is determined. Then for this inner diameter different outer diameters are used to determine different core geometries, the height being used as a variable of adjustment to guarantee the specified inductance at the maximum current. Knowing the core dimension for this particular fill factor and number of turns we determined if the core fulfilled the two following conditions

- No saturation on the inner diameter,
- Determined dimensions do not exceed the maximum prescribed dimensions.

For each design resulting of all the eligible combinations listed above, losses and cost are evaluated, and in the end, the design giving the lowest loss-cost product is selected. This operation is repeated for different fill factor and the same number of turns, and only the best solution is kept. After, we increase the number of turns and repeat the previous steps until the maximum number of turns is reached. Finally the design giving the lowest loss-cost product is select.

This method allows a quick design of toroidal inductors for different points of operation and given constraints. Improvements could be made, especially concerning winding loss calculation using the analytic approach developed by Dowell as suggested in [9].

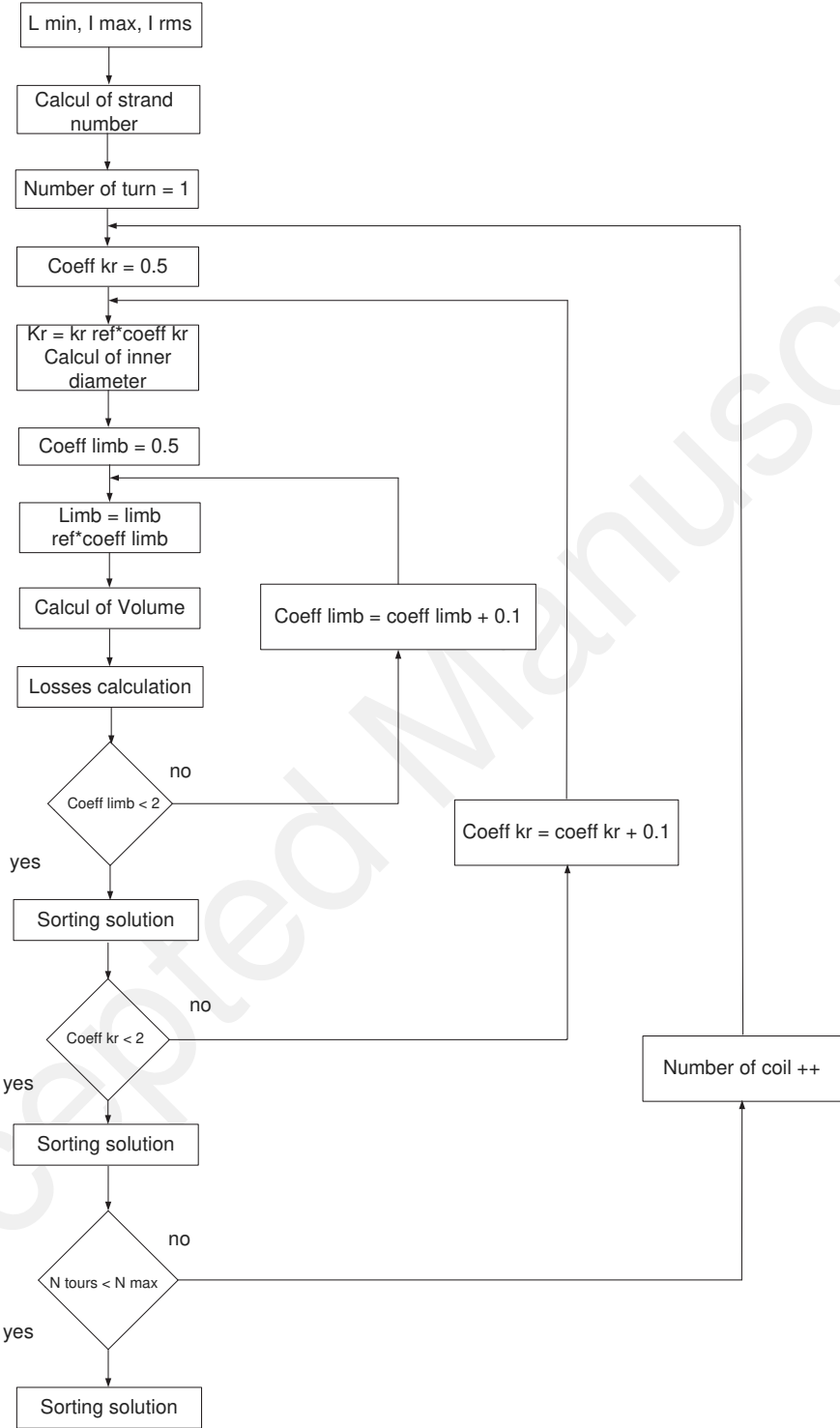


Figure 7 : Inductor design algorithm

## Comparison

The three topologies will finally be compared for points of operation at different line voltages and different battery voltages. We give here an example of results for operation on an operating voltage lying between  $250V_{RMS}$  and  $525V_{RMS}$ . The DC bus voltage is fixed by the battery and will vary between  $396V_{DC}$  and  $568V_{DC}$ .

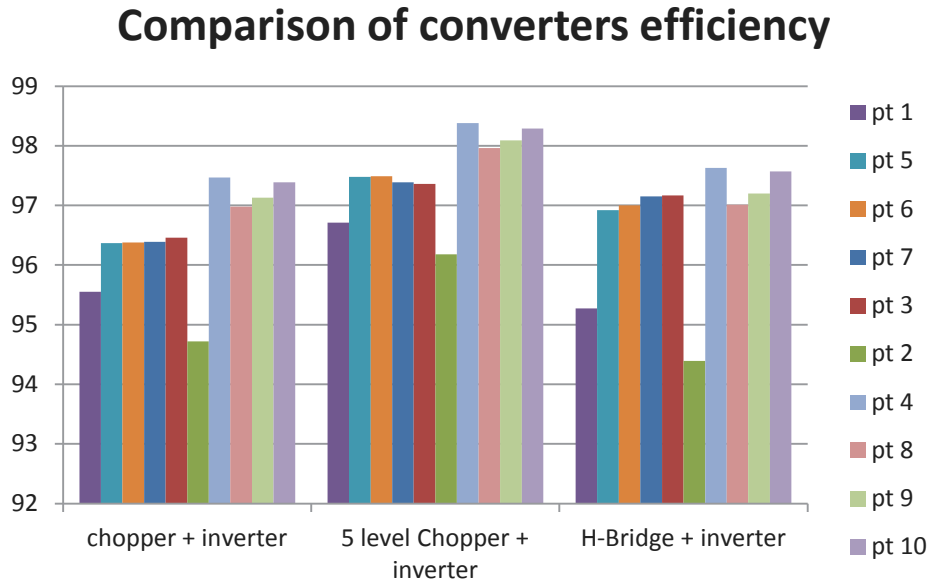


Figure 8 : Comparison of converters efficiency

**Table III: Comparison point of operation**

	Pt 1	Pt 2	Pt 3	Pt 4	Pt 5	Pt 6	Pt 7	Pt 8	Pt 9	Pt 10
$V_o$ [V]	396	569	396	569	396	396	396	569	569	569
$V_i$ [V]	144	144	303	303	219	230	277	219	230	277
Phase [rad]	0	0	0	0	3.14	3.14	3.14	3.14	3.14	3.14

It can be seen in Figure 8 : that the most efficient topology in AC/DC and DC/AC is the 5 level chopper + inverter, but this converter uses a lot of semiconductors with different voltage ratings and has a high number of inductors. The “Chopper + inverter” does not have the best performance but is the simplest of the three topologies, and it probably leaves room for improvement by using interleaving. The “H-Bridge + inverter” is generally slightly more efficient than the “Chopper + inverter” but the “H-Bridge + inverter” is a complex topology; it requires a transformer with multiple windings and a specific control strategy to regulate the capacitor voltage; also, it seems that little improvement is possible. For these reasons we chose to focus on an in-depth comparison of the “Chopper + inverter” and the “5-level chopper + inverter”.

A more detailed comparison of these two topologies at the nominal point of operation ( $400V_{RMS}$ ,  $480V_{DC}$  and  $0rad$ ) is now presented on the table IV.

As can be seen from these results, the losses in the two topologies seem to be mainly due to semiconductor losses. For the “5-level chopper + inverter”, the only ways to reduce them would be to increase the quantity of semiconductors, or to use an interleaved variant, but this would increase the cost and complexity even more. For the “Chopper + inverter” as we said previously, interleaving should bring some improvement without adding too much complexity. Further study concerning the optimization of these converters is required to determine the best option.

**Table IV: Comparison at nominal point of operation**

	Global losses S.C. + Inductors	Estimate raw material price in \$	S.C. conduction losses	S.C. switching losses	Sum of Inductance volume	$\max(LI_{\max}^2)$	$\max(LI_{rms})$
Chopper + inverter	3747W	1599	2111W	977W	0.016m <sup>3</sup>	43.87	0.073
5 level chopper + inverter	2381W	1965	1400W	515W	0.0223m <sup>3</sup>	33.5	0.1365

## Conclusion

The step-down/step-up functionality of the proposed topologies is essential for a number of recent applications such as off-line and solar UPSs using power storage elements. In this study topologies are evaluated with a numerical method and it seems now possible to realize such a converter with an efficiency around 97.5% or even 98%. This method brings the possibility to compare different topologies for given points of operations, to compare the evolution of efficiency and to estimate the main costs of each converter for different powers, frequencies, power factor, etc...Improvements can be made concerning the design and loss estimation of toroidal inductance and by extending the semiconductor loss calculation to other solutions such as MOSFET. Furthermore this method could be extended by accounting for interleaving and for the losses in the input and output filters.

## References

- [1] B. Cougo, T. Meynard, "Analysis and compensation methods of dead-time effects in a PWM AC chopper", LAPLACE, Toulouse. [2] Deboe B. D.: A novel type of grid converter, EPE 2011, paper 0321
- [2] P. Sanchis Gdrpide, O. Alonso SBdaba, L. Marroyo Palomo, T. Meynard, E. Lefeuvre, "A New Control Strategy for the Boost DC-AC Inverter", IEEE 2001. [4] Vanderkeyn Ralf W.: Example of fast switching component, EPE Journal Vol. 20 no 5, pp. 48- 56
- [3] E. F. D. OLIVEIRA, "Rectificador Trifasico PWM de alta Eficiencia com função *Bypass* e Caracteristicas Elevadora e Abaixadora de Tensão Para Carregamento de Baterias de Veiculos Eletricos", These 2013, Federal University of Ceara.
- [4] J. S. MANGUELLE, "Convertisseurs Multiniveaux Asymetriques Alimentes Par Transformateurs Multi-Secondaires Basse-Frequence: Reactions au Reseau d'Alimentation", These 2004, Federal Polytechnic school of Lausanne.
- [5] A. LEREDDE, "Evaluation des pertes dans les convertisseurs Multiniveaux", JCGE 2008, Lyon.
- [6] C. RIZET, "Amélioration du Rendement des Alimentations sans Interruption", These 2011, G2Elab.
- [7] T. DELAFORGE, R.J. PASTERCZYK, "Engineering Illusion to accurately Predict Power Losses in Magnetic Materials on the Base of Standard Manufacturers' Datasheets ", PCIM 2014, Nuremberg.
- [8] "Magnetic Powder cores", Chang Sung Corporation, [http://changsung.com/new/wp-content/themes/changsung/images/product\\_PDF/mgnetic\\_powder\\_cores.pdf](http://changsung.com/new/wp-content/themes/changsung/images/product_PDF/mgnetic_powder_cores.pdf)
- [9] T. Delaforge, H. Chazal, R.J. PASTERCZYK, "Optimization of Windings in PFC Boosts and PWM Inverters to Maximize Converter Efficiency", APEC 2014, Fortworth