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Abstract

Modern power electronics is focused on highly efficient, compact and cost-effective converters. In this paper, gallium nitride (GaN) transistors, multicell topology and integrated capacitors are combined to achieve these objectives. The first results of a 48V-to-5V DC/DC 3-level converter using integrated screen printed capacitors are presented. The power board is designed by assembling a ceramic substrate, with integrated capacitors using a Kapton® film as an insulation layer, and a multilayer PCB substrate for the active components. The integrated screen-printed capacitors technique and the proposed power board assembly allow double side cooling of the power semiconductors.

I. Introduction

Environmental issues and the widespread of consumer electronics increase the demand for highly efficient and more compact converters. Computers, mobile phones, tablet computers become more and more used in everyday life. In close proximity to the load, DC to DC converters power the load with regulated low voltage. Typically, these Point of Load (POL) converters operate off internal bus voltage ranging from 8V to 12V and have voltage outputs from 0.8V to 5V. The emergence of gallium nitride (GaN) transistors offer new perspectives and makes it possible to suppress the intermediate converter commonly used to step-down the 48V to 8 to 12V bus voltage. Indeed, very short pulses can be achieved by GaN power devices without compromising the efficiency. The high switching speed capability and low on-state resistance of these power components allows reaching better tradeoffs between power density and efficiency than Silicon (Si) transistors.

To improve the converter power density, a common solution is to increase the transistors switching frequency. This method can reduce significantly the size of passive components but decreases converter efficiency due to the increase of switching losses. Typically, passive components can be as much as 30% to 40% of the converter volume, with the inductors being a major proportion of this volume. Instead of using a classical 2-level step-down converter, an effective solution is to use a multilevel topology. The size and weight of the output inductor are then reduced thanks to an effective frequency higher than the switching frequency and a smaller voltage across the inductor. Another benefit is the diminution of the voltage stress on the power switches which allows using lower voltage rated devices with better switching characteristics.

In this context, the main objective of this paper is also to prove the feasibility of using integrated screen-printed capacitors instead of using discrete capacitors on the active layer of the power board [1], [2]. Input and flying capacitors of the converter are screen-printed on a ceramic substrate while the power devices, drivers and the output filter are located on the active layer which is a multilayer PCB substrate. An insulation layer separates the active and passive layers of the power board.

In the GaN-based DC-DC multilevel converter proposed here, screen printed capacitors lead to reduce PCB lateral power loop and provide a single side cooling surface at the back of all eGaN FETs devices. Shortening the distance between transistors reduces the parasitic inductances on the active substrate leading to higher converter efficiency. Moreover, if a double-side cooling of GaN transistors can be implemented, an increase of the converter output current may be possible.

In section II, the potential of GaN transistors is presented and compared with silicon-based devices. Section III introduces the 3-levels multilevel used for a 48V to 5V conversion. Then, screen-printed capacitors are presented, with details on fabrication process and characterization. Finally, the test results of a full converter are presented and discussed.

II. A based GaN flying capacitors converter

The first commercially available GaN High Electron Mobility Transistor (HEMT) already offers better Figure-of-Merite (FOM) than the best state of the art silicon (Si) devices [3]. Typically used to evaluate the power devices performances, the FOM using total gate charges (dynamic losses $\propto Q_g$) and on-resistance (static losses $\propto R_{dson}$) product $Q_g \times R_{dson}$ is illustrated in Figure 1. Table I lists the power devices used for this comparison.

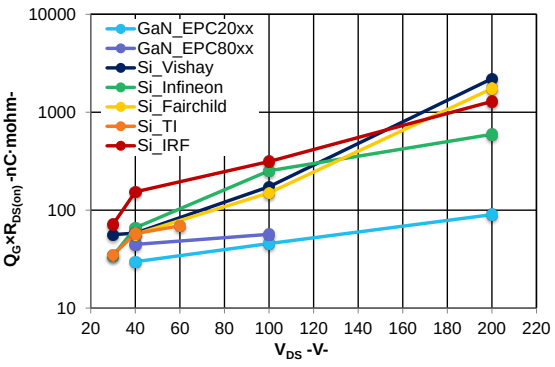


Fig. 1. Comparison of Factor-Of-Merit between GaN and Si devices

It can be noticed that the GaN transistors has a better FOM than Si devices announcing higher converter

performance. Also, this comparison is very promising for the next devices generation when GaN HEMT will be a more mature technology.

Table I. List of the compared devices

	30V	40V	60V	100V	200V
EPC20xx	/	EPC2014	/	EPC2016	EPC2010
EPC80xx	/	EPC8004	/	EPC8010	/
Vishay	SiRA04	SiR640	/	SiR870	Si7462
Infineon	BSC052N03	BSC014N04	/	BSC046N10	BSC320N20
Fairchild	/	FDMC8321	/	FDMS86150	FDB2614
TI	CSD17527	CSD18504	CSD18532	/	/
IRF	IRFH8330	IRF7739	/	IRL4030	IRFP4668

The FOM shows that the lower the voltage device rating, the higher the performance of the device. This feature is exploited in multilevel topology to achieve higher converter efficiency. The schematic of the 3-levels DC-DC converter used in this paper is given in Figure 2. Instead of using a single device rated to support the input bus voltage, several lower voltage-rating devices are connected in series. For the 48V flying capacitor converter used in this paper [4], the switches are rated to support 24V leading to employ 40V eGAN FETs devices. Combined with an output current frequency 2 times higher than the switching frequency and 3 voltage levels available V_F={0, V_{IN}/2, V_{IN}}, the output cut-off frequency of the output LC filter is typically reduced. Lower inductance and/or capacitance values lead to improve the power density by reducing the size/weight of the passive elements.

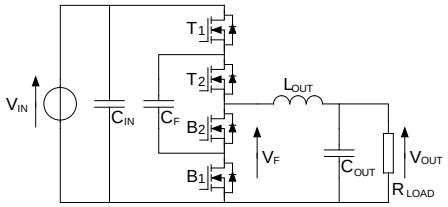


Fig. 2. 3-levels flying capacitor converter

III. Design of the 3-level DC-DC flying capacitors converter with GaN transistors

Multilevel converters are particularly suited to achieve higher power density thanks to a better harmonic content and higher performance lower voltage rated devices [5]. Figure 3 illustrates the flying capacitor (FC) converter operating in our case with a duty cycle D lower than D<0.5.

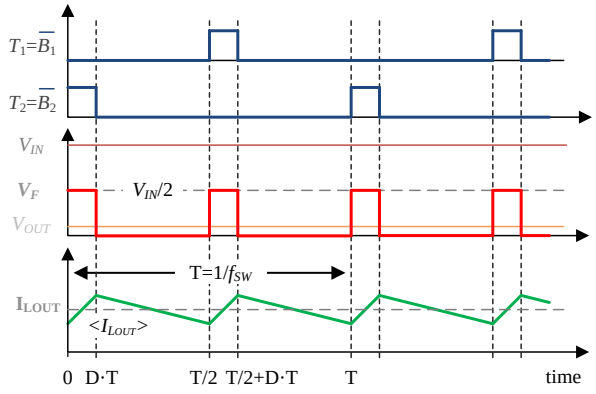


Fig. 3. Timing diagram for the 3 level FC converter with D<0.5

During the steady state, the flying capacitor C_F is naturally charged at half of the input voltage [6],[7]. The flying capacitance is given by:

$$C_F = \frac{D \cdot I_{OUT}}{\Delta V_{CF} \cdot f_{sw}} \quad (1)$$

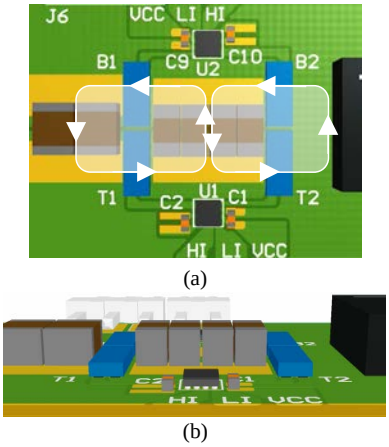
where ΔV_{CF} is the peak to peak voltage ripple across the flying capacitor, f_{sw} is the switching frequency, D the duty cycle and I_{OUT} the output current. Typically, the flying capacitor value is determined with a voltage ripple smaller than few percent and a duty cycle equal to D=0.5. The flying capacitor value becomes very large when the output current increases and/or the switching frequency decreases.

As shown in Figure 4, a first PCB design uses discrete ceramic capacitors since they present the highest capacitance density (µF/mm^3) and a very low Equivalent Series Resistance (ESR). These features allow to find high capacitance value in a very small package but still thicker than GaN transistor.

Typically, a 4.7µF ceramic capacitor X5R rated at 50V uses a 1206 package (3.2mm×1.6mm). Recommended by the manufacturer, the capacitor temperature rise is limited to 20°C which impose a maximal rms current of 2.8A at 100kHz or 3.4A at 1MHz. The capacitor rms current I_{CFrms} is given by (for the duty cycle D<0.5):

$$I_{CFrms} = I_{DC} \cdot \sqrt{2D} \cdot \sqrt{1 + \frac{\Delta I_L^2}{12 \cdot I_{DC}^2}} \quad (2)$$

where ΔI_L is the peak to peak current ripple in the output inductor and I_{DC} is associated DC current. Multiple ceramic capacitors have to be placed in parallel to compensate the weak current handling capacity of a unique ceramic capacitor.



(a)

(b)

Fig. 4. PCB design with discrete ceramic capacitors (a) top view (b) side view

From the practical view point, increasing the output current I_{OUT} with discrete ceramic capacitors have two disadvantages:

- It adds more discrete capacitors in parallel, extending the physical size of the two power lateral loop (Fig. 4) leading to increase the switching losses and voltage overshoot [8],[9].
- Since the ceramic capacitors are thicker than the eGAN FETs devices (EPC2015 thickness is 815µm),

they prohibit the use of a single heat sink on the back of all eGaN FETs devices (Fig. 5). This solution seems to be attractive to simplify construction, reduce cost and improve the power density. Such a double side cooling is motivated because the junction-case thermal resistance is 7 times lower than the junction-board thermal resistance and because GaN transistors have a very small heat transfer surface area of 6.56mm² (area of the back of the GaN transistors) limiting heat extraction.

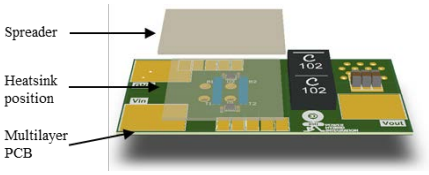


Fig. 5. 3-levels flying capacitor converter with double side cooling

IV. Ferroelectric integrated capacitors

A. *Fabrication Procedure*

In order to reduce the size and increase the unoccupied surface on PCB offering double size cooling ability, the input and flying discrete capacitors are deposited on the alumina ceramic substrate. Then, this capacitive substrate is connected to the PCB thanks to electrical vias. The layout of capacitive substrate is composed of two capacitive regions as shown in Figure 6. The smaller one is the input capacitor C_{IN} whereas the larger one is the flying capacitor C_F of the converter.

For these prototypes, integrated capacitors are fabricated by direct screen printing technique. The capacitor is realized by a dielectric layer sandwiched between two silver electrodes. The dielectric used is lead titanate based since it presents a high dielectric permittivity ranging from 2000 to 12000 resulting in high capacitance density. The silver ink is selected for matching up with the dielectric material and suitable for sintering process. The integrated capacitors are screen printed directly on the top of a 51x34mm^2 areas, 635µm thick and 96% alumina substrate. This type of substrate has very good ability for facing the high temperature of the sintering process. The first capacitive layer (silver-dielectric-silver) is fabricated according to the optimized procedure described in the following. In a first step, the substrate is cleaned using a solution of RBS 25MD 2% in an ultrasonic bath, after rinsing with de-ionized water; they are dried at 120°C during 1 hour. In the next step, the first (silver) electrode is printed on the surface of the alumina substrate dried at 120°C during 10 minutes and then sintered at 900°C during 10 minutes. A first dielectric layer (DL) is deposited on the first electrode, and dried and then sintered at the same temperature and dwell time that mentioned before. Instead of a silver electrode deposition, a second dielectric layer is screen printed to decrease the probability of direct failure due to holes and other defects of the first "high area" DL. Finally, after this second DL has been dried, the second silver layer is printed, dried and co-sintered with the second DL. The 3D structure of capacitive substrate is depicted in the Figure 7. The different thicknesses of each material layer range around 15 to 25µm and 25 to 35µm for the electrode and for the dielectric layer, respectively. Compared to the discrete capacitors, the integrated capacitive substrate proposed here allows the converter structure to be much thinner. This replacement creates more space on the surface of PCB; it brings more opportunity for cooling semiconductor devices.

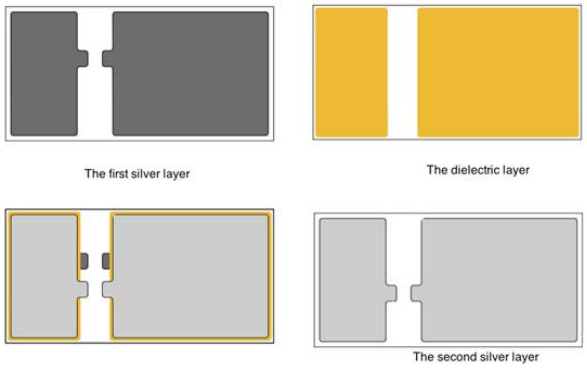
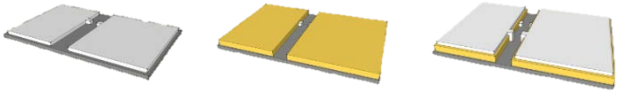


Fig. 6. Layout of the capacitive substrate



(a) (b) (c)

Fig. 7. 3D structure of the first capacitor layer: (a) first silver layer; (b) two dielectric layers; (c) the final capacitive layer

B. *Characterizations:*

Experimental setup: The main parameters capacitance, dissipation factor, impedance were measured using the HP4191A impedance/gain-phase analyzer based on auto-balancing bridge principle. The samples are directly connected to the HP4191A as shown in Figure 8(a) to eliminate undesired stray inductance.

(a) (b)

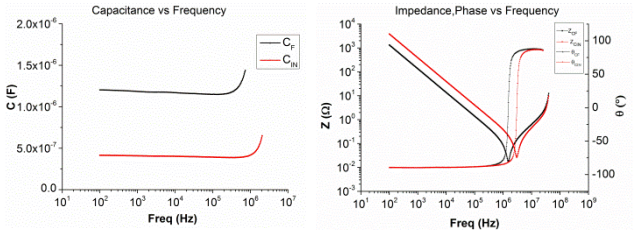
Fig. 8. (a) Impedance and Capacitance behaviors measurements (b) leakage current and breakdown/withstand voltage measurements

For the withstand voltage and leakage current determination, measurements have been achieved by using KEITHLEY 2410 Electrometer and a Signatone S-1160 probe station as shown in Figure 8(b).

Results and discussions:

The results of the capacitance measurements for the flying C_F and input capacitors C_{IN} are shown in Figure 9(a). For a dielectric layer of around 30µm, values of 1.2µF and 413nF are obtained for surfaces of 810mm^2 and 320.4mm^2 respectively. This yields to an average capacitance density of 1.3nF/mm^2. It's supposed that the capacitance density will be improved when using the conventional screen-printing process instead of direct one

due to the improvement of the quality of both: dielectric and silver layers.



(a) (b)

Fig. 9. (a) Capacitance behaviors as a function of frequency (b) Impedance behaviors as a function of frequency

The electrical characteristics of integrated capacitors are summarized in Table II in which SRF, C, D, ESR are picked from impedance measurements. The integrated capacitors present a very low value of equivalent series resistance (ESR) and equivalent series inductance (ESL).

Table II. Parameters of integrated capacitors

Name	SRF (MHz)	C (µF)	D	ESR (mΩ)	ESL (nH)
C_F	1.44	2	8.3	**17**	**2**
C_{IN}	2.75	1.08	1	**3.79**	**1.08**

The withstand voltage test was performed at room temperature on two MIM capacitors S1, S2 in FC72 (insulating liquid) and in the air, respectively. The results given in Table III prove that the withstand voltage is larger in the insulating liquid than in the air. This is mainly due to the fact that the geometry used favors flashover. Therefore, a passivation layer such as glass or parylene should be screen printed.

Table III. Withstand voltage test

Name	U (V)	I (µA)	Result	Environment
S1	1	Under Limit	Ok	FC72
	10	UL	Ok	
	20	UL	Ok	
	50	UL	Ok	
	100	0.2	Ok	
	200	0.2	Ok	
	300	0.2	Flashover	
	400	$>I_{Limit}$	Flashover	
S2	1	UL	Ok	Air
	10	UL	Ok	
	20	UL	Ok	
	50	UL	Ok	
	100	UL	Ok	
	200	UL	Flashover	
	300	0.7	Flashover	
	400	$>I_{Limit}$	Flashover	
	450	$>I_{Limit}$	Flashover	

A good insulation resistance (derived from leakage current measurement and applied voltage ($R_{Is}=V/I_L$)) is necessary for capacitors used to block off DC voltage and/or to store electromagnetic energy for a long period of time without variations. In the simple case, the leakage current I_L of a ferroelectric capacitor depends on the applied voltage. The measured leakage current (not presented here for the sake of clarity) of MIM capacitors ranges in the order of nano-amps (nA). The derived insulation resistance (R_{Is}) is around 1GΩ at 100V.

In summary, the different properties of the material under study and of the manufacturing process used to realize the input and flying capacitors are in good agreement with the objective.

V. Converter Assembly

The exploded view of the converter assembly is shown in Figure 10. A photo of the prototype is presented in Figure 11.

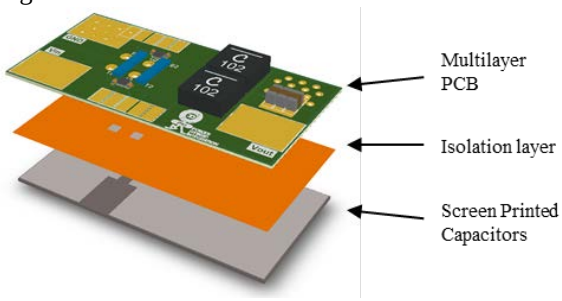


Fig. 10. Illustration of the assembly arrangement capacitor and its impedance

The active layer is a multilayer PCB substrate. GaN transistors, drivers and the output filter are located on the first layer. The second layer is a ground plane used as a shield layer in order to reduce the lateral power loop inductances, i.e. reduce switching losses and voltage overshoot [8], [9]. Compare to a DBC which has a better thermal feature (typical thickness superior to 0.6mm), the PCB substrate is advantageous because the insulation layer can be very thin (100µm) allowing to have a high field cancellation effect. The closer the two conductive layers, the smaller the parasitic inductances. The ground plane is also used as spreader layer, improving thermal aspects.

In order to avoid local short circuit between capacitive substrate and the PCB track, an insulating layer has to be used. This layer may reduce the stray capacitance between capacitor's electrodes and PCB. The 2 mils kapton® adhesive film is selected because it is able to withstand the temperatures between 250-400°C used during the soldering process. Kapton® film does not soften at elevated temperatures, thus the film provides an excellent release surface at elevated temperatures.

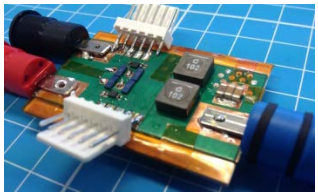


Fig. 11. Experimental converter with screen printed capacitors

VI. Results

Several tests were carried out under less nominal power. The input voltage was fixed to 44V and the output voltage equal to 5V. The output current was limited because of the small input and flying capacitances values. Direct screen printing and a one-capacitive layer lead to an input capacitance equal to 0.4µF and a floating capacitance equal to 1.2µF. Screen printing and a higher

number of capacitive layers will lead to more important capacitances values allowing to increase the output current. The switching frequency f_{SW} is equal to 400kHz and the total output inductor value is 2µH. The GaN transistors are eGaN FETs EPC2015 rated at 40V.

Figure 12 present the waveforms of the output voltage V_{OUT} and the output current I_{OUT}. The output current reaches 3A. V_F the potential of the serial multicell midpoint with respect to ground varies from 26V to 19V. The voltage unbalanced is due to an open loop command. V_F is characteristic of a 3-level flying capacitor topology: the signal has an effective frequency equal to 800kHz ($2 \cdot f_{SW}$) and a maximal value around half the bus voltage $V_{IN}/2$.

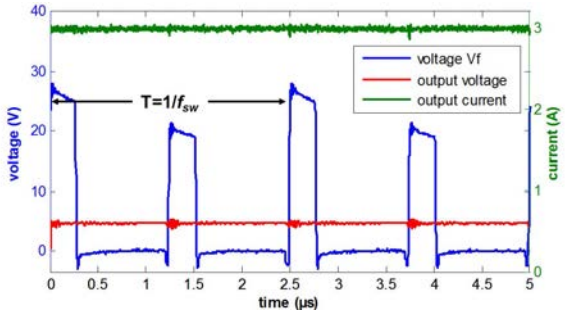


Fig. 12. Experimental waveform of V_F; output voltage and current

VII. Limits and perspectives

Integrated screen-printed capacitors seem to be an interesting solution for integration. However, in this solution, nominal capacitance has to be increased and also the interface between capacitors and the PCB requires attention given its mechanical and thermal behavior. Insulation layer is made with Kapton® which is a solution without great mechanical resistance. Thus, an improvement could be to change this interface.

The opposite surfaces between capacitors and the shield layer of the PCB form parasitic capacitors which produce current spikes and ElectroMagnetic Interferences (EMI). A shield layer reduces PCB lateral parasitic inductances (§III), and is especially important in the area close to the switches, where transient phenomena have effective impacts. Modification of the shield layer in uncritical areas could reduce parasitic capacitors with low impact on power loop inductance reduction. However, the reduction of the shield layer also reduces the thermal spreader effect. The design of the best solution is a tradeoff between thermal effects, EMI, and parasitic elements.

Larger input and flying capacitances allow to increase the converter current and consequently to reach a higher power density. Thus, the capacitor process has to be improved to increase the quality and the number of layers.

VIII. Conclusions

In order to increase the power density of DC-DC converters, the solution explored in this article consists of using integrated capacitors with GaN devices on a multilevel converter. The flying capacitor topology allows the reduction of constraints on active and passives devices, and at the same time to use lower rated devices with better characteristics.

The integrated capacitor were developed using screen-printed technique, which reduces switching parasitic elements while allowing double side cooling.

In this paper, a prototype of a flying capacitor converter designed for 48V input and 5V output with direct screen printed capacitors proves the feasibility to replace discrete capacitor by integrated capacitors. The output current reaches 3A and has an effective frequency of 800kHz, twice the commutation frequency.

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