Pre-design methodology and results of a robust monolithic InterCellTransformer (ICT) for parallel multicell converter

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In this paper, the pre-design methodology of a monolithic Inter Cell Transformer (ICT) in parallel multicell converters is presented for normal operation and with a reduced number of phases. The goal is not to saturate the active phases when the number of cells is reduced. An analysis and comparison of monolithic ICT have been conducted in these two configurations. The increased volume and mass of the robust monolithic ICT is very important for low number of cells. Air-gaps have been inserted in order to limit this augmentation. These air-gaps balance and reduce the overload flux density in active cores during the post-failure operation. In order to validate the theoretical results, a ladder structure of a 6-phase monolithic ICT and a reconfigurable converter has been built. The experimental results for the prototype will be presented by the authors in their next paper.

I. Introduction

Parallel and interleaved multicell converter have been introduced in low voltage DC/DC applications, such as Voltage Regulator Modules (VRM) for the supply of power to microprocessor boards [1]. Presently, applications are wide spread in the medium and high power field, such as in Uninterruptible Power Supplies (UPS) or converters (DC/DC and DC/AC) for on-board applications such as electrical powertrain and plug-in on-board charger on EV/HEV. The benefits of parallel multicell converters are :

- A waveform improvement, including a decrease in the energy stored in input / output filters.
- A scalable power range using only the low current rating of power devices.
- A reduced number of phases of operation used for: a) optimal efficiency at medium and low power, b) failure management including post-fault continuation.

$\frac{1}{2}$ Basically, in Fig. 1, a set of "p" commutation cells generate a two-level voltage waveform with a $\frac{2.\pi}{p}$ phase-shift. The connection of equal uncoupled inductors at the output provides, without load, a "$p+1$" level waveform with an output switching frequency equal to $p.F_{sw}$.

Then, when a load is connected, this property produces a $p.F_{sw}$ load current ripple. Considering the filtered load, the maximal current ripple at each uncoupled inductor (duty 50%) is equal to:

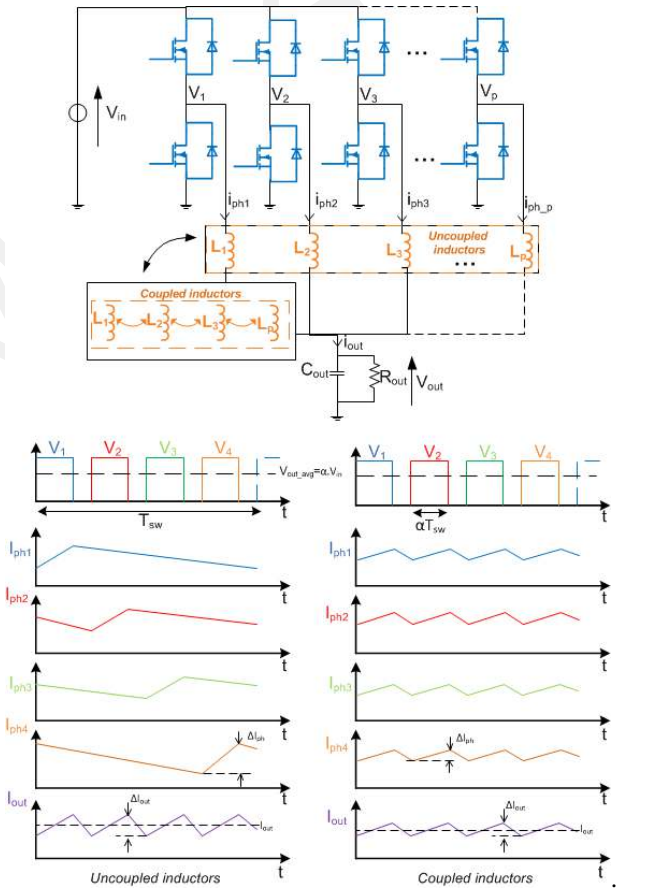


Figure 1. Parallel multicell converter with p phases using uncoupled and coupled inductors and filtered load

$$\Delta I_{ph(max)} = \frac{V_{in}}{4.L.F_{sw}} \quad (1)$$

The output current ripple is calculated including an apparent duty cycle $\alpha^{'}$ and the apparent output switching frequency $p.F_{sw}$ as previously introduced:

$$\Delta I_{out} = \frac{\alpha^{'}.(1-\alpha^{'})}{p^2}.\frac{V_{in}}{4.L_{out}.F_{sw}} \quad (2)$$

In (2) note that L_{out} is the equivalent output inductor equal to L/p. This equation shows that an increased the cell number in parallel leads to a reduction in the output current ripple by a factor p: ($\Delta I_{out(max)} = \Delta I_{ph}/p$). Finally, the relative current ripple in each phase is equal to $(\Delta I_{ph}/I_{ph}) = p^2.(\Delta I_{out}/I_{out})$. This property is the reason for extra semiconductors and winding losses, increasing the volume and mass of uncoupled inductors.

One solution consists of placing all windings together on the same magnetic core. This type of ICT is generally called a monolithic transformer. The results of [2] show a smaller sized magnetic core and waveform improvement: with the phases and output relative current ripples having the same value: $(\Delta I_{ph}/I_{ph}) = (\Delta I_{out}/I_{out})$. However, ICT are greatly sensitive to the current imbalance between phases, such as the dispersion of the current sensors gain or component imperfection (Rdson). As illustrated in Fig. 2, a current imbalance lead to an overload of the flux density (δB_{DC}), which results in the saturation of the corresponding core . Phase 5 has +0.5% of the nominal current phase and phase 6 has -0.5%. Phase 5 works in the knee of the initial magnetisation curve with a high magnetising current. In the worst case, typically the interruption of one leg, at first sight this magnetic structure does not seem to be adapted, with a reduced number of phases. In this

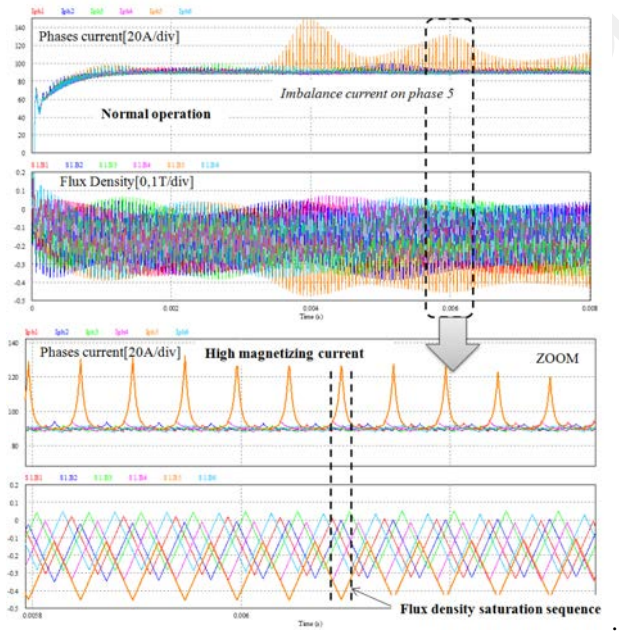


Figure 2. Example of 6-phase monolithic ICT. Simulation of phase currents and core flux density: case for current imbalance (0.5%) on phase 5(t=10ms) (Vin=400V, Iph = 95A, p=6)

article, the authors present several pre-design approaches to make the monolithic ICT more robust for operation, including a cell commutations interruption. All results will be compared with uncoupled inductors, which appear as the limit of the acceptable solution. Another approach consists of coupling and starting an additional parallel and redundant leg instead of the failed leg after a safe disconnection [3]. This solution will not be presented in this article. In the first part of the article, the "$Ae_{core}.S_w$" pre-design and pre-optimised method in normal operation will be recalled, and afterwards over-sizing including an interruption of the "k" out of "p" phases will also be detailed. In the second part of the article, a method based on air gap insertion into the core leg under normal operation making the ICT more robust, stopping in "k"out of "p" phases and not saturating the magnetic core. Finally, a 6-phase robust ICT set up in closed-scale topology is introduced including removable horizontal core leg, permitting a variable air gap (thin or thick) adjustment.

II. Pre-design of a monolithic ICT in normal operation

This part presents a simple pre-design methodology based on an "$Ae_{core}.S_w$" calculation under normal operation. Fig. 3 shows the ladder structure of a monolithic ICT. $\varphi_{return-leakage}$ is the leakage flux equivalent flowing through the winding space inside the window between two consecutive cores. $\varphi_{winding-leakage(1,2)}$ represent the leakage flux directly flowing through the air in the phase 1 and 2.

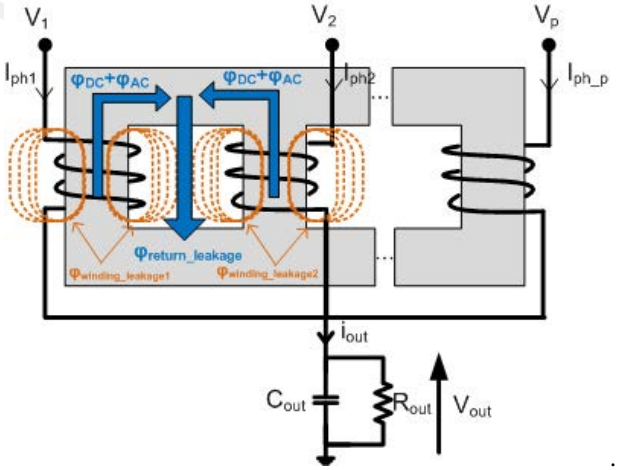


Figure 3. Monolithic ICT ladder structure

Nominal operation presumes work in the linear part of the magnetisation curve of a typical ferrite core material. Monolithic ICT behaviour analysis can be split into two parts, DC and AC flux density analysis:

- DC model: Based on a DC ampere-turn and magneto-motive force (MMF) on each winding and reluctances network.

Fig. 4 shows a DC equivalent circuit model of the ladder structure of the monolithic ICT. R_{hc} and R_{vc} are respectively the reluctances of the vertical legs and the top or bottom

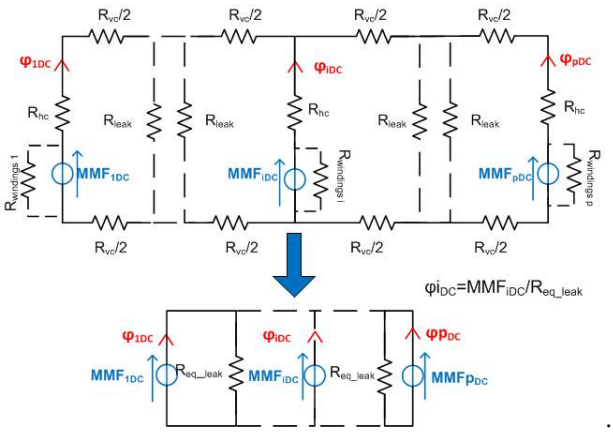


Figure 4. DC forces equivalent circuit model: $MMF_{iDC} = N.I_i$

horizontal legs. $R_{windings(1,2,p)}$ is the windings leakage reluctances directly flowing through the air. R_{leak} is the local leakage reluctance flowing through the core window. The fluxes in each leg φ_{1DC} are caused by the magnetomotive forces(MMF) of each winding R_{hc} and R_{vc} reluctances can be neglected compared to R_{leak}. In this part, we also suppose that all MMF are equal and balanced. Then, it is obvious that all leakage flux density components only depend on the equivalent output leakage inductance.

- AC model: Based on AC magnetising flux sources produced by the AC voltage applied across the winding terminals.

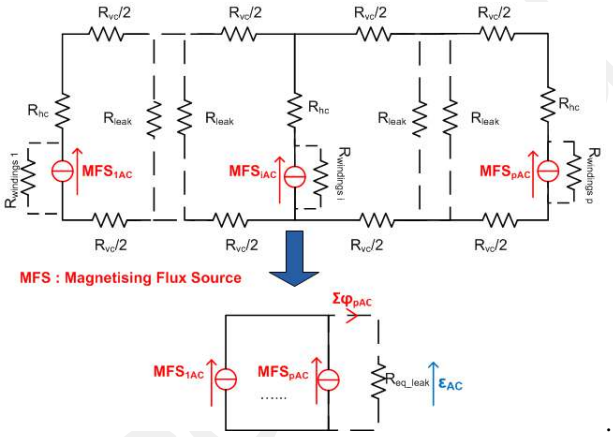


Figure 5. AC sources equivalent circuit model:$MFS_{iAC} = \int Vac_{winding_i}, dt$ with MFS being magnetising flux source

Based on Fig. 5, we can state that the sum of the AC flux sources produce an AC homopolar MMF at switching frequency $p.F_{sw}(\epsilon_{AC} = R_{eq_{leak}}.\sum \varphi_{AC_{core}})$. This component induces a coupling effect [2] and allows the current ripple relation to be determined in all phases:$N.I_{iAC} = \epsilon_{AC}$. By adding the AC and DC model, an unsaturation condition has been written to the flux density in the core :

$$B_{DCcore} + B_{ACcore} < k_{sat}.B_{sat} \quad (3)$$

With B_{sat} being the saturation flux density, and k_{sat} the increase coefficient on saturation flux density. By using (3), we find the core cross-sectional area expression (Ae_{core}). Then, we can write the area product method for each phase, which is the product between the core cross-sectional area and the winding area (S_w):

$$(Ae_{core}.S_w) > \frac{n_b.k_f.P}{4.p.F_{sw}.B_{sat}.J}.\sqrt{1+\frac{k_i^2}{12}}.(\frac{1}{2}+\frac{1}{k_i^2.p^2}) \quad (4)$$

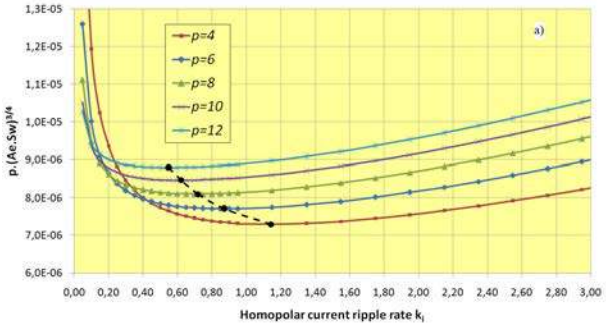
With n_b being the number of windings in the winding area (in this case, n_b=2), k_f is the winding area coefficient, k_i is the homopolar current ripple ratio, and p is the number of interleaved cells. In (5) we also introduce the concept of total volume and total mass [4].

$$(Volume/mass)_{total} \propto p.[(Ae_{core}.S_w)_{eachphase}]^{3/4} \quad (5)$$

Equation (5) is drawn in Fig. 6.a) as a function of k_i when p is fixed, and in Fig. 6.b) as a function of p when k_i is fixed. We can see in these two graphics interesting optimum values (k_{iopt} and p_{opt}) which are the roots of the partial derivative relation, shown in (6) and (7):

$$\frac{\partial}{\partial k_i}(Totalmass/volume)\mid_{pfixed} = 0 \rightarrow k_{i(pot)} = (\frac{24}{p^2})^{1/3} \quad (6)$$

$$\frac{\partial}{\partial p}(Totalmass/volume)\mid_{k_i fixed} = 0 \rightarrow p_{(pot)} = (\frac{10}{k_i})^{1/2} \quad (7)$$



p_{opt} is equal to 14, 10 and 8 for k_i=0.05, 0.10 and 0.15 respectively. Note that p_{opt} = 8 is a practical value, but the use of this value presumes an increase in the k_i value from 5% (typical value) to 15%, thus minimising the core mass to 20%. Fig.7 shows a 6-phase ICT simulation during normal operation using previous relations (3) and (4). We note that flux density in each vertical cores are below the limit of saturation B_{sat}. This pre-design also includes geometrical factors for ICT, and physical parameters that will not be depicted here but which can be found in [4].

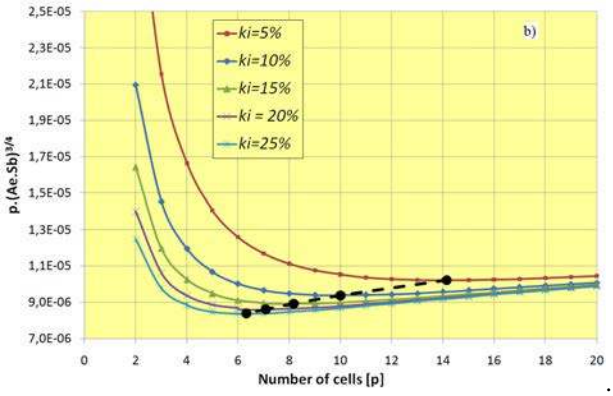


Figure 6. a) Volume and mass function according to k_i , b) Volume and mass function according to p

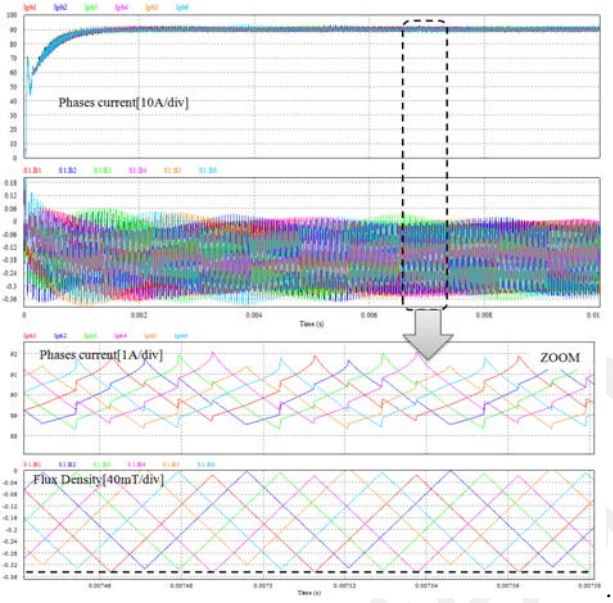


Figure 7. Waveforms of phase current and flux density during normal operation of 6 phase DC/DC converter (V_{in}=400V, I_{ph} = 90A, p=6, F_{sw}=50kHz, duty cycle = 1/2, k_i=5%, B_{sat}=0.4T, N=18(number of windings), Core material N87 at $100 degrees$)

III. Pre-design of a monolithic ICT with reduced number of phases

In this part, we present a pre-design model with a reduced number of phases. As it can be seen in Fig. 8, the 'k' parameter represents a disconnected number of cells. Cells are disconnected during one or several electrical failures or following a half-bridge stop working towards improved converter efficiency at low power operating points. The reduced number of phases leads to cancelling the current and Ampere-turns into k phases. In this case, each k core is equivalent to a magnetic short-circuit in parallel with $p-k$ operational phases, and which must sustain an over rate a DC flux density equal to $k.B_{sat}$. Their reluctances are negligible in comparison to the leakage reluctances. So, the operational cores experience an overload flux density ($k.B_{sat}/(p-k)$) in addition to the nominal flux density, as can be seen in (8).

$$B_{sat} > \frac{k.B_{sat}}{(p-k)} \tag{8}$$

We deduce from (8) a condition for the minimum number of phases in order to avoid a saturation flux density in all cores.

$$p > 2k \tag{9}$$

where 'p' is the total number of phases and 'k' represents the disconnected number of cells.

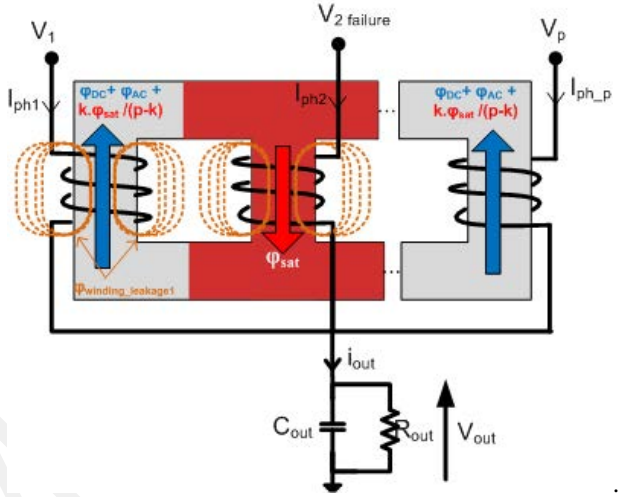


Figure 8. Monolithic ICT Ladders structure with one phase reduced

These condition (8) and (9) supposes that the total overload flux density is equally-distributed to $p-k$ operational phases. We can see the DC and AC equivalent circuits in Fig. 11.

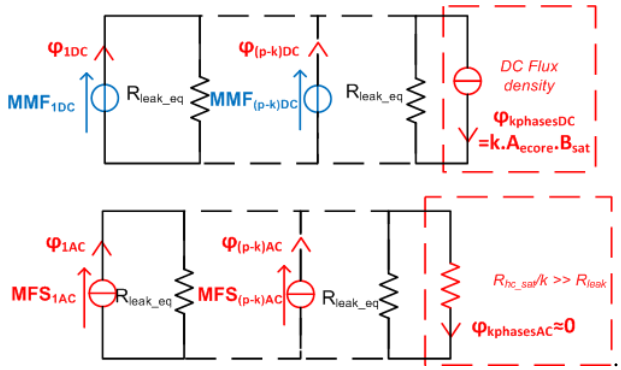


Figure 9. DC and AC equivalent circuits of monolithic ICT structure with a reduced number of phases

We note in Fig.11 that only the DC equivalent circuit is modified, therefore also the homopolar inductance [5]. The currents in each phase are equal to $Iout_{nominal}/p$, which induces an output current derating:

$$I_{out(derating)} = I_{out(nominal)}.\frac{(p-k)}{p} \tag{10}$$

From Fig.11, we determine a core cross-section area expression:

$$B_{DCcore} = \frac{V_{in}}{4.p(p-k).F_{sw}.k_i.N.Ae_{core}} + \frac{k.B_{sat}}{p-k} \quad (11)$$

Using (3), we can determine the area product relation in this configuration:

$$(Ae_{core}.S_w) \quad > \quad \frac{n_b.k_f.(p-k).P_{nom}}{4.p.F_{sw}.(k_{sat}.(p-k)-k).B_{sat}.J} \cdot \sqrt{1+\frac{k_i^2}{12}} \cdot (\frac{1}{2} + \frac{1}{k_i^2.p^2}) \quad (12)$$

When k=0, we can ascertain the area product expression without a reduced number of phases, so in normal operation. Finally, using relation (5) a direct link can be done to give out in Fig. 10, Volume-Mass evolution about monolithic ICT according to the number of phases p and number of failures k. Also, the light blue curve represents the uncoupled inductors.

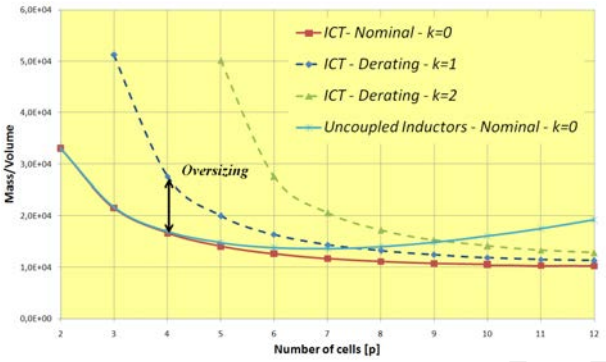


Figure 10. Mass trend as a function of the number of cells for different numbers of failures (V_{in}=100V, I_{out}=100A, F_{sw}=50kHz, B_{sat} = 0.4T, k_{sat}=0.9, $J = 4A/mm^2$, k_i=5%)

We note in Fig. 10 the hyperbolic variation in mass trend for the monolithic ICT. In the analysis in Fig. 10, (4) and (14), it should be noted that:

- With a low number of phases, the DC flux density is higher than the AC flux density, as an inter-phase inductors topology.
- With a high number of phases, the AC flux density is overwhelming ($1/k_i.p.(p-k)$ approaching zero) as a transformer rating.

Table I shows that the core losses decrease with the number of cells, when $k = 1$.

Fig. 10 shows an increased ICT mass for a low number of phases (p<4). The monolithic ICT's excess weight is too elevated, especially for embedded converters.

IV. Pre-design of a monolithic ICT with Air-Gap insertion

We have shown in the second part that reducing the number of phases can cause a high flux density overload on the operational $p-k$ phases. This property leads to an increase in

Table I
Volume/mass, core(Steinmetz equation) and copper losses relative evolution as a function of the number of phases, when k=1 and k=2

Number of cells	4	6	8	10
$Powerderating(k=1)$	-25%	-16%	-12,5%	-10%
$Volume/mass(k=1)$	+66%	+30%	+18,5%	+13%
$\frac{Pcore_{losses(k=1)}}{Pcore_{losses(k=0)}}$	-34%	-19%	-13%	-10%
$\frac{Pcopper_{losses(k=1)}}{Pcopper_{losses(k=0)}}$	+58%	+41%	+25%	+17%
$Powerderating_{(k=2)}$	×	-33%	-25%	-20%
$(Volume/Mass)_{(k=2)}$	×	188%	54%	34%

core size when the number of phases is small (p<4). We also found an unequal distribution inf the flux density saturation, due to a residual air-gap at the bottom of the vertical core. This imbalance increases when the ratio R_{hc}/R_{vc} is large. In order to reduce and balance the flux density overload, we investigated the insertion of air-gaps at the junction of the vertical and horizontal cores, as seen in Fig. 10.a). The purpose of these air-gaps is to reduce the R_{hc}/R_{vc} ratio in order to balance the flux density saturation on the operational $p-k$ phases.

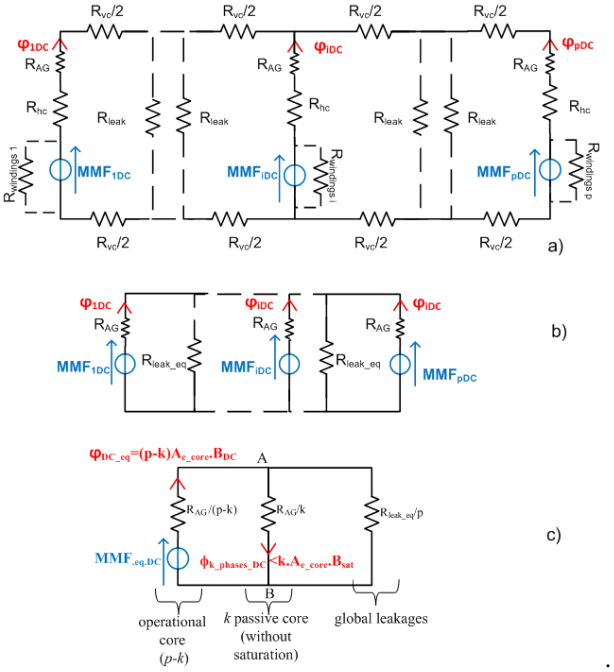


Figure 11. a) DC MMF equivalent model in normal operation with air-gap insertion in vertical core, b) DC MMF equivalent model neglecting vertical and horizontal legs reluctances. c) Equivalent model when k phases are disconnected

Then, the vertical leg reluctances become negligible compared to the vertical air-gap reluctances (R_{AG}), leading to the equivalent circuit in Fig. 10.a). The k vertical cores in failure are assumed not to be saturated due to the vertical air gap reluctances. This hypothesis will be verified later by simulation. Based on Fig. 10c), the core cross-section area expression can be written on the operational $p-k$ phases:

$$B_{DCcore} = \frac{\mu_0.N.I_{out}}{AG.p}\left[1 - \frac{(p-k)}{p}.\frac{1}{1+\frac{AG}{p.AG_{leak}}}\right] \quad (13)$$

With AG being the vertical air-gap thickness and AG_{leak} an equivalent air-gap through which the total leakage flux of the ICT flows. The AC flux density source is not modified. By using (13) and (3), we can write the following condition:

$$k_{sat}.B_{sat} < \frac{\mu_0.N.I_{out}}{AG.p}\left[1 - \frac{(p-k)}{p}.\frac{1}{1+\frac{AG}{p.AG_{leak}}}\right] + \frac{V_{in}}{8.N.F_{sw}.Ae_{core}} \quad (14)$$

The insertion of a vertical air-gap decreases the DC flux density as shown in (13). This air gap also balances the overload flux density between the phases during the electrical failure of the commutation cell.
Unfortunately, the air-gap insertion leads to a decreased magnetising inductance, which increases the magnetic current ripple in each phase. With the help of [5], the magnetising and homopolar leakage inductances can be determined.

$$L_{mag} = \frac{\mu_0.N^2.Ae_{core}}{AG.\left(1+\frac{AG}{p.AG_{leak}}\right)} \quad (15)$$

$$L_{leak(total)} = \frac{\mu_0.N^2.Ae_{core}}{p.AG.\left(1+\frac{p.AG_{leak}}{AG}\right)} \quad (16)$$

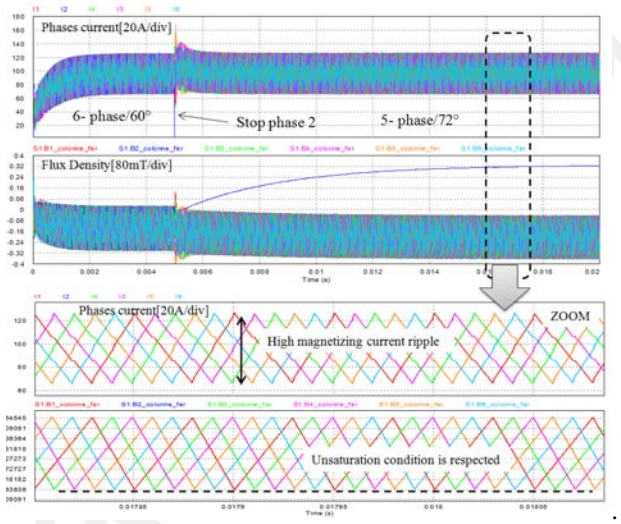


Figure 12. Waveforms of phase current and flux density when phase 2 is disconnected (V_{in}=400V,I_{ph}=95A,p=6, B_{sat}=0.4T, AG=3.2mm)

Fig. 12 present a 6-phase ICT simulation when phase 2 is turned off. Unsaturation condition is respected in active phases but involves a high vertical air-gap value (3.3mm) and therefore a high magnetising current ripple flowing between two phases. In order to avoid this augmentation, a idea would be to use a small phases current derating and a thin vertical air-gap.

V. Conclusion

This paper introduced a pre-design methodology for a robust monolithic InterCell Transformer (ICT) for parallel multicell converters. This study can be applied to DC/DC and DC/AC converters for on-board applications such as electrical powertrain and plug-in on-board charger on EV/HEV. We showed in the first part that optimum parameters ($ki_{opt}$and p_{opt}) exist that can be useful to fix the initial values for a post-optimisation process. Based on volume and mass representation, we can state that a monolithic ICT working with one leg missing has excessive weight for a low number of phases ($p < 4$), this is especially too large for embedded converters. A vertical air-gap insertion has been presented in the third part, however this air-gap increases the magnetising current. A better solution would be to use in parallel a phases current derating and a thin vertical air-gap in order to limit the magnetizing current. New monolithic ICT structures are being studied that may overcome such drawbacks. Another way to deal with this problem is to work on the electrical architecture of the converter, by adding a redundancy leg ($p+1$) which can automatically replace a faulty leg in an inverter or chopper [3]. Experimental results will be presented by the authors in their next paper.

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