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Ayawo Roger Ekon, Mickael Petit, François Costa, Francois Bouvet, Eric Dupuy. Impact of routing on the EMC behavior of a GaN HEMT-based full bridge DC-DC converter. 2022 International Symposium on Electromagnetic Compatibility – EMC Europe, Sep 2022, Gothenburg, Sweden. pp.415-420, 10.1109/EMCEurope51680.2022.9900951 . hal-03934032

**HAL Id: hal-03934032**

**<https://hal.science/hal-03934032v1>**

Submitted on 8 Mar 2023

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# Impact of routing on the EMC behavior of a GaN HEMT-based full bridge DC-DC converter

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**Abstract**—In the perspective of upgrading the SOLEIL synchrotron accelerators, new electromagnet power supplies utilized for the control of the electron beam trajectory are being studied. For those implemented in the fastest beam orbit feedback loop, a new generation of low voltage, high frequency DC-DC converters based on Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) is envisaged. One of the crucial points of their design concerns the routing of the switching cells, which is critical with respect to Electromagnetic Compatibility (EMC) and surge voltages, thus requiring a preliminary investigation. For this purpose, a routing model using the Ansys Q3D software is studied in this paper. The data from the Q3D simulation are compared to the experimental results for the prediction of the EMC performance of the DC-DC full-bridge converter. The EMC model resulting from this study allows analyzing the influence of the inter-cell parasitic inductances on the levels of the disturbances conducted in common and differential mode.

**Keywords**—Power electronics, Routing, EMC, GaN components

## I. INTRODUCTION

The magnet power supplies foreseen for the new storage ring, currently under study, of the SOLEIL synchrotron light source require greater compactness, very high reliability, and minimization of the residual ripple of the output current. These increased constraints are contradictory [1], especially for the power supplies involved in the fast orbit feedback system [2], as they also request higher dynamics. Meeting these requirements means a technological and structural rethinking of the design of existing power supplies. In particular, an increase in switching frequency is necessary to higher the dynamic range and reduce the current ripple. The use of wide band gap components based on GaN allows meeting these constraints and enables enhancing the converter power density.

Indeed, with increasingly steep switching edges [3], these components allow their use at high frequencies (0.1-1 MHz range), and thus an improvement in power density. Despite their switching and conduction performances, the EMC constraints of systems integrating these components are becoming extremely severe. Consequently, EMC must be taken into account during the design of the converter from the routing phase where certain rules must be respected without degrading the thermal performance [4]. A compromise between EMC and thermal management must be found. Achieving the EMC objectives essentially implies a reduction of the switching loops area. On the other hand, in order to

better dissipate the losses, the distance between the active components is essential to limit the thermal coupling and spread the heat flows.

Achieving the first objective means mastering the various parasitic effects, and in particular, the parasitic inductances of the switching cells. In addition to this, the capacitive couplings between different variable potentials must also be controlled. A predictive study to minimize disturbances at the source, facilitating in a second time the sizing of the EMC filters, is thus essential from the design phase. The study of the impact of the switching cell area on the EMC performance of a Buck chopper has been proposed by [5] [6]. On the other hand, a study carried out by [7] shows the effect of an unbalanced capacitive coupling between the DC bus potentials and the ground on the EMC performance of a half bridge converter. However, these studies do not correspond to the topology chosen for the new magnet power supplies of the future SOLEIL fast orbit system, since it consists of a double switching cell. This makes the routing more complex than those presented in the literature do: the number of parasitic elements is clearly increased.

Thus, this paper discusses the characterization of inductive and capacitive parasitic effects in a full bridge converter based on numerical simulation using Ansys Q3D software [8] [9]. A comparison is made between the simulation data and measurements performed on a model. Intercellular parasitic inductances depending on the distance between the switching cells partially govern the EMC behavior of the converter, which is studied in the following.

## II. EMC MODEL AND ROUTING RULES

The studied converter is a four-quadrant DC-DC converter (H-bridge) based on 40 V / 29 A GaN components (ECP2055) *Fig. 1-a*. The capacitance of the input capacitor of the converter is  $C_{xe} = 47 \mu\text{F}$ . The DC bus voltage is  $V_{dc} = 24 \text{ V}$  and the switching frequency is  $f_{sw} = 400 \text{ kHz}$ . The converter is designed for the power supply needs of the future SOLEIL fast orbit feedback system. In order to guarantee the symmetry of the converter, each switching loop has the same topology (length and loop area). For this reason, the capacitor  $C_{xe}$  has been distributed in two parts as shown in *Fig. 1-b*:

- a part composed of two capacitors ( $C_{b1}$  &  $C_{b2}$ ) which play the role of decoupling capacitors close to the switching cells,
- the other part is composed of the capacitor  $C_{xe'}$  realized by  $n$  capacitors of capacity ( $C_{xe}/n$ ) parallelized. The value of the

equivalent parasitic inductance (ESL) is then minimized. In order to minimize the surface area and the total inductance of the switching loops, MLCC-SMD capacitors (Multilayer Ceramic Capacitor-Surface Mounted Device) are used: on the one hand, their equivalent series inductances (ESL) are lower and on the other hand, their reduced connections allow limiting the surface area of the switching loops.

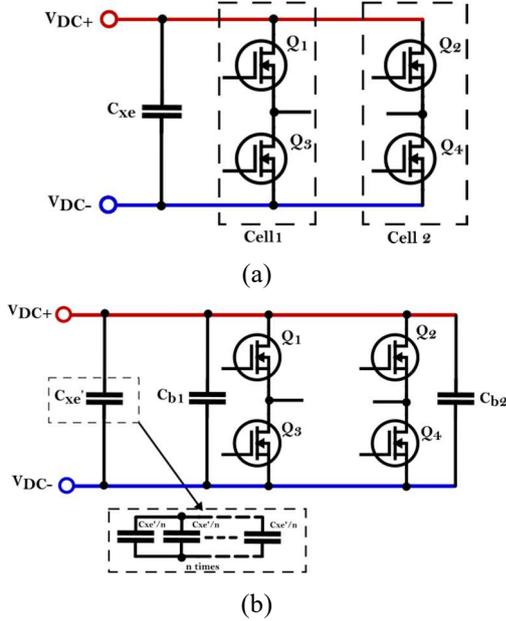


Fig. 1. Scheme of a complete bridge chopper with its decoupling capacitor

### A. Equivalent model

The equivalent EMC model of the converter is shown in Fig. 2. The internal parasitic inductances of the transistor packages, the different parasitic inductances on the control side as well as the different inductive couplings are not represented.

Concerning the power circuit, two switching loops can be identified:

- **loop 1**: composed of  $[Q_1, L_{b1+}, R_{s\_Cb1}, C_{b1}, L_{s\_Cb1}, L_{b1-}, Q_3 \text{ and } L_{p1}]$ .
- **loop 2**: composed of  $[Q_2, L_{b2+}, R_{s\_Cb2}, C_{b2}, L_{s\_Cb2}, L_{b2-}, Q_4 \text{ and } L_{p2}]$ .

This representation localizes the inductive effects that are actually distributed along the loop.

Based on model, the constraints that will apply to optimize the routing in order to limit overvoltages and minimize the propagation of parasitic currents at the source are explained as follows:

- the equivalent parasitic inductances in each switching loop are at the origin of overvoltages across the transistors when they are switched-off. Indeed, during the corresponding transient, the energy stored in these inductances is exchanged with the capacitance  $C_{oss}$  of the transistor via a resonance mechanism. The equivalent parasitic impedance of each of these loops must be minimized. The values of ESL and ESR of the capacitors and transistors being fixed by their technology and size, the only elements we can minimize are those due to the routing ( $L_{bi+}$ ,  $L_{bi-}$  and  $L_{pi}$ ).

- the intercellular inductances ( $L_{M+}$  and  $L_{M-}$ ) do not directly contribute to the impedance of the switching loops. However, they do contribute to the degradation of EMC performance and to overvoltage at the transistor terminals. On the other hand, they must be minimized and balanced by routing and placement. Their effects are studied and further investigated in section IV.

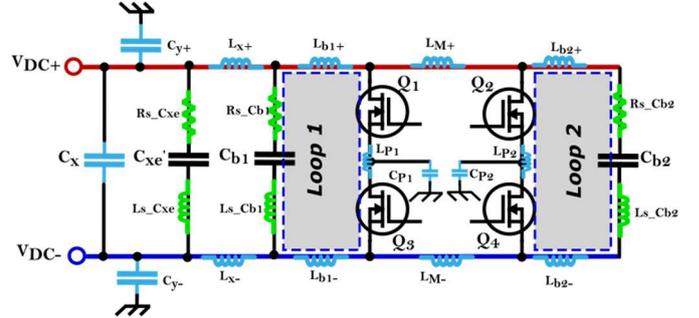


Fig. 2. Diagram of the EMC equivalent model on the power side

- the coupling capacitances between the DC bus potentials and ground ( $C_{y+}$  and  $C_{y-}$ ): they contribute to common mode filtering. They must be maximized and balanced also by the routing. This is also the case for  $C_x$ . Contributing to the differential mode filtering, the latter must be maximized. In [7] the effect of the imbalance between  $C_{y+}$  and  $C_{y-}$  capacitances in a Buck chopper has been studied.

- the coupling capacitances between the medium potentials of the switching cells and ground ( $C_{p1}$  and  $C_{p2}$ ): these floating potentials are the cause of common mode disturbances in the frequency range from 150 kHz to a few MHz [3]. These couplings must also be minimized by routing.

In general, inductive power/control power/power and control/control couplings are to be optimized by routing and placement.

### B. Routing

Since there are many possible placements depending on the PCB technology, the one proposed here is suitable for a simple two-layer PCB. Thus, all components are surface mounted and placed on one side according to the schematic layout shown in (Fig. 1 b). Constrained by the small footprint of the active components, the thickness of copper that can be used is  $35\mu\text{m}$ . In order to optimize the parasitic effects some routing rules have been respected:

- placing the DC bus potentials and the ground plane on adjacent layers to maximize the  $C_{y-}$  and  $C_{y+}$  capacities.
- bringing the elements of a switching loop (switching cell and  $C_{bi}$ ) as close as possible in order to minimize the equivalent impedance of the loop.
- reducing as much as possible the coupling surface between the ground plane and the planes representing the potentials at the midpoint of the cells.
- reserving an equivalent coupling surface between the midpoint potentials and the ground plane in order to guarantee the symmetry of the  $C_{pi}$  capacitances. Equation (1) gives the coupling capacitance between two planes:

$$C = \epsilon_0 \epsilon_r \frac{S}{d} \quad (1)$$

where  $\epsilon_0$  is the permittivity of vacuum ( $\frac{1}{36\pi} 10^{-9}$ ) and  $\epsilon_r$  is the relative permittivity of the dielectric (in this case FR4 ( $\epsilon_r \approx 4$ )).  $d$  is the distance between the two plates, in this case the thickness of the dielectric (i.e. 1.5 mm on our PCB).  $S$  is the coupling area between the potentials.

Finally, the circuit was routed to ensure some symmetry between the two switching cells.

The top side of the routing is shown in Fig. 3 where  $C_{xe'}$  is reduced to a single capacitor. In order to improve the current density, the midpoint tracks ( $P_1, P_2$ ) of the top layer are connected by vias to much larger planes on the bottom face. The capacitor  $C_{xe'}$  is placed at  $DX = 13$  mm from  $C_{b1}$ . The distance contributing to determine the value of  $L_m$  separating the two arms is  $DM = 11$  mm.

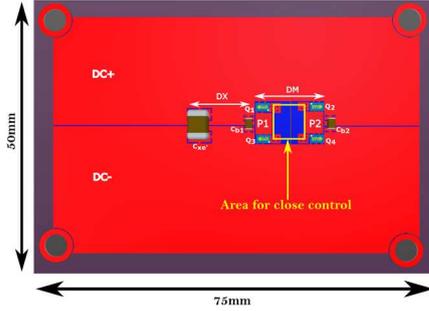


Fig. 3. Full Bridge converter top side routing

### III. SIMULATION AND EXPERIMENTAL VALIDATION

This section describes the simulation tool used and the methodology of the experimental measurements. A comparison is made between the experimental results and those obtained by simulation.

#### A. Instrumentation

The KEYSIGHT E4990A impedance analyzer is used. It is calibrated by Open/Short/Load standards and configured for a 'measurement time = 3', corresponding to the precision and speed of acquisition. The frequency sweep is performed between 100 kHz and 120 MHz. It is associated with KEYSIGHT 42941A probe. A SMA connector compensation kit is used for these measurements. Fig. 4 shows the test card.

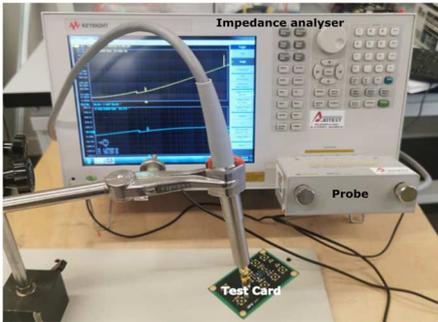


Fig. 4. Photograph of the measuring bench

#### B. Methodology for using Q3D extractor

Q3D is a simulation tool produced by ANSYS allowing the extraction of parasitic resistances, inductances, capacitances, conductances (RLCG) of a routed circuit. It is equipped with a 3D quasi-static electromagnetic field solver based on the method of moments [9]. The elements extraction is done by a frequency sweep. Fig. 5 shows the variation of

the inductance as a function of the frequency. The difference between the asymptotic AC and DC values is a consequence of the skin and proximity effect.

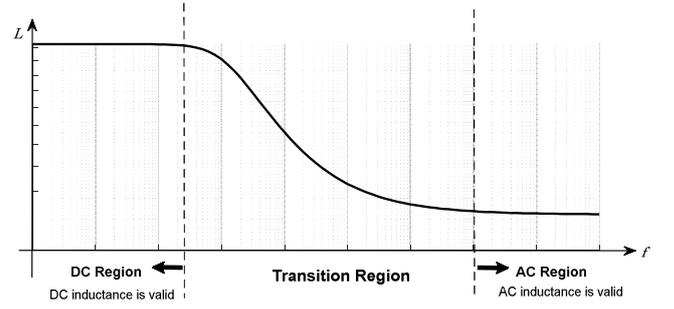


Fig. 5. Inductance of a conductor as a function of frequency [10]

It is the asymptotic value in the AC region that is taken into account for offsetting up the model since the frequency equivalent to the rise times ( $t_r$ ) of the transistors is high ( $f_{req} \sim 0.35/t_r$ ). This corresponds to about 70 MHz for a rise time of 5 ns for example.

In Q3D, the active and passive components are not simulated. Depending on the extraction, open circuits or short circuits represent them. The impedances to be extracted are on the other hand the partial track impedances between the pads represented under the software. The direction of current flow is necessary to determine which pad is source or sink. This method neglects any inductive coupling of the tracks with the passive components actually implemented on the PCB.

#### C. Experimental measurement vs. simulation

In a first step, we will compare the predictions from Q3D of a test card with measurements. For this purpose, the diagram in Fig. 6 representing the wiring of the converter is proposed. In this wiring, the transistors are disconnected and their location left in open circuit. The capacitor  $C_{xe'}$  is replaced by an SMA connector from which the measurement will be made. The  $C_{bi}$  capacitors are SMD capacitors 1.5  $\mu$ F / 50V, X7R class insulation ref (CGA4J3X7R1H155K125AB). This capacitor has been previously characterized and integrated in the equivalent model.

The following expressions can be derived:

$$L_1 = L_{x+} + L_{x-} \quad (2)$$

$$L_2 = L_{b1+} + L_{b1-} + L_{M+} + L_{M-} + L_{b2+} + L_{b2-} \quad (3)$$

The two resonance frequencies ( $f_{r1}, f_{r2}$ ) and the antiresonance frequency ( $f_a$ ) resulting from the impedance curve are calculated as follows:

$$f_{r1} \approx (2\pi\sqrt{L_{r1} * (C_{b1} + C_{b2})})^{-1} \quad (4)$$

$$f_{r2} \approx (2\pi\sqrt{L_{r1} * C_{b1}})^{-1} \quad (5)$$

$$f_a \approx (2\pi\sqrt{L_{r3} * (C_{b1} + C_{b2}) / (C_{b1} * C_{b2})})^{-1} \quad (5)$$

$$L_{r1} = L_1 + L_{s_{cb1}}, \quad L_{r2} = L_2 + L_{s_{cb2}} \quad (6)$$

$$L_{r3} = L_2 + L_{s\_Cb1} + L_{s\_Cb2} \quad (7)$$

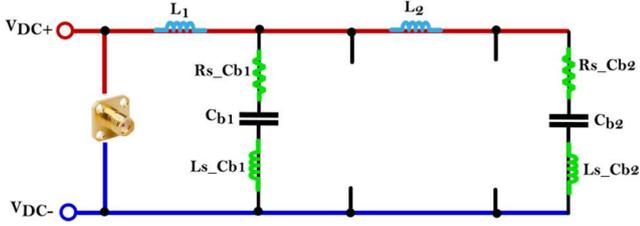


Fig. 6. Equivalent diagram for the measurement of the parasitic inductances of the power tracks

It is intuitively assumed that  $L_1 < L_2$  and  $L_{s\_Cb1} \approx L_{s\_Cb2}$ . The ESLs of the capacitors being known by their characterization, it is incumbent to measure  $L_1$  and  $L_2$ .

Fig. 7-a and b compare the  $L_1$  and  $(L_1 + L_2)$  inductances obtained by the experimental measurement and the Q3D simulation. To measure  $L_1$ ,  $C_{b1}$  is shorted and  $C_{b2}$  is disconnected from the schematic in Fig. 5. The reverse operation is applied to measure  $(L_1 + L_2)$ .

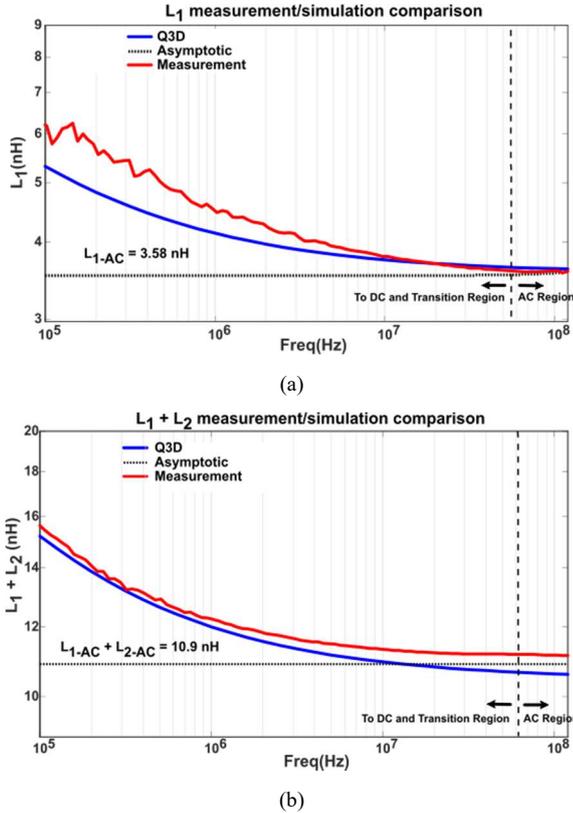


Fig. 7  $L_1$  inductance measurement (red) compared to the simulation (blue) and to the asymptotic value (black dotted line):  $L_1$  (a) and  $L_1 + L_2$  (b)

TABLE I compares the asymptotic values in small signals of  $L_1$  and  $L_1 + L_2$  obtained in simulation and experimentally.

TABLE I: COMPARISON SIMULATION/MEASUREMENT OF ASYMPTOTIC VALUES IN SMALL SIGNALS

	$L_1$ (nH)	$L_1+L_2$ (nH)
Q3D	3.5	10.5
Measure	3.6	10.9

The previous results allowed to plot the impedance curve of the diagram in Fig. 6 seen from the SMA connector and presented in Fig. 8. The curves of the model are not damped since the value of the resistances are not taken into account.

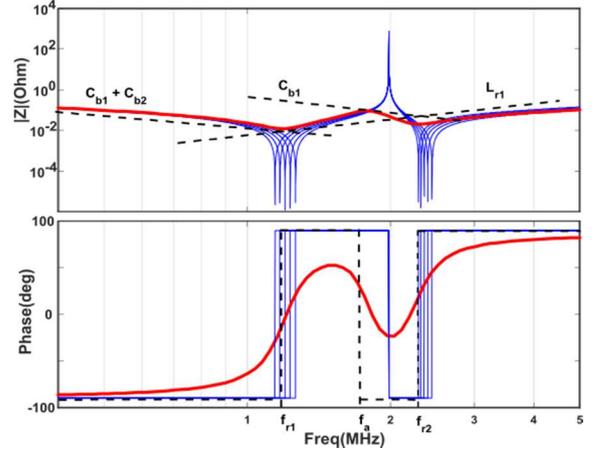


Fig. 8. Measured impedance (red), model (blue): variation of  $L_1$  to  $\pm 20\%$  at the turn of the measurement, asymptotic trend (black dotted line).

The maximum relative error of the simulation compared to the measurement is less than 4%. This maximum relative error as well as the similarity of the measured and calculated impedance curves in Fig. 8 show that it is possible to have a satisfactory confidence in the results from the Q3D simulation of the parasitic components of a routing; the simulation accuracy is satisfactory. We will rely on these results from now on.

These global measurements being validated, the different partial elements calculated are presented in TABLE II.

TABLE II: VALUES OF THE PARASITIC ELEMENTS OF THE EMC MODEL

Partial inductances (nH)									
$L_{x+}$	$L_{x-}$	$L_{b1+}$	$L_{b1-}$	$L_{M+}$	$L_{M-}$	$L_{b2+}$	$L_{b2-}$	$L_{p1}$	$L_{bp2}$
1.7	1.8	0.5	0.5	2.5	2.4	0.5	0.5	1.1	1.2
Parasitic capacities (pF)									
$C_{y+}$	$C_{y-}$	$C_{p1}$	$C_{p2}$	$C_x$					
26	30	7.3	7.2	4.3					

Although  $DM < DX$ ,  $L_{M+/-} > L_{X+/-}$ . This disparity is due to the fact that the two tracks  $L_{x+}/L_{x-}$  are much closer together than the tracks  $L_{M+}/L_{M-}$ . This closeness allows a reduction of the resulting inductances under the effect of the mutual. As discussed in Section 2, this analysis shows the importance of routing for noise optimization.

The equivalent inductance of each switching loop is about 2.2 nH. To this value, the parasitic packaging inductances of the transistors and capacitors will be added.

#### IV. EMC ANALYSIS

Upstream of the model presented in Fig. 2, a Line Impedance Stabilization Network (LISN) is added Fig. 9. In this case, it essentially allows fixing a propagation path to the conducted perturbations. It is simplified in order to measure directly the common mode ( $I_{cm}$ ) and differential mode ( $I_{dm}$ ) currents.

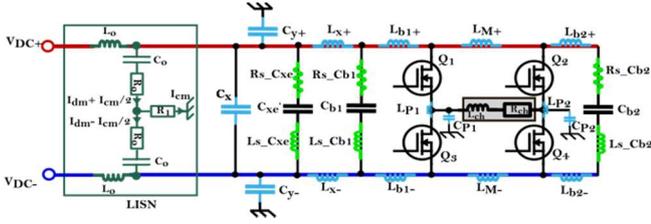


Fig. 9 Complete power model with an upstream LISN ( $R_0 = 27 \Omega$ ,  $R_1 = 39 \Omega$ ,  $C_0 = 220 \text{ nF}$  and  $L_0 = 250 \mu\text{H}$ )

In the following,  $C_{xe}$  is a  $47 \mu\text{F} / 50 \text{ V}$  capacitor. The simulation includes numerical models of the transistors provided by the manufacturer (*Ref EPC2055*). The transistors are controlled on switching on/off by  $2 \Omega / 5 \Omega$  gate resistors. The power circuit feeds an inductive load of  $100 \mu\text{H} / 1 \Omega$  and is simulated under LTspice. The average current in the load is  $12 \text{ A}$ .

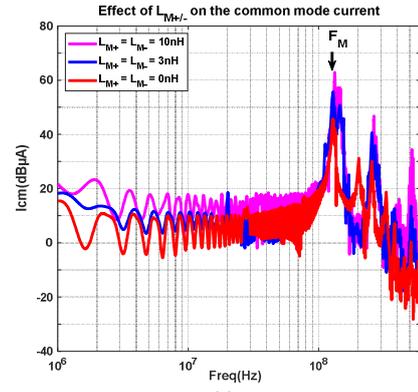
#### A. Effect of $L_{M+/-}$ intercells inductances

$L_{M+/-}$  inductances are not part of the switching loop. In this section, their effect is studied. For this purpose, the other parasitic elements are kept constant according to the results in TABLE II. Only the value of the intercellular inductances  $L_{M+}$  and  $L_{M-}$  is a parameter. This is a consequence of possible variations of the DM distance in Fig. 3.

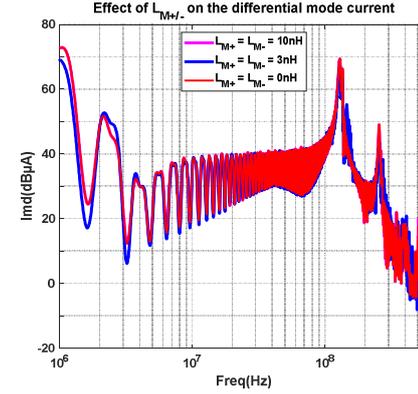
Fig. 10-a and b show the spectra of the common and differential mode currents as a function of  $L_M$  values, for a variation of  $L_{M+/-}$  from  $0 \text{ nH}$  to  $10 \text{ nH}$  ( $L_{M-} = L_{M+}$ ) i.e. a variation of DM from  $0 \text{ mm}$  to about  $43 \text{ mm}$ .

An increase in the level of the disturbance spectra is recorded in common mode. This increase exists in the frequency band above MHz. For the chosen operating point, the  $F_M$  resonance frequency remains constant ( $\sim 130 \text{ MHz}$ ) as a function of  $L_{M+/-}$  but its amplitude varies in the same direction as  $L_{M+/-}$  ( $46 \text{ dB}$  to  $62 \text{ dB}$ ). Indeed, this peak in the frequency spectrum corresponds to the resonance of the voltage across the transistors when they are switched-off. In differential mode, increasing  $L_{M+/-}$  decreases the spectrum by a few MHz at the resonance frequency, which is similar to a contribution to differential mode filtering. This high amplitude, high frequency CM resonance could lead to severe radiated emissions that would require specific reduction methods.

For unbalanced  $L_{M+/-}$  values, ( $L_{M+} \neq L_{M-}$ ), Fig. 11 a and b allow us to observe the influence of this unbalance especially on the common mode. Thus, we can observe on this spectrum, an increase in the amplitude of harmonics in the frequency band between  $10$  and  $90 \text{ MHz}$  of the order of  $5 \text{ dB}$  for a deviation of  $2 \text{ nH}$ . However, in the differential mode, a slight difference between the spectra can be seen, even if it is not as obvious as in the common mode.

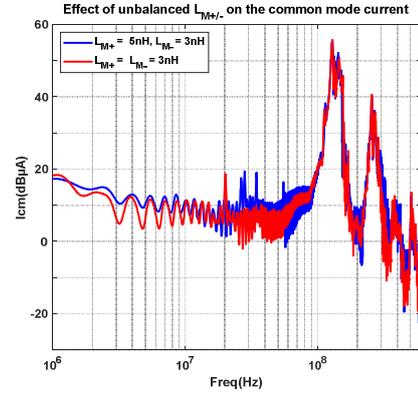


(a)

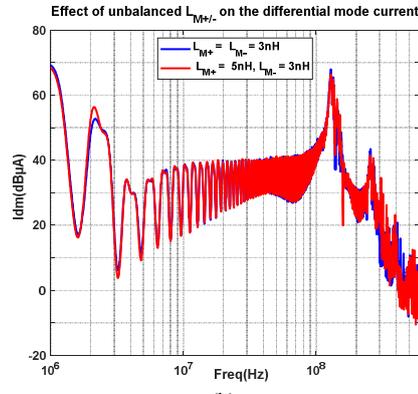


(b)

Fig. 10. Common (a) and differential (b) mode current as a function of  $L_{M+/-}$



(a)



(b)

Fig. 11. Effect of  $L_{M+/-}$  unbalance on common mode (a) and differential mode (b) current

### B. Discussion of the influence of $L_{M\pm/}$

The previous study is performed for a single operating point and for the specified load. The results presented above actually show the importance that must be given to the  $L_{M\pm/}$  inductances. However, subject to experimental validation, all parasitic inductances inherent to the full bridge must be taken into account in the same way as the switching loop impedances during design.

Reducing these inductances means bringing the switching cells closer together by acting on the DM distance. Even if this work does not address the thermal aspect, a compromise must be found between EMC and thermal during the final routing. This will force to find an optimal value of DM in order to reach these two objectives.

### V. CONCLUSION

We undertook this study in order to identify the main sources of disturbances and their effects from the design phase of the future power supplies of the SOLEIL Synchrotron and thus better understand their EMC constraints.

They are constituted by a full bridge DC-DC converter and based on the use of GaN components. The use of Q3D for the estimation of the parasitic by simulation has given results consistent with the experimental measurements. These measurements allowed building a partial EMC model of the power structure. Finally, a study on the effect of the intercellular parasitic inductances (specific to this structure because they are located between the switching cells) on the EMC behavior has been performed. This study shows that in order to improve the EMC behavior, the reduction of the inter-cell parasitic impedances is as important as the reduction of the switching loops areas. This reduction requiring the approach of the switching cells must not obviously degrade the thermal aspects. The developed model does not take into account the parasitic resistances of the routing; a better damping of the resonance peaks can be expected. The experimental validation of the effect of  $L_{M\pm/}$

and the damping of the impedance curves will be the subject of future work.

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