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Abstract

P and N type polycrystalline silicon has been applied in thin film transistors for driving all kinds of displays, and for building up CMOS-like circuits. For one aspect, the high driving current is required, which is usually achieved by improving field effect mobility of the active layer. For another aspect, balanced electrical characteristics are required for achieving

CMOS-like logic circuits. In this article, in order to increase driving current, P and N type polycrystalline silicon vertical thin film transistors (TFTs) configuration is proposed that can get rid of the strict requirement of the field effect mobility in order to increase the driving current. In addition, the balanced electrical properties are demonstrated for P and N type vertical TFTs, which are elucidated by the density of states (DOS) calculations. The simple SPICE modelling indicates the potential application in CMOS inverter based on our vertical TFTs.

Key Words: polycrystalline silicon, vertical thin film transistor, complementary circuits, density of states

Introduction

Polycrystalline silicon has been applied in a variety of domains, such as in solar cells [1], near-infrared photodetectors [2], low-cost electrical circuits [3, 4], and so on. Polycrystalline silicon has also been widely employed as the active layer of thin film transistors (TFTs) [5, 6], which are adopted as the switching transistor and the driving transistor in active matrix liquid crystal display (AMLCD) [7], active matrix organic light-emitting diode (AMOLED) display [8], electrophoretic display (EPD) [9]. The advantage of applying polycrystalline silicon TFTs for driving transistors lies in its

high driving capability, which is usually achieved by increasing grain sizes through methods such as excimer laser annealing (ELA) [10], metal-induced lateral crystallization (MILC) [11]. However, these two methods have their own shortcomings. A more common approach is adopting the solid phase crystallization (SPC) method, with a maximum temperatue of 600^{o}C [12]. Aiming to further increase the driving current, polycrystalline silicon vertical TFTs were proposed with a higher channel width/length ratio, while source/drain are positioned at the bottom and on top of the configuration, as shown in figure 1. In figure 1, P+ and N+ stand for P type heavily-doped polycrystalline silicon layer and N type heavily-doped polycrystalline silicon layer, which works in P type vertical TFT and N type vertical TFT, respectively. The channel length is defined by the barrier layer thickness between source and drain, and the channels are positioned on the sidewalls that are formed by dry etching. Note that, after patterning, there are two teeth in schematic figure 1, which owns four sidewalls, and correspondingly, there are four channels on the four sidewalls, which function as multi-gate TFTs that helps to further increase the drive current. This article deals with the electrical characterizations of the symmetric P and N type polycrystalline silicon vertical TFTs, and uses density of states (DOS) to elucidate the electrical parameters of P and N type polycrystalline silicon vertical TFTs. In addition, a simple SPICE modelling is proposed to show the potential application of CMOS logic gates.

Device Fabrication

Our work is based on a 600ºC fabrication process, which is compatible with special glass substrates, such as Corning 1737 glass substrates, and further work can be on the reduction of processing temperature by other techniques, such as the plasma enhanced chemical vapor deposition (PECVD) technique. In the primary study, silicon wafers were employed to guarantee the endurance of a high processing temperature. The P and N type polycrystalline silicon vertical TFTs were fabricated by a five-mask process, and polycrystalline silicon layers were formed by a low pressure chemical vapor deposition (LPCVD) method followed by a solid phase crystallization (SPC) step at 600ºC for 12 hours. In addition, a P type or N type polycrystalline silicon layer was formed by *in situ* doping, where silane SiH_4 gas flow was injected accompanied by diborane B_2H_6 or phosphine PH_3 precursor. The five-mask fabrication process is carried out as follows:

(1) Initially, two-inch (100) silicon wafers were adopted as the substrates, which are cleaned by standard RCA cleaning steps. After that, thick silicon oxide layers were deposited on the wafer substrates by using the atmospheric pressure chemical vapor deposition (APCVD) method. Afterward, four different layers were sequentially deposited, including a P type or N type heavily-doped polycrystalline silicon layer by LPCVD and

SPC, a 100 nm silicon oxide layer deposited by APCVD, a 1 μm thick undoped polycrystalline silicon layer by LPCVD and SPC, and another P type or N type heavily doped polycrystalline silicon layer. For the four layers stacking, the combination of a thin SiO_2 layer and thick undoped polycrystalline silicon layer worked as the barrier layer, the thin SiO_2 layer was adopted in order to ease the dry etching process due to the high etching selectivity between SiO_2 and polycrystalline silicon, and the thick undoped polycrystalline silicon layer was employed to guarantee a high channel length in order to minimize short channel effects.

(2) The four layers' stacking is dry etched by reactive ion etching (RIE), with a low pressure of 1 mTorr, a high power of 50 Watts, and a gas flow of 10 sccm using SF_6 as an etchant. As a result, physical bombardment dominates over chemical erosion during the RIE process, in order to form continuous sidewalls for active layer deposition.

(3) After that, another RIE process is carried out, the partial etching reaches the bottom heavily-doped polycrystalline silicon layer, with the aid of a laser interferometer, in order to discriminate source and drain.

(4) Thereafter, a 150 nm thick undoped polycrystalline silicon thin film is deposited by LPCVD and SPC, and the RIE process is carried out to pattern the active layer on the sidewalls.

(5) After that, another RCA cleaning step is carried out, in order to eliminate most of the defects at the active layer/gate oxide layer interface.

Then, a 70 nm thick gate oxide layer is deposited by APCVD, followed by a densification process at 600ºC for 12 hours. Thereafter, the fourth mask is used to form contact holes for the source and drain.

(6) Finally, a thick aluminum layer is deposited by thermal evaporation and patterned by the fifth mask to form source, drain and gate contact pads.

For complexity of the fabrication process for vertical TFT, it needs four layers' stacking for vertical configuration, in contrast, to our state of art lateral TFT, it needs only two layers' stacking of doped and undoped polysilicon. For masks numbers, our vertical TFT needs 5-mask process, while for lateral TFT, it only needs 4-mask process. The vertical TFT shows higher complexity in comparison to lateral TFT. However, the scaling capability can be large in comparison to the lateral TFT. In fact, for vertical TFT and lateral TFT with the same area of $30\lambda^2$ (λ is design rule) that are designed in our laboratory, the W/L can be 36 times larger for vertical TFT, which shows its higher driving capability. For the chosen multi-tooth vertical TFT, the channel width/length ratio is 80 μm/1.1 μm, and all the characterizations were carried out by an Agilent B1500 semiconductor parameter analyzer in ambient air.

Results and discussion

After fabrication, the polycrystalline silicon vertical TFTs were electrically characterized, and figure 2(a) shows the transfer characteristics

for P and N type vertical TFTs at different drain-source voltages. For P type vertical TFTs, drain-source voltage is -1 V, -100 mV, or -10 mV, and for N type vertical TFTs, drain-source voltage is 1 V, 100 mV, or 10 mV. The deduced electrical parameters are shown in Table 1. The threshold voltage V_{th} and effective mobility μ_{eff} were deduced from the following current formula:

$$I_{ds} = \frac{W}{L} C_{ox} \mu_{eff} (V_{gs} - V_{th} - \frac{1}{2} V_{ds}) V_{ds} \quad (1)$$

Where W/L is the channel width/length ratio, C_{ox} is the gate capacitance per unit area, V_{gs} and V_{ds} are gate-source voltage and drain-source voltage, respectively. The V_{th} is extracted by the extrapolation of I_{ds}-V_{gs} relationship, the intercept on the V_{gs} axis is approximately the threshold voltage V_{th}, while the mobility μ_{eff} can be extracted from the slope of I_{ds}-V_{gs} relationship (transconductance g_m) by the following relationship:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{W}{L} \mu_{eff} C_{ox} V_{ds} \quad (2)$$

given that W/L, C_{ox}, and V_{ds} are known. Note that, additionally to short channel effects (SCEs), DIBL can be considered, even with a large channel length of 1.1 μm and a small drain-source voltage of less than 0.1 V. Indeed, for polycrystalline silicon vertical TFTs, the carrier concentration of channel layer is low due to the trapping effect of carriers at the grain boundaries, the depletion widths of the source and drain junctions are relatively large. Therefore, the depletion regions of drain and source

junctions conjoint with a relatively large channel length and lower drain voltage.

The electrical parameters were listed in Table 1. Several conclusions can be drawn: (1) for different V_{ds}, the electrical parameters are almost the same, except that the transconductance g_m is proportional to the V_{ds}, and the I_{on}/I_{off} reduces at larger V_{ds} for N type vertical TFTs, However, for P type vertical TFTs, I_{on}/I_{off} are almost the same for different V_{ds}. Therefore, the short channel effects are more serious for N type vertical TFTs when V_{ds} increases to 1V; (2) for P type vertical TFTs, the threshold voltage is approximately -16V, and for N type vertical TFTs, the threshold voltage is approximately 11V, while the flat band voltage is approximately -3V for both P and N type vertical TFTs (taken approximately as the gate voltage at the minimum drain current I_{ds}). The nearly same deep trap density can also be verified by the nearly same subthreshold slope, which is 2.1 V/dec for P type vertical TFT and 2.4 V/dec for N type vertical TFT; (3) the effective mobility is approximately 3.1 $cm^2/V•s$ for P type vertical TFTs, while it is approximately 5 $cm^2/V•s$ for N type vertical TFTs, indicating the shallow trap density of N type vertical TFT is slightly smaller than the P type vertical TFT, as slightly more free carriers contribute to the transport. The deep and shallow trap density will be further elucidated by density of states (DOS) calculation, which will be shown later. In order to eliminate the short channel effects, the smaller V_{ds} is adopted. In the following

calculations, the V_{ds} is always set to be -10 mV for P type vertical TFTs, and 10 mV for N type vertical TFTs. Nevertheless, symmetric parameters were obtained. The symmetric parameters are mainly due to that the fabrication processes of P and N type vertical TFTs are in the same run with the same device structure. The vertical configuration adopts the same etching conditions to achieve the sidewalls, and the similar active layers are deposited on the sidewalls.

The device is operating at a high gate voltage of ±25V, which can be reduced by adopting a different gate dielectric layer with high gate capacitance and large equivalent oxide layer thickness, which can be achieved by reducing gate oxide layer thickness and adopting high dielectric constant materials, or by using electric double layer electrolyte.

Prior to the DOS calculation, the contact resistance should be considered, as it may affect the apparent electrical parameters and DOS accuracy. The contact resistance can be calculated by a simple relationship:

$$R_{total} = \mathrm{R}_{\mathrm{contact}} + \frac{L}{WC_{ox}\mu_{\mathrm{eff}}} \cdot \frac{1}{V_{gs} - V_{th}} \quad (3)$$

As shown in figure 2(b) and 2(c), the contact resistance of P and N type vertical TFTs are demonstrated. The calculated mobility is the intrinsic mobility without contact resistance. For P type vertical TFT, the contact resistance is approximately 1553 Ω, and the deduced effective mobility that eliminates contact resistance is approximately 3.5 $cm^2/V•s$. For N type vertical TFT, the contact resistance is approximately 363 Ω, and the

deduced effective mobility that eliminates contact resistance is approximately 5 $cm^2/V•s$. The deduced effective mobilities for this method are a little larger than the nominal effective mobilities by the extrapolation method, which are 3.1 $cm^2/V•s$ for P type vertical TFT and 4.7 $cm^2/V•s$ for N type vertical TFT. In order to show the accuracy of the deduced contact resistances, a derivative transfer line method (TLM) based on varied channel widths W of 20 μm, 40 μm, 80 μm and fixed channel length of 1.1 μm has been studied. As shown in figure 2(d) and 2(e), due to the total resistance is inversely proportional to the channel width W, the deduced contact resistances are negative, which indicates that the contact resistances are negligible. Considering that the contact resistance is much smaller than the total resistance, and the effective mobilities can fit quite well, the contact resistance should not greatly affect the electrical parameters. In addition, in order to accurately evaluate the threshold voltage, the second-derivative method [13] is adopted, as shown in figure 2(f) and 2(g). Even though the large noise, the threshold voltage can be deduced to be approximately -19.1 V for P type vertical TFT, and 9.1 V for N type vertical TFT, which are close to the values of -16.7 V and 10.8 V for P and N type vertical TFTs deduced from the conventional extrapolation method. Therefore, the contact resistance does not greatly influence the electrical parameters, the DOS of P and N type vertical TFTs can be calculated and elucidate the electrical parameters.

The field effect mobilities for P type and N type vertical TFTs are demonstrated from transfer characteristics, which are shown in figure 2(h). The field effect mobility increases with gate bias, and the maximum field effect mobilities for P type and N type vertical TFTs are approximately 4 $cm^2/V\cdot s$ and 5 $cm^2/V\cdot s$, respectively, which can be comparable to the effective mobilities of P and N type vertical TFTs.

When the TFT is switched off, it works in the reversed diode mode that the diffusion current dominates, and the thermionic field emission of the carriers through grain boundary trap states may also work. The reversed current of the diode can be expressed as [14]:

$$J = \left(\frac{qD_n n_{p0}}{L_n} + \frac{qD_p p_{n0}}{L_p}\right)\left[1 - \exp\left(\frac{qV_{ds}}{kT}\right)\right] \quad (4)$$

Where D_n/D_p is the diffusion coefficient, n_{p0}/p_{n0} is minority carrier density at equilibrium state, L_n/L_p is the diffusion length. Therefore, the similar I_{off} of P and N type vertical TFTs is due to the similar carrier density in the channel layer, as well as the similar active layer morphology due to Poole-Frenkel effect.

As it is known that the trap density of states (DOS) is related to the electrical parameters, such as the subthreshold slope and the field effect mobility, the analysis of DOS is critical to elucidate the electrical characteristics. The DOS can be calculated from the following formulae [15]:

$$\exp(\frac{eu^a}{kT}) - \frac{eu^a}{kT} - 1 = \frac{q}{kT}\frac{\varepsilon_i d}{\varepsilon_s t_{ox} I_0}[V_{gs} I(V_{gs}) - \int_0^{V_{gs}} I(V_{gs}^{'}) dV_{gs}^{'}] \quad (5)$$

$$p(u^a) = \frac{\varepsilon_0 \varepsilon_i^2}{\varepsilon_s t_{ox} q}(\frac{dV_{gs}}{du^a}) \quad (6)$$

$$N(E) = \frac{1}{q}(\frac{dp(u^a)}{du^a}) \quad (7)$$

Where u^a is surface potential, ε_i is the relative permittivity of SiO_2, ε_s is relative permittivity of silicon, t_{ox} is oxide thickness, I_0 is flat-band current, V_{gs} (V'_{gs}) is gate voltage, ε_0 is the free space permittivity. The calculated density of states were shown in figure 3(a) and 3(b), respectively. From the figures shown, the DOS of P type vertical TFT varies from 10^{19} $eV^{-1}cm^{-3}$ to 10^{21} $eV^{-1}cm^{-3}$, corresponding to the surface potential from 0 eV to slightly less than 0.4 eV, where the DOS of N type Vertical TFT varies from more than 10^{18} $eV^{-1}cm^{-3}$ to 10^{22} $eV^{-1}cm^{-3}$, when the surface potential varies from 0 eV to more than 0.4 eV. The large deep trap density is associated with the high subthrehsold slope, which is mainly due to the inferior gate dielectric layer/active layer interface and the inferior active layer quality, where the active layer is deposited on the etched sidewall with a higher roughness. In previous work [16], the DOS is calculated by different methods, and the DOS varies from 10^{18} $eV^{-1}cm^{-3}$ to approximately 3×10^{22} $eV^{-1}cm^{-3}$ for E_F-E varied from 0 to 0.4 eV, the threshold voltage is approximately 4V, subthreshold slope is approximately 1.18 V/dec, and field effect mobility is approximately 11.0 $cm^2/V{\cdot}s$. In another work [17], the DOS varies from 10^{18} $eV^{-1}cm^{-3}$ to approximately 10^{23} $eV^{-1}cm^{-3}$ for E_F-

E varied from 0 to 0.4 eV. The threshold voltage is approximately 5.3 V, the subthreshold slope is 1.21 V/dec, and the field effect mobility is approximately 5.63 $cm^2/V{\cdot}s$. As mentioned in this manuscript, the DOS varies from 10^{18} $eV^{-1}cm^{-3}$ to more than 10^{22} $eV^{-1}cm^{-3}$ for E_F-E varied from 0 to more than 0.4 eV, the threshold voltage is approximately -3.4 V, the subthreshold slope is 2.4 V/dec, the field effect mobility is approximately 4.9 $cm^2/V{\cdot}s$. Compared with previous work [16], the DOS range is approximately the same for this work, however, the lower threshold voltage and the large subthreshold slope indicates the large deep trap density, especially at the gate dielectric layer/active layer interface, which may also affect the field effect mobility. Compared with previous work [17], the DOS is larger in work [17], however, the lower threshold voltage and larger subthreshold slope may also affect the field effect mobility from DOS calculation. In addition, from comparing previous work [16] and [17] where the almost same threshold voltage and subthreshold slope are obtained, the shallow trap DOS obviously affects the field effect mobility, with a higher mobility where DOS is lower. Nevertheless, the almost symmetric electrical parameters and DOS for P and N type vertical TFTs enable their usage in complementary MOS applications, such as in logic gates as inverters. For the similar DOS of P and N type vertical TFTs, the similar active layer morphology is obtained, and the similar active layer/gate oxide layer interface is also achieved by introducing an RCA

cleaning step before gate oxide layer deposition.

A simple simulation of an inverter with a SPICE tool has been carried out, as shown in figure 4. Figure 4(a) shows the fitting of the simulated transfer characteristics of P type vertical TFTs and N type vertical TFTs with the experimental transfer curves. The drain-source voltages were set to be ±0.1 V and ±1 V, and the good fittings are shown in subthreshold region and on-state region, while a bit of deviation is observed in the sub on-state region. Nevertheless, the symmetric transfer characteristics of P and N type vertical TFTs were obtained in the simulation. Figure 4(b) shows the voltage transfer characteristics of the simulated CMOS inverter, while the device configuration is demonstrated in the inset of figure 4(b). For V_{in} varying from 0V to 20V, V_{out} can vary from 14V to 3V, with the top electrode voltage V_{DD} being 20V. Note that, due to slightly asymmetric output characteristics of P and N type vertical TFTs, the reversed leakage current, as well as certain kink effect introduced in the SPICE model, the cross points shift to 14V and 3V for V_{OH} and V_{OL}. The asymmetry of output characteristics should be further improved, the reversed leakage current should be reduced, and the kink effect should also be suppressed, such as by introducing lightly-doped drain (LDD) structure [18]. In addition, the rise at low level can also be due to the reversed leakage current when the P type vertical TFT works in the off-state. The voltage gain is rather small, however, the primary inverter prototype is demonstrated. Figure 4(c)

shows the simulated transient property of the CMOS inverter, a relatively fast voltage inversion can be obtained, which shows its potential applications in certain domains, such as in ring oscillators. The fabrication and measurement of the inverter device can also be carried out, which can be the further work.

Conclusion

P and N type polycrystalline silicon vertical TFTs were fabricated and electrically characterized. Symmetric transfer characteristics were obtained, and the deduced electrical parameters were also symmetric, with slightly larger field effect mobility of n type vertical TFT than its p type counterpart. The contact resistance does not greatly affect the electrical parameters, as verified by the accurate threshold voltage deduction. DOS calculations show symmetric trap density, which indicates the potential applications in CMOS logic gates, and a simple SPICE modelling of the CMOS inverter has been carried out.

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Declaration of Interest Statement

There are no conflicts to declare.

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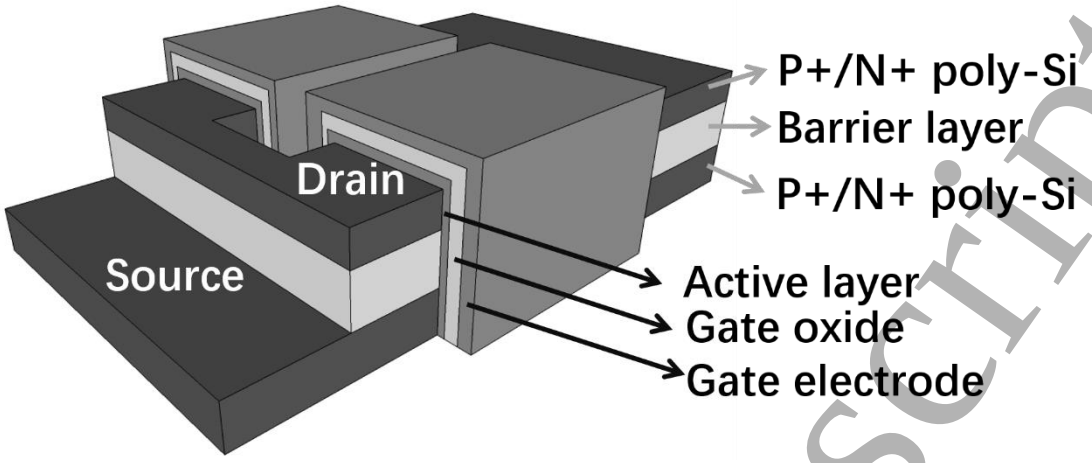
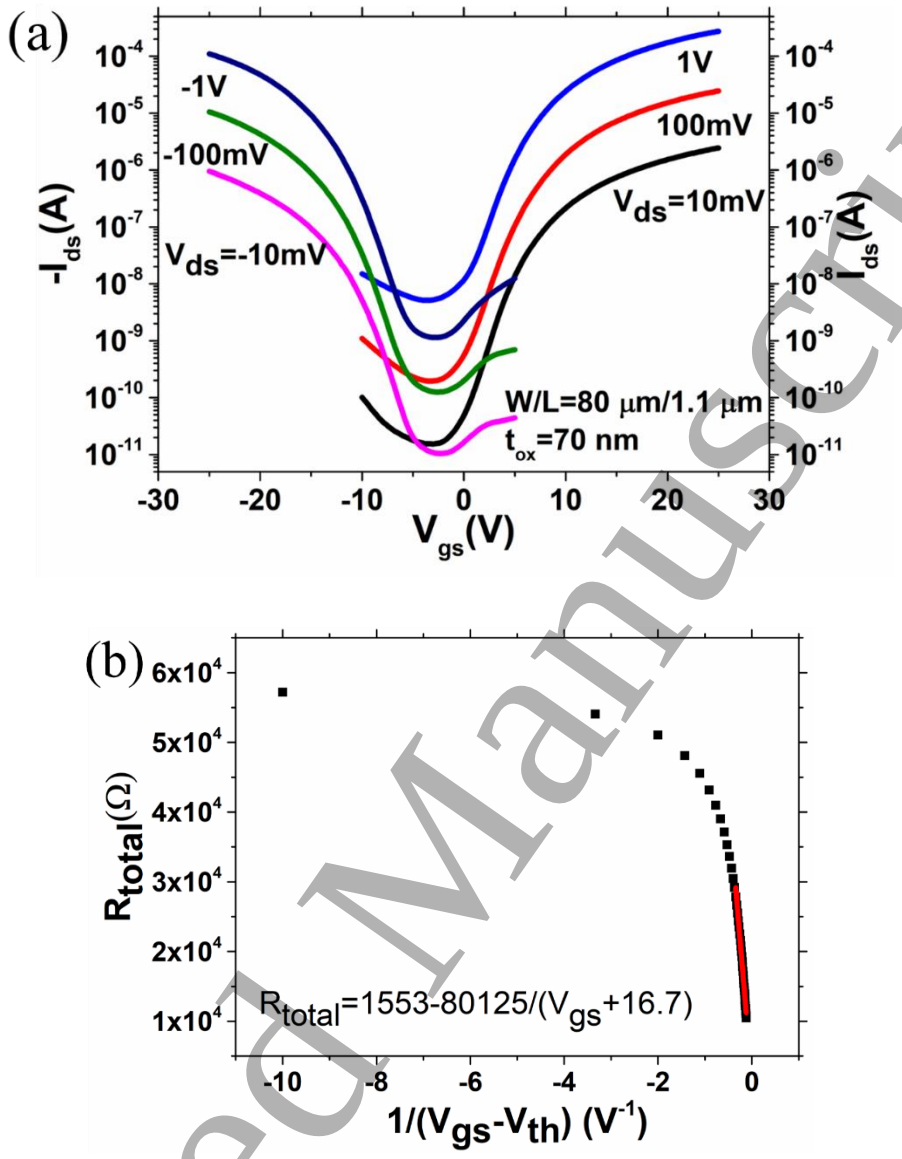
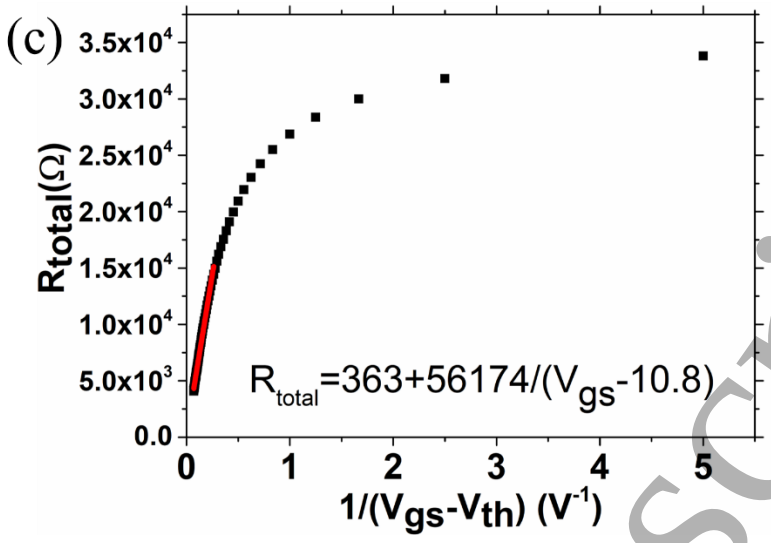
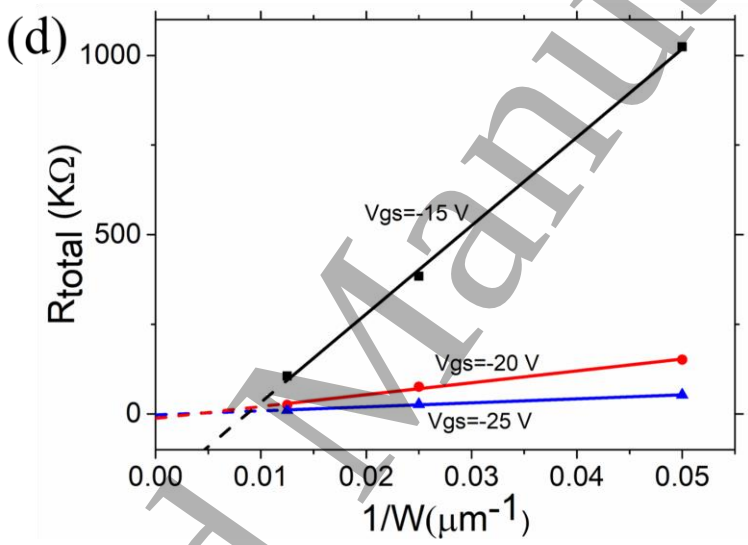
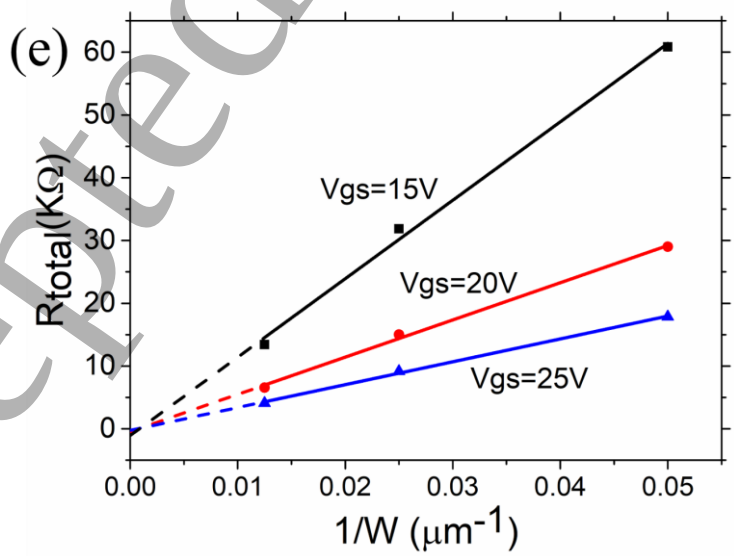


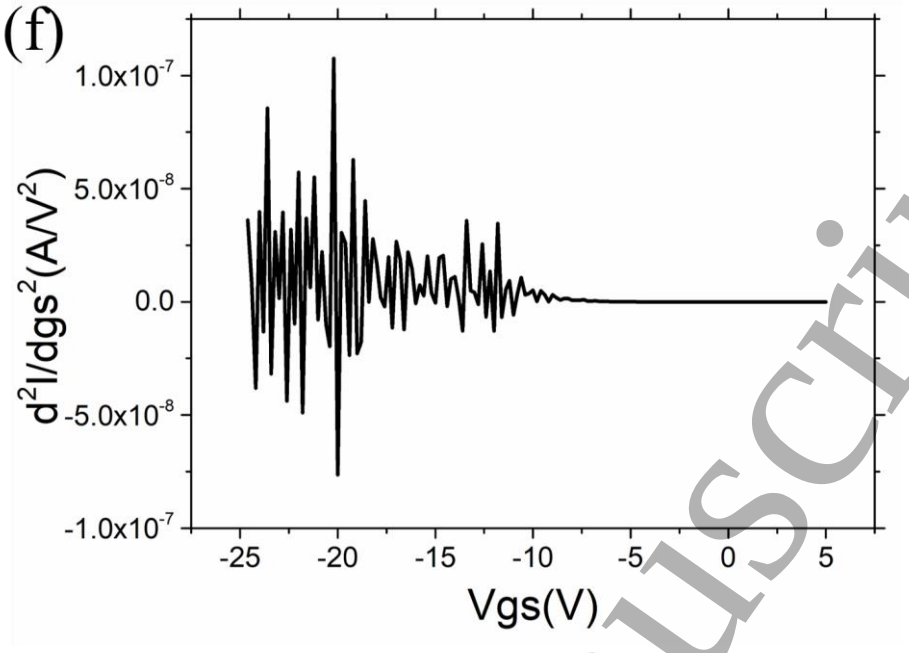
Figure 1: schematic view of the P and N type polycrystalline silicon vertical TFT.

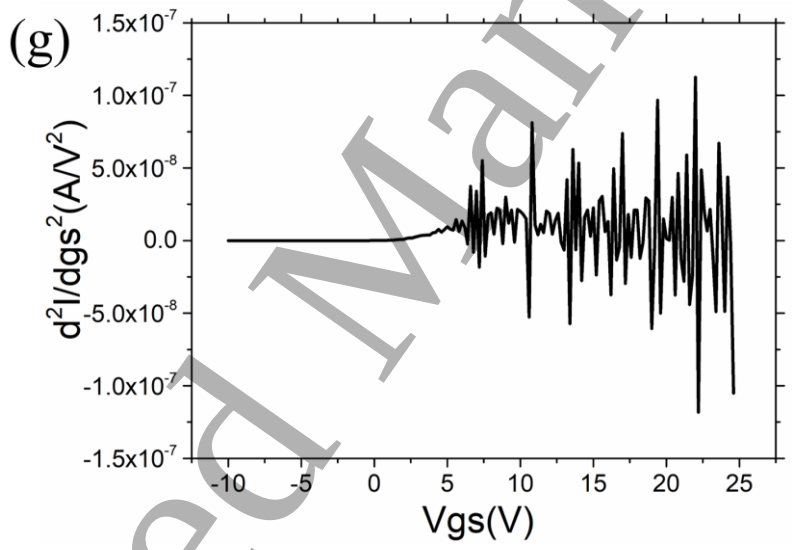












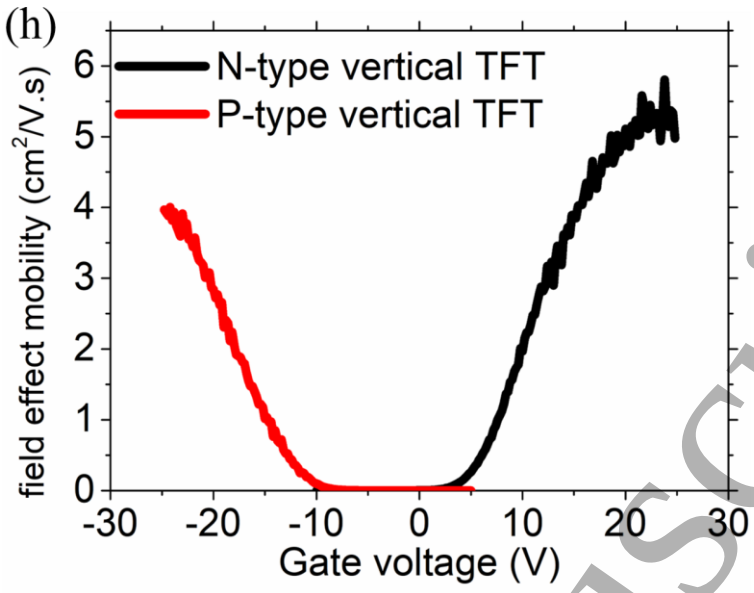


Figure 2: (a) transfer characteristics of P and N type vertical TFTs under different V_{ds} of ±10 mV, ±100 mV, and ±1V, (b) the contact resistance of P type vertical TFT, (c) the contact resistance of N type vertical TFT, (d) the contact resistance of P type vertical TFT by transfer line method (TLM), (e) the contact resistance of N type vertical TFT by transfer line method (TLM), (f) accurate threshold voltage extraction of P type vertical TFT, (g) accurate threshold voltage extraction of N type vertical TFT, (h) field effect mobilities for P type and N type vertical TFTs.

Table 1: Electrical parameters for P and N type polycrystalline silicon vertical TFTs.

Type	V_{ds}	I_{on}/I_{off}	V_{th}(V)	μ_{eff}(cm^2/V•s)	g_m(μS)	SS(V/dec)	V_{FB}(V)
P type	-1V	9.7×10^4	-15.8	3.2	11	2.1	-2.8
	-100 mV	8.4×10^4	-16.0	3.1	1.1	2.1	-2.6
	-10 mV	9.2×10^4	-16.7	3.1	0.11	2.1	-2.2
N type	-1V	5.4×10^4	10.8	5.3	19.1	2.4	-3.6
	-100 mV	1.3×10^5	11.2	4.9	1.7	2.4	-3.4
	-10 mV	1.6×10^5	10.8	4.7	0.17	2.3	-3.0

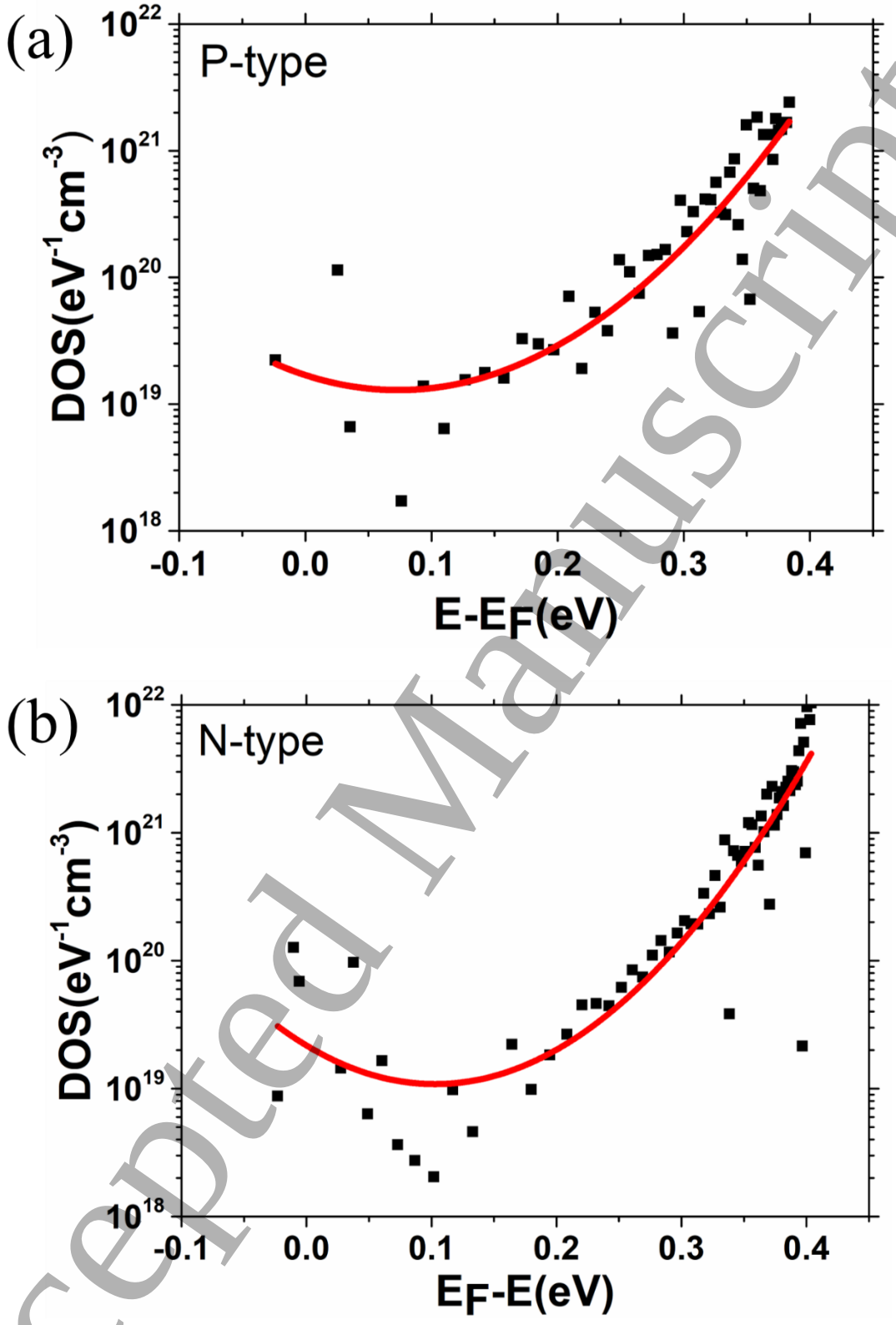
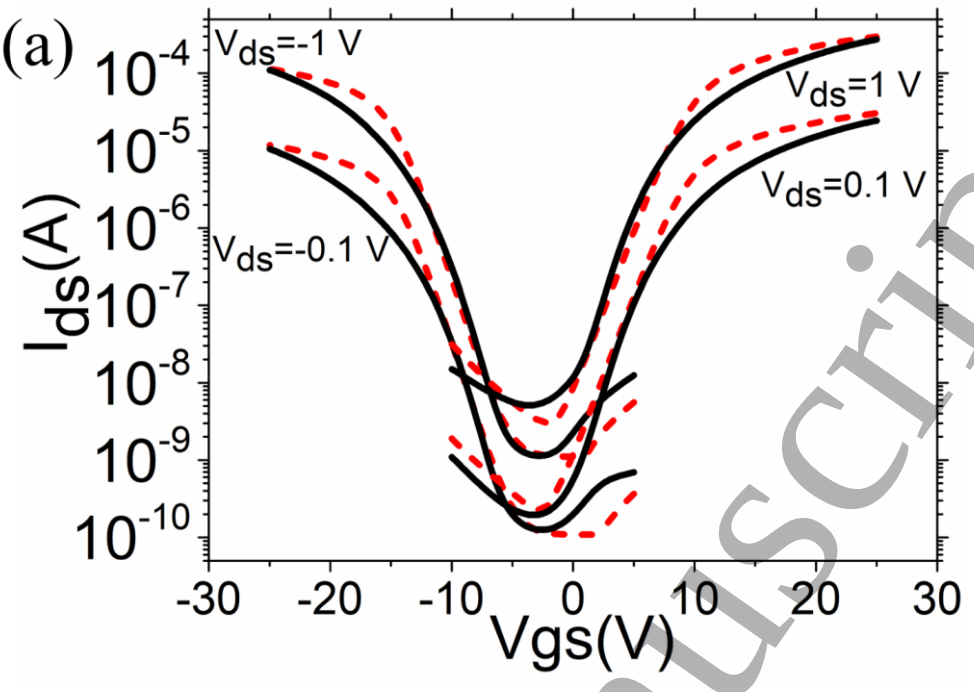
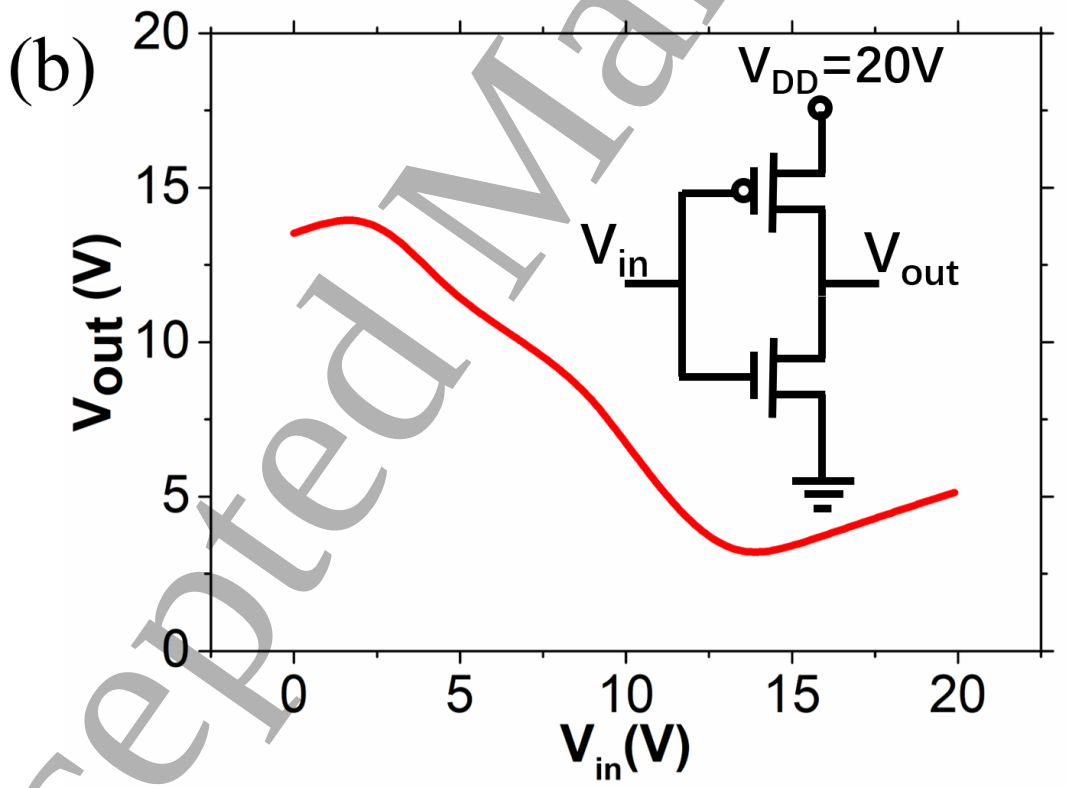


Figure 3: (a) DOS calculation for P type vertical TFT, (b) DOS calculation for N type vertical TFT.





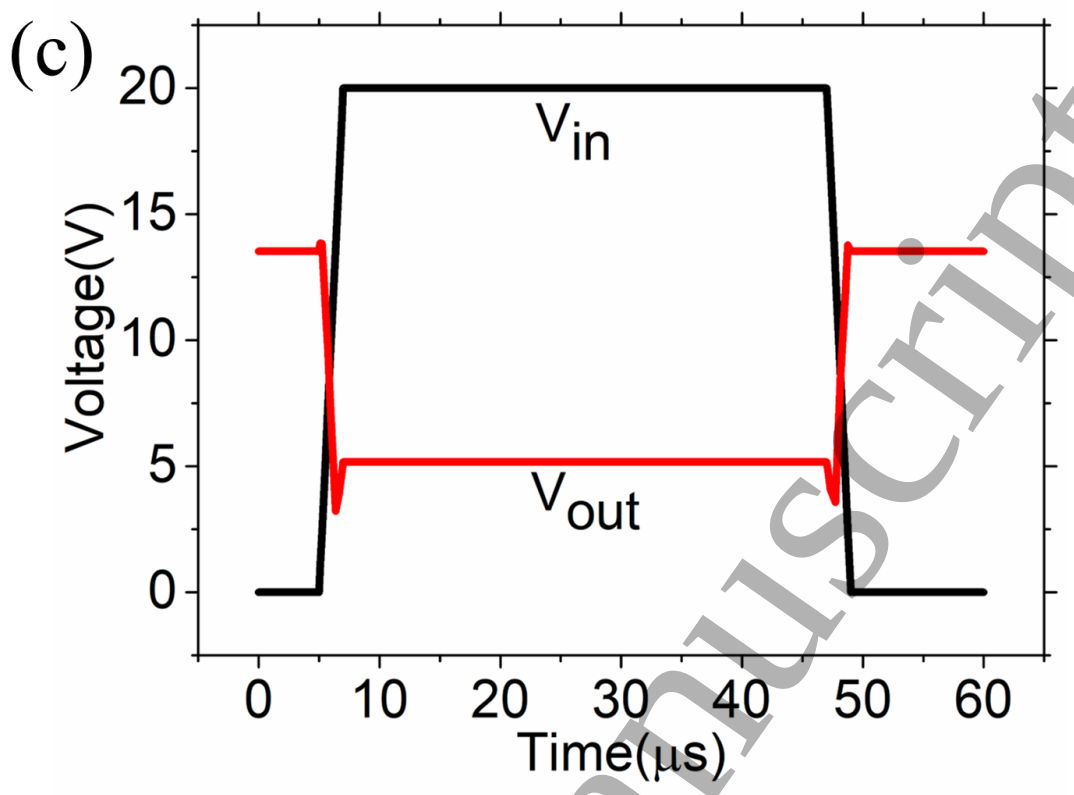


Figure 4: (a) SPICE simulated transfer characteristics of P and N type vertical TFTs by fitting the experimental transfer characteristics, the solid lines represent the experimental data, while the dotted lines represent the simulated data, (b) the simulated voltage-transfer characteristic for the inverter, the inset shows the CMOS inverter configuration, (c) the simulated transient property of the CMOS inverter.