A New Topology of DC-DC Converter Based On Piezoelectric Resonator

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Mustapha Touhami, *Student Member, IEEE*, Ghislain Despesse, and François Costa, *Member, IEEE*

***Abstract*- The emergence of new piezoelectric materials makes it possible to offer high performances in terms of power densities and integration. These new materials can be used in DC-DC power converters as solution to replace the magnetic components and to meet the growth in demand of miniaturization, high power densities and high efficiency applications. This paper deals with a new topology of a DC-DC converter based on piezoelectric resonator. The conversion mechanism, based on energy and charge balance, is explained in details through an analytical model and validated by experimental results. A prototype has been designed for an input-output voltage up to 250-125 V and a power range of 100 W. It provides an efficiency higher than 93% for wide operating points in radial mode vibration. As an example, we obtain an efficiency 93.8 % of for 250 -117 V input-output voltage at 50 W output power. In addition, the thickness mode operation is experimentally validated at 1 MHz, and exhibited a peak output power of 175 W with an efficiency of 80 % for 200 – 60 V input-output voltage. The experimental results show the promising performances of the proposed DC-DC power converter based on piezoelectric resonator for high- to-low voltage, high efficiency and low-to-medium power applications.**

I. INTRODUCTION

Nowadays, high efficiency and miniaturization in power electronics become essential due to the increase in demand of portable devices. A key part of the challenge is to reduce the size of passive components. Until now, the main way to get it was to increase the switching frequency, which reduces the size of energy storage components in power converters. Indeed, the volume of inductors, mostly used in power electronics, decreases when increasing the switching frequency [2]–[4]. However, magnetic properties of materials and heat transfer limit the scaling of the switching frequency [3], [4]. In addition, the on-chip integration of magnetic materials is quite complex or incompatible with the current fabrication processes [4]. Furthermore, the capacitors used as energy storage in power electronics can easily be integrated in monolithic structures, which can be assembled in parallel and/or in series from small cells to fit the requirements in terms of power and voltage [5], [6]. Moreover, switched capacitance converters (SCCs) can achieve high- power density for low-power applications (less than 1 W), which could be 100-1000 times greater than magnetic converters [5]. However, their efficiency drops significantly for variable gain, needing to operate at variable switching frequency for maintaining high efficiency over load variations [5], [6].

As the performance of piezoelectric materials increased in terms of quality and coupling factor, the piezoelectric resonators (PRs) and piezoelectric transformers (PTs) can be used to store temporarily the electrical energy in power converters in a mechanical form, which enable using these materials as a replacement to the magnetic components. In addition, the manufacturing process of piezoelectric components can be easier than electromagnetics since there is no winding or core assembly [7], [8]. Moreover, piezoelectric materials have planar shape, which makes them suitable for portable applications with low profile.

To increase the power density and reduce the size of DC-DC power converters, PTs were used to replace electromagnetic transformers in power supply applications having a high sensitivity to electromagnetic interferences such as medical equipment [9]–[11]. The conversion principle of PT is based on electromechanical energy coupling between the primary and secondary of PT. Indeed, PT's primary is used as actuator and the secondary as generator. However, most of topologies based on PTs need an additional inductor to operate in zero voltage switching (ZVS) to reduce power losses [12], [13]. However, [14]–[16] examine inductorless power converters based on PTs that can operate in ZVS but need specific conditions that limit the operating range.

A recent research showed a promising potential of piezoelectric resonators that could challenge the LC resonators [17]. Emerging inductor-less DC-DC converters based on single PR are presented in [18]–[20]. In [18]–[20], the PR operates with the same principle as switched capacitances, which conducts to inherit the same drawbacks as SCCs [6]. To overcome the abovementioned limits, a new conversion principle using PR based on energy and electric charge balance is introduced and fully demonstrated in [21], [22]. This principle is similar to variable capacitance power conversion shown in [23]. In steady state operation, the energy and charge balance is ensured during each conversion period while operating in soft switching by charging/discharging softly the inherent capacitance of PR which allows reducing power losses and EMI level [24]. A full design of a voltage step-down DC-DC converter, based on PR validates the conversion principle [22]. This is assessed by the comparison of simulation and experimental results. Furthermore, good performances are obtained in low-voltage with an efficiency up to 98.4 % for low

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power (< 1 W), [22]. Multiple topologies based on the same operating principle are shown in [1], [25]–[27], and high performances can be observed for high voltage conversion. This operating principle can be extended to PTs for isolated power converters [28].

In this paper, we introduce a new topology of step-down DC-DC inductorless converter based on PR that allows maximizing the energy transferred to the output load and ensuring high efficiency for high-to-low voltage and low-power applications. The operating principle is explained in detail, and an analytical model is demonstrated. Experimental results are also presented to validate the operating principle and the performance of our topology.

Thus, this paper is organized as follows: in section II, we describe the new topology of the DC-DC step-down converter and its operating principle throughout its switching sequences, over a period of conversion in steady-state operation. Section III presents an analytical model in steady-state operation with practical considerations. It should be noted that in this model, the damping effect of the PR is taken into account. Section IV shows the theoretical results obtained by the analytical model. Section V illustrates simulation results obtained with a SPICE model to validate the principle and the theoretical performances. Section VI exhibits the comparison of experimental results with those obtained by simulation. We finish with a conclusion presented at the end of the paper.

II. Converter Description

In this section, we introduce a new DC-DC converter based on piezoelectric resonator (PR). The electrical model of piezoelectric resonator is presented. The switching sequences of the converter are shown in steady state depending on the input and output voltages.

A. Circuit description

Fig. 1 presents a new DC-DC converter that includes six N-MOSFETs $S_{1, 2...6}$ and a single piezoelectric resonator. The switches S_3 to S_6 can be replaced by diodes, analyze, the PR is

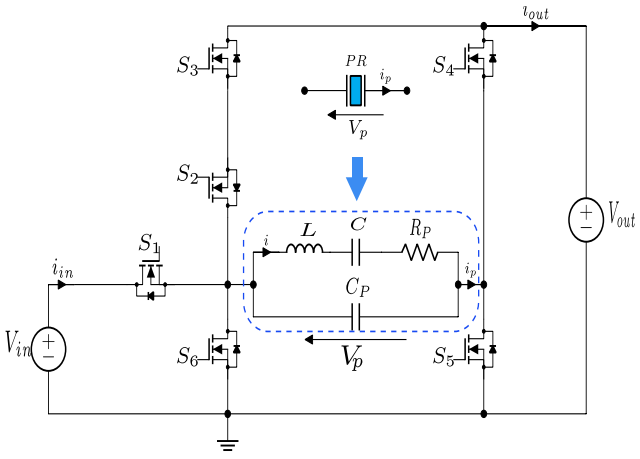


Fig. 1. The proposed topology.

TABLE I
EXAMPLE OF OPERATING MODES AND SWITCHING SEQUENCES

	Conditions	V_{in}	V_{in}-V_{out}	-V_{out}	*Zero*	V_{out}
Mode 1	$V_{in} < 2V_{out}$	$i>0$	-	$i>0$	$i<0$	-
Mode 2	$V_{in} > 2V_{out}$	-	$i>0$	$i>0$	-	$i<0$

modeled as an *L-C-R*$_P$ circuit that describes its mechanical behavior and an intrinsic capacitance C_P in parallel, as shown in Fig. 2. This topology makes it possible to establish several stages of connection of the PR with: V_{in}, V_{in} - V_{out}, -V_{out}, V_{out} and *Zero voltage* (short-circuit) in order to exchange energy between input source and output load or to modify the charge of the PR. In addition, isolated stages can be performed to let the voltage across the PR and switches evolve softly by charging/discharging the capacitance C_P for operating with Zero Voltage Switching (ZVS) conditions. Moreover, the circuit is designed for operation at a wide output voltage range and over a wide power range.

B. Operating modes

For a periodic conversion in steady-state operation, the energy and charge balance must be achieved. From this, the cycle should be composed of a minimum of six stages: three connected stages and three isolated stages. The connected stage is defined when the voltage across the PR is constant, while the isolated stage correspond to one of the ends of the PR is floating. So, the voltage across the PR can evolve by charging or discharging the capacitance C_P. During a cycle, we alternate between connected stages and isolated stages. Connected stages allow PR to exchange energy with input source and output load. Indeed, the PR stores electrical energy into mechanical energy when connected to the input source, and restitutes this energy as electrical form when it is connected to load. Isolated stages operate at constant charge (i.e., no charge is exchanged) in order to charge and discharge the capacitance C_P (depending on the sign of i in the *L-C-R*$_P$ branch). These operating stages enable evolving the voltages across the PR and the switches to achieve the next connected stage, and then turning on the switches with zero voltage switching (ZVS) conditions. Connecting PR to *Zero voltage* (short-circuit) allows to balance the electric charge over a full period [22], [25]. By taking into account the previous considerations, we can deduce for example two conversion cycles. The first one (mode 1) allows the PR to be connected successively with: V_{in}, $-V_{out}$, and *zero Voltage*, this first sequence of stages operates at any output voltage [25]. However, it contains a *zero voltage* stage that leads to increase losses because during this stage, no energy is exchanged with the input source and/or the output load [22], [25]. Consequently, the power losses increase and the maximum power conversion is then limited by heat. The second one (mode 2) enables connecting the PR as follow: $V_{in} - V_{out}$, $-V_{out}$ and V_{out}. This switching sequence allows ensuring multiple connected stages with the output load, maximizing the average current delivered to the load and the output power. However, this mode operates only as a step-down converter, with the gain

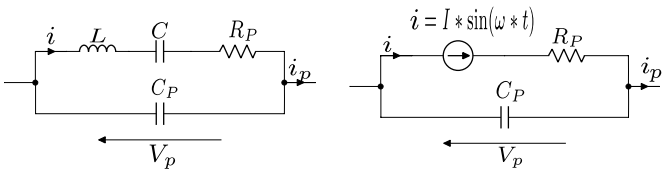


Fig. 2. Electrical model of PR: (a) Van Dyke Butterworth circuit [29], (b) Current source equivalent model.

ratio V_{out}/V_{in} not exceeding 0.5. Thus, in order to operate with high efficiency and a large variable output voltage, we can use mode 1 for $V_{out} > V_{in}/2$, and mode 2 for $V_{out} < V_{in}/2$. The operating modes and switching sequences are summarized in TABLE I. For this paper, we consider only the high-to-low voltage applications, using mode 2. This mode is suitable for:

- Step-down converters with low gain conversion $\frac{V_{out}}{V_{in}}$.
- Maximizing the energy transfer to the load by ensuring multiple connections with V_{out}.
- Minimum of the number of stages required for each conversion cycle: six stages.

C. *Example of operating switching sequences*

To implement the switching sequence $\{V_{in}\text{-}V_{out}, -V_{out}, V_{out}\}$, we have replaced the switches $S_{3,\ 4,\ 5\ and\ 6}$ by four diodes $D_{1,\ 2,\ 3\ and\ 4}$ (as see in Fig. 3), because of these switches operate as diodes. Fig. 4a-f show the six configurations depending on the sign of i matching with the switching sequence. The switches and diodes are considered lossless. The following analysis describes the operating cycle:

First stage [t_0, t_1]: During this stage, S_1 and D_4 are ON and V_P equals to V_{in}-V_{out}, as shown in Fig. 4a. The current i is positive. PR takes electrical energy from the differential input-output voltages, and stores it as a kinetic one. This stage ends by turning OFF S_1.

Second stage [t_1, t_2]: all switches are turned OFF. The PR is isolated (as seen in Fig. 4b) and V_P goes from V_{in}-V_{out} to -V_{out}, because during this stage i is positive, as shown in Fig. 5a. This stage ends by turning ON D_1 and D_4 when V_P equals to -V_{out}.

Third stage [t_2, t_3]: During this stage, the current flows through PR, D_1 and D_4, as shown in Fig. 4c. The PR transfers the first part of the stored energy to the output load in an electrical form. This stage ends when the current in D_1 and D_4 crosses to zero, leading to their OFF state.

Fourth stage [t_3, t_4]: All switches are OFF, as shown in Fig. 4d. The voltage V_P goes from -V_{out} to V_{out}. At the end of this stage, the switch S_2 is turned ON with soft switching condition.

Fifth stage [t_4, t_5]: The current load flows through PR, D_3, S_2 and D_2, as seen in Fig. 4e. The second part of the stored energy in PR is transferred to the output load. This stage ends by turning OFF S_2.

Sixth stage [t_5, t_6]: During this stage, all switches are OFF, as seen in Fig. 4f. V_P increases from V_{out} to V_{in}-V_{out}. This stage allows turning ON S_1 when V_P equals to V_{in}-V_{out} at the end of the period.

In the sixth stage, V_P should equal $V_{in} - V_{out,}$ by the end of this stage in order to turn on S_1 with ZVS. However, the voltage across D_3 is null (due to the parasitic capacitance of the D_3), because the current i is negative. Therefore, the source voltage of S_1 is not equal to V_{in}, but it is equal to $V_{in} - V_{out}$. Consequently, the Drain-Source voltage of S_1 is not null but equal to V_{out} that induces power losses. The Fig. 5a shows the all theoretical waveforms of PR's voltage and current for 1-6 stages without the ZVS of S_1. In this figure, the connected stages $\{V_{in} - V_{out}, -V_{out}$ and $V_{out}\}$ correspond to the first, third and fifth stage respectively.

To overcome that limitation and ensure the ZVS condition, we let V_P goes up to V_{in}, since the current is negative. Once, the current i becomes positive, D_3 is turned OFF while V_P decreases from V_{in} *to* $V_{in} - V_{out}$. However, the sixth isolated stage takes more time in this case (see Fig. 5a). Thus, by considering the ZVS condition of S_1, the sixth stage is then divided in two parts (6.a and 6.b) to separate the change of the sign of the current i into two distinguished parts, as illustrated in Fig. 4f-g. These two stages are described as follow:

Sixth-a stage [t_5, t_6]: During this stage, all switches are OFF, as shown in Fig. 4f. V_P increases from V_{out} to V_{in}. This stage allows turning ON S_1 when V_P equals to V_{in} at the end of the period.

Sixth-b stage [t_6, t_0]: S_1 is turned ON, but all other switches are turned OFF, as shown in Fig. 4g. Since the PR is isolated, V_P decreases from V_{in} to V_{in}-V_{out}. This stage ends by turning ON D_4. Fig. 5b shows the modified conversion cycle allowing to ensure the ZVS condition.

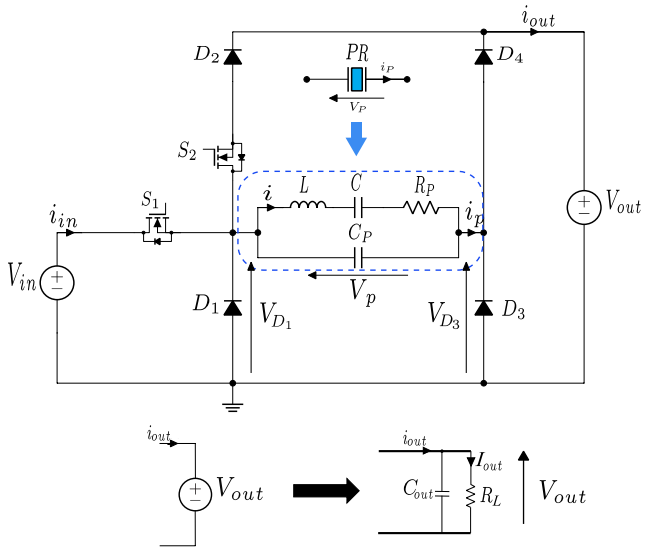


Fig. 3. The circuit topology for switching sequences V_{in}-V_{out}, -V_{out} and V_{out}.

III. STEADY STATE ANALYSIS: PRACTICAL CONSIDERATIONS

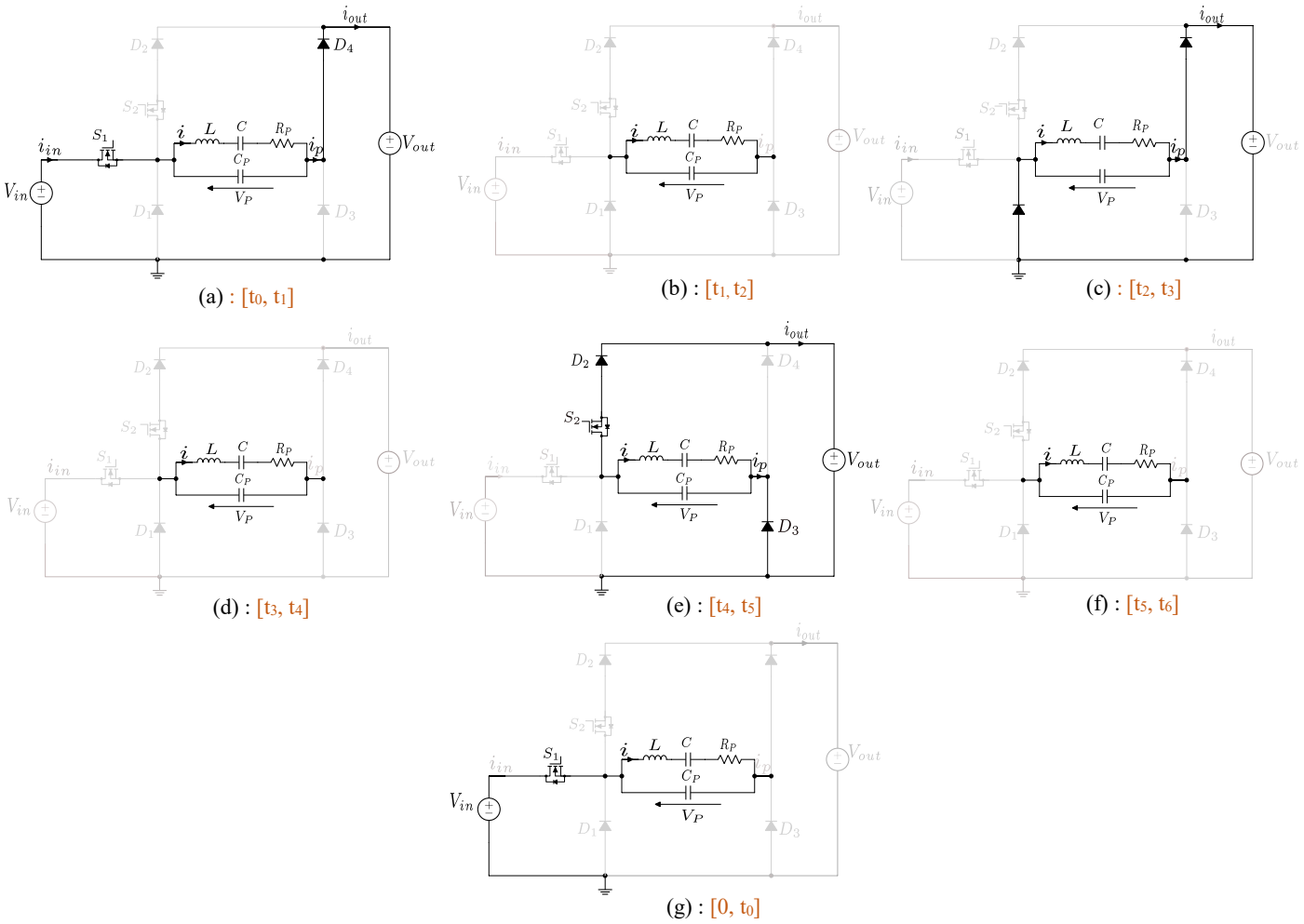


Fig. 5. Circuit configurations.

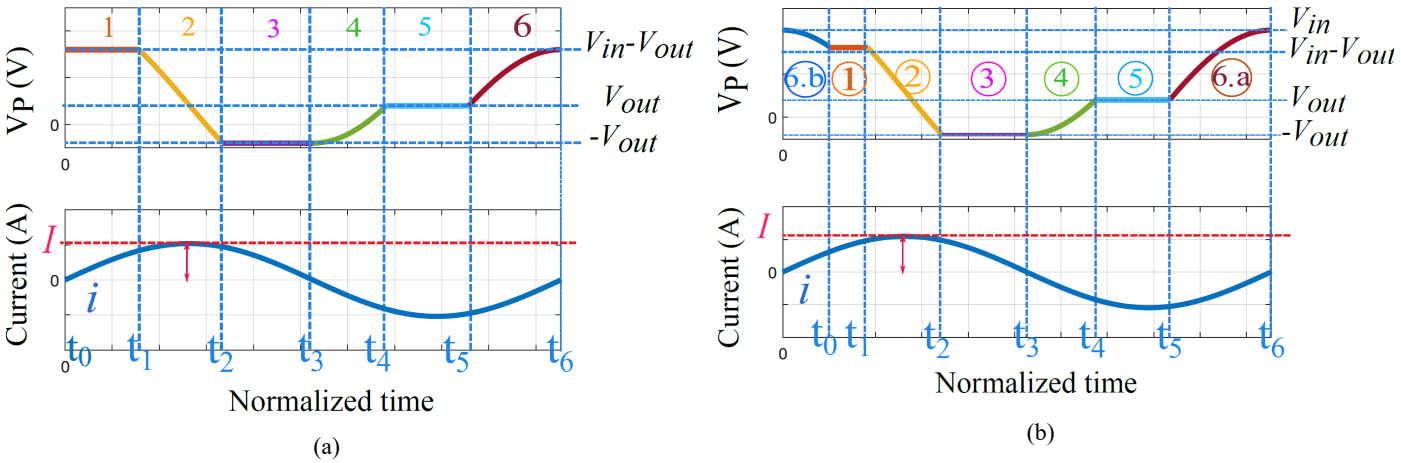


Fig. 4. Theoretical waveforms of PR's voltage and current *i:* (a) 1-6 stages, (b) 1-6b stages

In this part, some practical considerations for the analytic model are presented. The following analysis will be applied by taken the switching sequence presented in section II.C (without considering the parasitic capacitances of switches). The above considerations can be extended to any switching sequence.

A. PR model

In order to simplify the analytical model and estimate the current *i*, the *L* - *C* branch can be modeled by a current source, as illustrated in Fig. 2b. Indeed, the region between the resonant (*L*-*C*) and anti-resonant frequencies (*L*-(*C*//C_P)), is called inductive region. The internal current *i* is approximated by a sinusoidal current source thanks to the high quality factor of ceramic such as the case of the Lead Zirconate Titanate (PZT)

[30], [31]. In the inductive region, the operating frequency moves and depends on the transmitted power. Indeed, for a high power operation, the working frequency is approaching the resonant frequency, and for lower power, it is approaching the anti-resonant frequency. Moreover, in steady state operation, the stored energy in the PR, when connected to the input source, is the sum of the one delivered to the output load and PR's losses (while omitting losses of switches). As result, the energy balance induces sustainable oscillations that leads to a constant amplitude of the current *i*. By taking into account the previous assumptions, we approximate the current *i* by (1).

$$i(t) = I\sin(\omega t) \tag{1}$$

I: is the amplitude of the oscillation and ω is the radial frequency. Therefore, the power losses due to the damping effect throughout R_P can be estimated for a period of conversion T by using the equivalent circuit model shown in Fig. 2b and (1). Thus, the power losses P_{PR} is defined by:

$$P_{PR} = \frac{R_P}{T}\int_0^T i^2(t)\ dt = \frac{1}{2}R_P I^2 \tag{2}$$

B. Electric charge balance

For a period of conversion in steady state, the total charge of PR is conserved. As a result, the charge stored in the PR in stage 1 is then transferred to the output during stage 3 and 5. Equation (3) gives the charge balance.

$$Q_1 + Q_3 + Q_5 = 0 \tag{3}$$

Where Q_1 is the stored charge in stage 1 and taken in positive value, since the current *i* is positive. Q_3 is the positive charge restored during stage 3, and Q_5 is the negative charge restored during stage 5 as long as the current *i* is negative. By using (1), one can estimate the charge for each stage by:

$$Q_1 = \int_{t_0}^{t_1} i(t)\ dt = \frac{I}{\omega}(\cos\omega t_0 - \cos\omega t_1) \tag{4}$$

$$Q_3 = \int_{t_2}^{t_3} i(t)\ dt = \frac{I}{\omega}(\cos\omega t_2 - \cos\omega t_3) \tag{5}$$

$$Q_5 = \int_{t_4}^{t_5} i(t)\ dt = \frac{I}{\omega}(\cos\omega t_4 - \cos\omega t_5) \tag{6}$$

C. Energy balance

In steady state, the electrical energy stored during stage 1 is transferred during the third stage when V_P equals to $-V_{out}$ and during the fifth stage when PR is connected to V_{out}, with a part dissipated in the PR. Therefore, the energy balance is defined by (7):

$$E_{in} = E_{out} + E_{loss}(PR) \tag{7}$$

Where E_{in} is the electrical energy stored during stage 1 and taken as positive value, E_{out} is the electrical energy transferred to the output load and taken as a positive value. By including (2) in (7), the energy balance equation becomes:

$$(V_{in} - V_{out})Q_1 - V_{out}Q_3 + V_{out}Q_5 - \frac{1}{2}R_P I^2 T = 0 \tag{8}$$

D. Soft switching conditions

In order to perform the soft switching, the Drain-Source voltage of S_1 and S_2 should equals to zero when turning on these switches. The condition of turning on S_1 is given by (9), and for turning on S_2, V_P should reach V_{out} at $t = t_4$.

$$V_P\ (t_6) = V_{in} \tag{9}$$

$$V_P\ (t_4) = V_{out} \tag{10}$$

E. Load model

To solve the previous equations, we have modeled the load by a capacitance C_{out} in parallel with a resistor R_L that is determined by the desired output power P_{out} and the output voltage V_{out}. C_{out} is chosen sufficiently large that the output voltage is considered constant with no voltage ripple, as shown in Fig. 3. The output power is then given by:

$$P_{out} = \frac{V_{out}^2}{R_L} = V_{out}I_{out} \tag{11}$$

Where I_{out} is the mean value of the current flowing through R_L that depends on the current *i*, *{t_0, t_1, t_2; t_3; t_4 and t_5}* and the resonant period, as the transferred energy to the output load operates during stage 1, stage 3 and stage 5. Equation (2) gives the mean current value calculation.

$$I_{out} = \frac{1}{T}\int_0^T i(t)\ dt = \frac{1}{T}\left(\int_{t_0}^{t_1} i(t)dt + \int_{t_2}^{t_3} i(t)dt - \int_{t_4}^{t_5} i(t)dt\right) \tag{12}$$

IV. Steady State: Analytical models

The analytical model is presented and solved in this section, by taking as example, the previous conversion cycle that considers the zero voltage switching (1-6b stages). An energy diagram V_P *(Q)* is also presented to describe the conversion cycle. The efficiency of the proposed topology is also estimated.

A. Model with losses

In this section, we present the analytical model that estimates each time duration *{t_0, t_1… t_6}* for a period of conversion in steady state. Moreover, power losses due to the damping effect are considered. To obtain the analytical model, we take as an example the switching sequence shown in Fig. 5b, which operates with ZVS conditions. Yet, the following analysis can be adapted for 1-6 stages by putting $t_0 = 0$ in the previous equations (see Fig. 5a). As shown in Fig. 5b, during the connected stages, voltage V_P is constant and known, however, during isolated stages *{2, 4, 6a, 6b}*, V_P evolves by charging or discharging C_P. Indeed, if the current *i* is positive,

the capacitance C_P is then discharged and V_P decreases, and if i is negative, the capacitance C_P is charged and V_P increases. Therefore, the relationship between V_P and i during isolated stages $[t_k, t_{k+1}]$ is expressed by (13):

$$V_P\,(t_{k+1}) = -\frac{1}{C_P}\int_{t_k}^{t_{k+1}} i\,(t)\,dt + V_P(t_k) \tag{13}$$

By inserting (1) in (13), we obtain:

$$V_P\,(t_{k+1}) = \frac{I}{C_P\omega}(\cos\omega t_{k+1} - \cos\omega t_k) + V_P(t_k) \tag{14}$$

By considering the continuity of V_P, the energy and charge balance, we determine each time duration $\{t_0, t_1 \ldots t_6\}$ by (15)-(21):

$$t_0 = \frac{1}{\omega}\cos^{-1}\left(1 - \frac{V_{out}}{I}C_P\omega\right) \tag{15}$$

$$t_1 = \frac{1}{\omega}\cos^{-1}\left(1 - 4\frac{V_{out}}{V_{in}} + \frac{V_{out}}{I}C_P\omega + 2\frac{V_{out}^2}{V_{in}I}C_P\omega - \frac{1}{2} * \frac{R_P*\omega*T}{V_{in}} * I\right) \tag{16}$$

$$t_2 = \frac{1}{\omega}\cos^{-1}\left(1 - 4\frac{V_{out}}{V_{in}} - \frac{V_{in}-V_{out}}{I}C_P\omega + 2\frac{V_{out}^2}{V_{in}I}C_P\omega - \frac{1}{2} * \frac{R_P\omega T}{V_{in}} I\right) \tag{17}$$

$$t_3 = \frac{T}{2} \tag{18}$$

$$t_4 = t_4 = \frac{1}{\omega}\cos^{-1}\left(2\frac{V_{out}}{I}C_P\omega - 1\right) \tag{19}$$

$$t_5 = \frac{1}{\omega}\cos^{-1}\left(1 - \frac{V_{in}-V_{out}}{I}C_P\omega\right) \tag{20}$$

$$t_6 = T \tag{21}$$

By substituting the equations (15)-(21) and (11) into (12), we estimate the amplitude I by:

$$-\frac{1}{2}R_P I^2 - \frac{2V_{out}}{\pi}I + \frac{V_{out}^2}{R_L} + \frac{V_{out}(V_{in}+V_{out})C_P\omega}{\pi} = 0 \tag{22}$$

Therefore, to estimate the current I, we solve (22), which includes the damping effect. This equation is solved analytically. Equation (23) shows a simplified expression by considering R_P=0 (no losses in the PR).

$$I = \frac{\pi}{2}I_{out} + \frac{(V_{in}+V_{out})}{2}C_p\omega \tag{23}$$

Once I is known, we can compute the time duration of each stage. In this conversion cycle, the total charge transfer that is named K in [25] is equal to 1, which represents a high factor of utilization according to the approach of [25].

B. *Computing the analytical model*

The power losses due to the PR are taken into account in the following computing of the analytical model. The modeling is applied on the conversion cycle 1-6b stages shown in Fig. 5a, at the operating conditions V_{in} = 200 V, V_{out} = 40 V and P_{out} = 10 W, and solved for operating frequency of 95 kHz. The electrical parameters of PR are given in TABLE II. The time-duration of each stage is calculated by using equations (15)-(21). Fig. 6 shows the waveforms for the conversion cycle in the time-domain. The waveforms show the PR's voltage V_P, the current i, the input current i_{in} and i_{out} that corresponds to i during the first and third stage, and -i during the fifth stage.

Fig. 7 represents the voltage V_P as a function of the PR's charge evolution over a single conversion cycle. In the diagram V_P *vs.* Q, the horizontal curves correspond to the connections to the DC source or load, imposed by the switches and diodes, while the vertical curves correspond to the evolution of the voltage V_P required by the transitions between these voltage levels. That occurs when the switches and diodes are OFF. Moreover, for a displacement in the positive direction, the transferred charge is considered as positive (Ex: $Q_1 = q_1 - q_0 =$

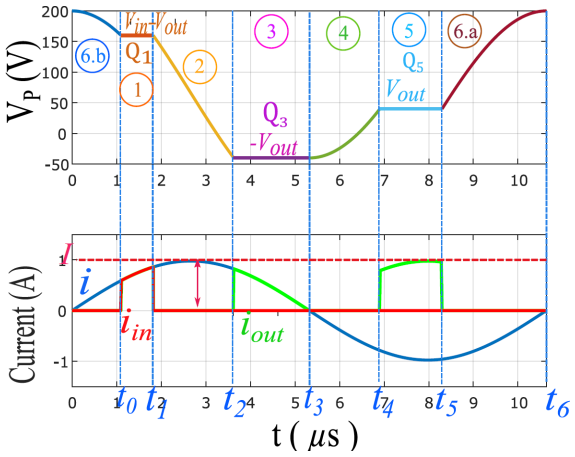


Fig. 6. Waveform of PR's voltage and currents with 1-6b stages, by solving the analytical model for: V_{in} = 200 *V*, V_{out} = 40 *V and* P_{out} = 10 *W*.

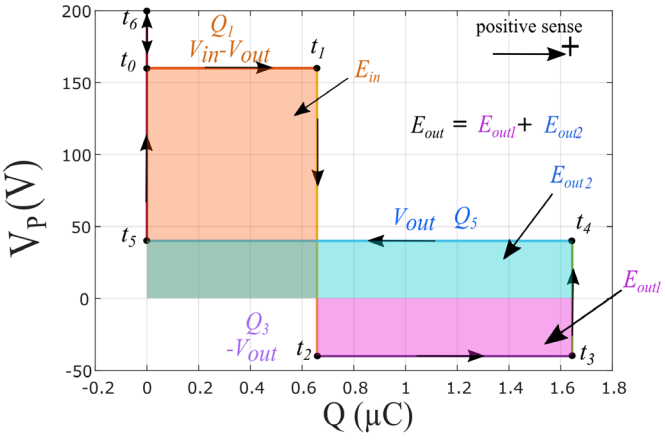


Fig. 7. Voltage Vs Charge Q of PR with 1-6b stages: V_{in} = 200V, V_{out} = 40 V and P_{out} = 10W.

TABLE II
CHARACTERISTICS OF THE ELECTRICAL MODEL OF PR IN RADIAL MODE VIBRATION. (PART NO: Z0.75T25D-W (C-213). MATERIAL IS PZT, THE SUPPLIER IS FUJI-Ceramics.

	D (mm)	Th (mm)	L (mH)	C (nF)	R_P (Ω)	C_P (nF)	f_r (kHz)	Q	k_p
Value	25	0.75	1.1	2.9	0.6	8.4	89	1000	52%

0.656−0 = 0.656 μC), and for displacement in the negative direction, the transferred charge is taken as negative value (Ex: $Q_5 = q_5 - q_4 = 0 - 1.646 = -1.646\ \mu C$). Therefore, the area under the curve represents the electrical energy exchanged (Ex: $E_{in} = (V_{in} - V_{out})\ Q_1$). The diagram V_P *vs* Q gives a better representation of the energy and charge transfer. The representation of V_P *vs* Q enables constructing any switching sequences by alternating horizontal and vertical lines while ensuring the closed diagram and energy balance. This representation illustrates the transfer of energy and charge.

C. *Efficiency estimation*

The efficiency of the converter is given by (24). . This equation takes only into account only the power losses in the PR that is approximated by (2). Fig. 8 shows the efficiency for 1-6b stages as a function of the output power and for different gain levels $G = V_{out}/V_{in}$ at input voltage of $V_{in} = 200$ V. As shown in Fig. 8, the efficiency is higher than 96% for a wide range of operating points. For a low power (less than 4 W), a significant part of I is used to charge and discharge C_P giving an advantage for high gain ratio which reduces the voltage excursion of V_P. In counterpart, at a higher power level (>7W), regarding (23), the amplitude I becomes proportional to I_{out} and then, at same current level and then at same losses, a greater output voltage induces a greater output power and then a greater efficiency.

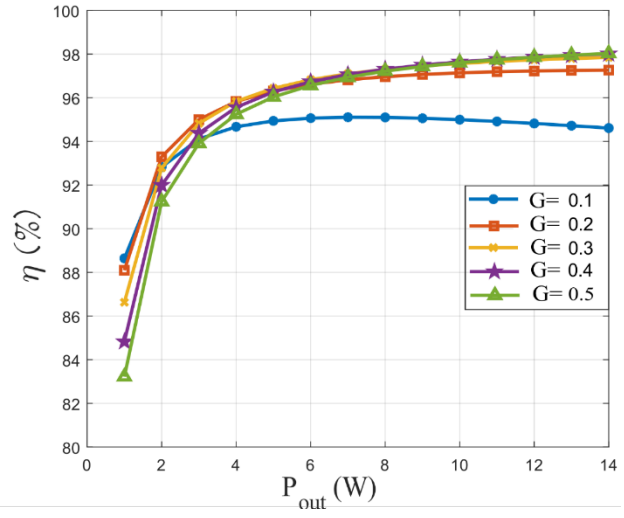


Fig. 8. Efficiency vs Output Power obtained by solving the analytical model for 1-6b stages for a fixed input voltage $V_{in} = 200$ V and various gain levels $G = 0.1$ to 0.5.

These plots give an overview of the maximum efficiency reached as a function of the power and the conversion gain. It can be used to compare the conversion cycles as function of gain and power.

$$\eta = \frac{1}{1 + \frac{\frac{1}{2}R_P I^2}{P_{out}}} \tag{24}$$

V. SIMULATIONS RESULTS

To validate the operating principle and the performances, we performed a simulation under LTSpice was performed. In this simulation, the PR is modeled as in Fig 3 and its electrical parameters are shown in TABLE II. GS66508B GAN FET SPICE model was chosen for S_1 and S_2 to operate at high frequency and for a wide range of applications (up to 650 V), fast diode US1G was taken for (D_1, D_2), and VSSB310 for (D_3, D_4). Then, we have implemented the switching times, relative to the operating period, calculated from the analytical model. The switches are controlled at the same frequency of the mechanical oscillation (*i.e. the operating frequency is located in the inductive region of the PR*). The synchronization on the mechanical movement is done thanks to the detection of a sign change on the current *i*. Fig. 9 shows the simulated waveforms of PR's voltage V_P and the instantaneous current of i, i_{in} and i_{out} in steady state for $V_{in} = 200$ V, $V_{out} = 40$V, $P_{out} = 10$W and f= 95kHz. As shown, the simulated current i is almost sinusoidal, which validates the approximation made in section III.A. The amplitude I obtained by simulation is equal to 1.05 A while we have obtained 0.998A by using (23). Thus, the analytical model exhibits a good accuracy for the estimation of the current I ($\Delta I < 5\,\%$), [22]-[25]. Fig. 10 shows the efficiency as a function of the output power for a voltage ratio G= 0.1 to 0.5. A high efficiency is observed in simulation up to 95 % for G =

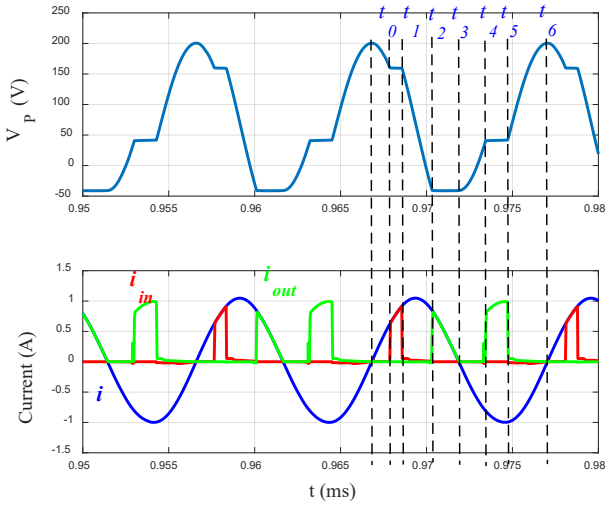


Fig. 9. Simulated waveforms in time-domain: $V_{in} = 200$ V, $V_{out} = 40$ V and $P_{out} = 10$ W.

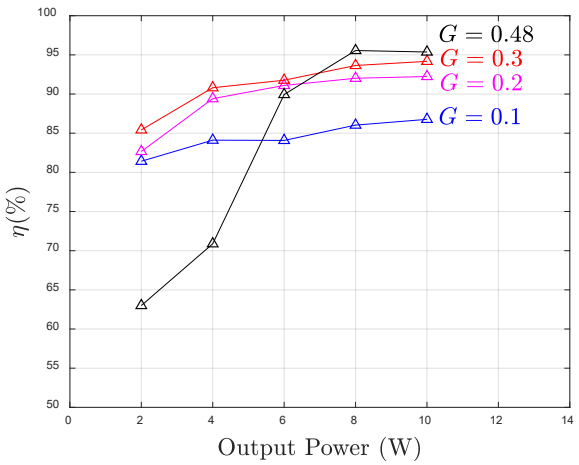


Fig. 10. Efficiency vs. Output Power obtained in simulation for input voltage V_{in} = 200 V and G = 0.1, 0.2, 0.3 and 0.48.

0.48 and P_{out} = 10W. For a fixed output power, the efficiency is higher for high output voltage since the amplitude of I decreases which induces lower power losses in the PR: $P_{PR} = \frac{1}{2} R_P I^2$.

VI. Experimental Results

In this section, we assess the operating principle described above. The experimental waveforms under various conditions (V_{in}, V_{out} and P_{out}) are shown to illustrate the operating principle and to demonstrate the performances of the converter in terms of efficiency and power.

A. The proposed setup

Fig. 11 shows the prototype used to validate the operating principle. The PR is selected in order to have a high quality factor (> 1000) and a high coupling factor (> 50 %) to minimize the losses [30], [31]. For this prototype, we have firstly chosen the radial mode vibration for operating at low frequency. The resonant frequency f_r in this mode is determined by the diameter of PR and the frequency constant N_P (m.Hz) of the material (*i.e.*, N_P= 2230 m.Hz for C-213 from Fuji Ceramics). Therefore, equation (25) gives the relation between the resonant frequency and the diameter. The thickness should be as small as possible, but it needs to ensure the insulation (assumed 1 kV/mm C-213) and to sustain the mechanical constraints. By taking into account these parameters, the material PZT C 213 from Fuji was chosen with a diameter of 25 mm obtaining a resonant frequency around 90 kHz and a thickness of 0.75 mm, because this material offers a high quality factor and high coupling factor [30], [31]. Fig. 12a shows the full impedance spectrum measured by an analyzer under small signal excitation spectrum measured by an analyzer under small signal excitation (1 V is applied by the impedance analyzer). The radial mode was measured near 89 kHz and the thickness mode at 2.75MHz. In addition, various vibration modes can be observed. From the obtained impedance spectrum, we measure f_r, f_{ar}, C_P and R_p (R_p *is* measured at the

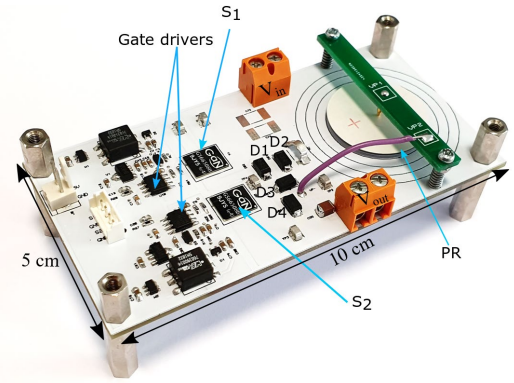


Fig. 11. Picture of prototype circuit.

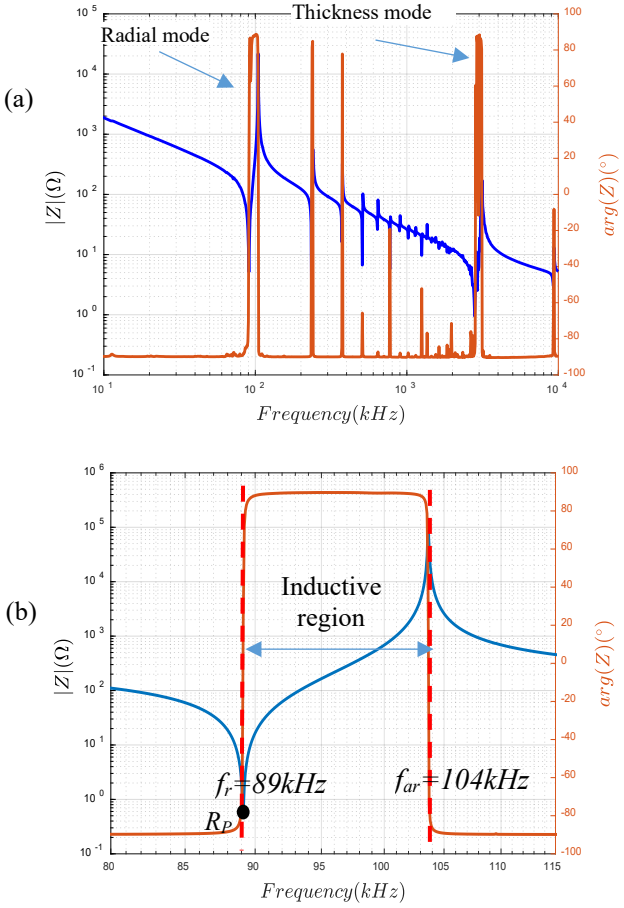


Fig. 12. Plot of PR's impedance spectrum for D = 25mm and *th* = 0.75mm: (a) full spectrum (b) radial mode.

resonant frequency f_r), then, we use (26)-(29) to calculate *L, C, Q* and k_p (k_p *is the coupling factor for radial mode vibration of a PR disc shape*) [32]. The electrical parameters are summarized in TABLE II. To reduce the contact resistance due to soldering and to prevent the PR from damage due to heat during soldering, we have fixed the PR at its center by a surface-mount contact (with a thickness of 0.15 mm) in the bottom and a spring contact at top. The prototype circuit is built on a 100 x

TABLE III
PART COMPONENTS

Component	Reference	Constraint conditions
S_1 and S_2	GS66508B GAN FET R_{dson}= 50mΩ	V_{in}
D_1, D_2	US1G,V_f=1 V@ 1Adc	V_{in}
D_3 and D_4	US1G,V_f=1 V@ 1Adc	V_{out}
Isolated Gate driver	SI8172	V_{GS} = +6 V \ -3 V

50 mm PCB with two layers of 35-µm copper. The part components used to build the prototype are listed in TABLE III with theirs electrical constraints.

$$N_P = \frac{f_r}{D} \tag{25}$$

$$C = k_p^2 C_P \tag{26}$$

$$L = \frac{1}{(2\pi f)^2 C} \tag{27}$$

$$Q = \frac{2\pi f_r L}{R_P} \tag{28}$$

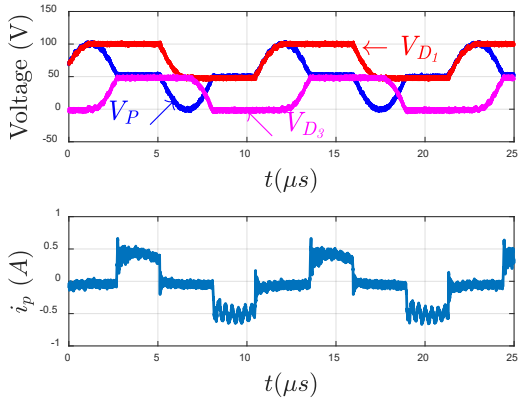
$$k_p = \sqrt{\frac{(f_{ar}^2 - f_r^2)}{f_{ar}^2}} \tag{29}$$

The experimental results are obtained in open-loop operation, while the timing are pre-calculated by using the analytical model presented in section IV, and solved at the frequency of 95 kHz for a given V_{in}, V_{out} and P_{out}. Then, the driving controls of S1 and S2 are provided by a waveform generator. The timing and frequency are then tuned to ensure ZVS and load conditions by using the observed waveform of V_P. Nevertheless, we have implemented the optimal law control of the presented dc-dc converter based on PR in [26], that includes the synchronization with internal current *i*, load regulation and ZVS regulation.

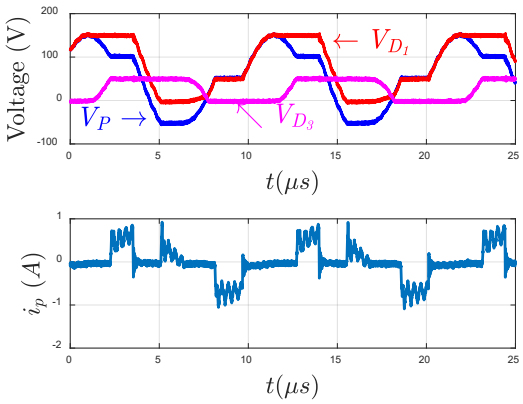
B. Experimental waveforms

The waveforms are experimentally validated throughout Fig. 13 and Fig. 14 at various operating points. Fig. 13 presents the main waveforms of the PR's voltage and the current for a fixed output voltage and power for a typical application as V_{out}= 48 V and P_{out} = 10 W over a different input voltages V_{in} = 100 V, 150 and 200 V. These waveforms demonstrate the operating principle based on alternating between isolated stages (charging/discharging C_P) and the connected stages (energy transfer). Therefore, the current i_P of the PR (only during connected stages) is shown. From its waveforms, we can deduce the instantaneous current i_{in} and i_{out}, where $i_{in} = i_P$ during stage 1, and i_{out} is the sum of i_P during stage 1, stage 3 and -i_P during the stage 5. Fig. 13 illustrates how the waveforms evolve over a various gain ratios *G*. For a $G = 0.48$, stage 3 ($V_P = -V_{out}$) is not necessary as the energy stored during stage 1 ($V_P = V_{in} - V_{out} = V_{out}$) is completely transferred during stage 5 ($V_P = V_{out}$). By increasing the gain ratio *G*, the time-duration of isolated stages increases while the time-duration of connected stages decreases, since the PR's voltage needs to go from V_{in} to $-V_{out}$ before going back to V_{in} which increases while $V_{in}+V_{out}$ increases. By adjusting t_2 while keeping the other switches in the ZVS operation mode and synchronized on the

(a): V_{in}=100 V, V_{out}=48 V, P_{out} =10 W, f=92.17 kHz, η=95.5%.



(b) : V_{in}=150 V, V_{out}=48 V, P_{out} =10 W , f=96.74 kHz, η=92.6%.



(c) : V_{in}=200 V, V_{out}=48 V, P_{out} =10 W , f=97.89 kHz, η=91.8%.

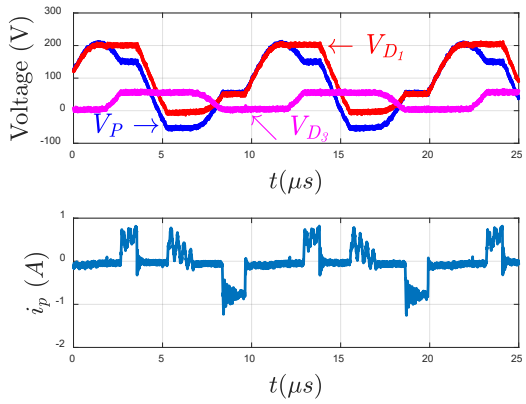


Fig. 13. Experimental waveforms in time-domain for V_{out} = 48 V, P_{out} = 10 W and input voltage: (a) V_{in} = 100 V, (b) V_{in} = 150 V, (c) V_{in} = 200 V.

mechanical oscillation, one can change the energy balance and then makes I increases or decreases to adjust the output current and then to regulate the output voltage. Yet, we have demonstrated and experimentally validated the control strategy of this converter in [26]. At the same output power, the efficiency decreases while reducing the output voltage, because the current amplitude *I* and the losses (2) increases while $I_{out}=P_{out}/V_{out}$ increases, see (23). Also, the efficiency decreases

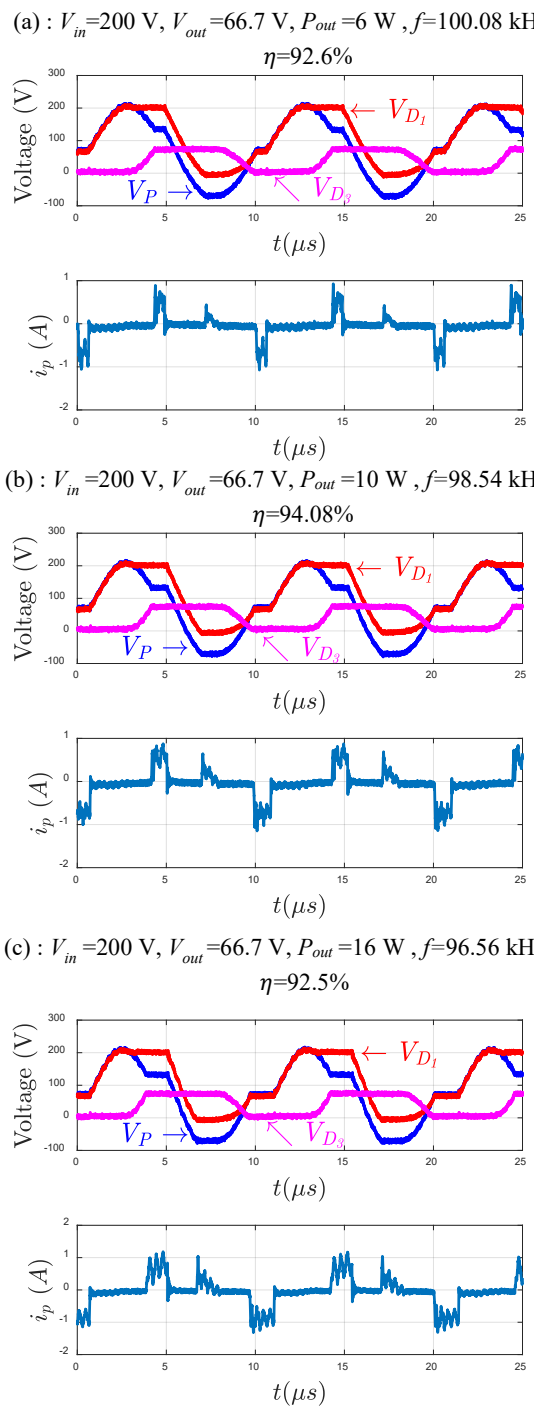


Fig. 17. Experimental waveforms in time-domain for V_{in} = 200 V, V_{out} = 66.7V and output power: (a) P_{out} =6 W, (b) P_{out} =10 W, (c) P_{out} =16 W.

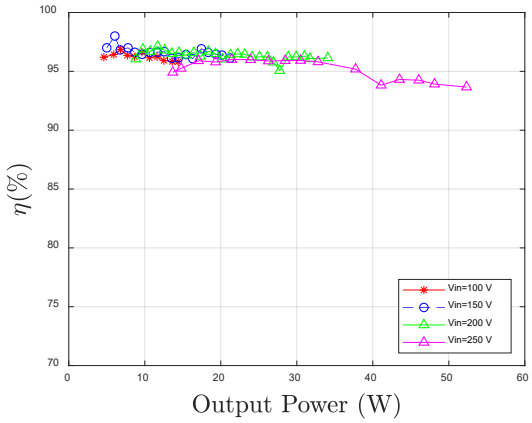


Fig. 16. Efficiency vs output power for gain G = 0.48 and for different input voltages.

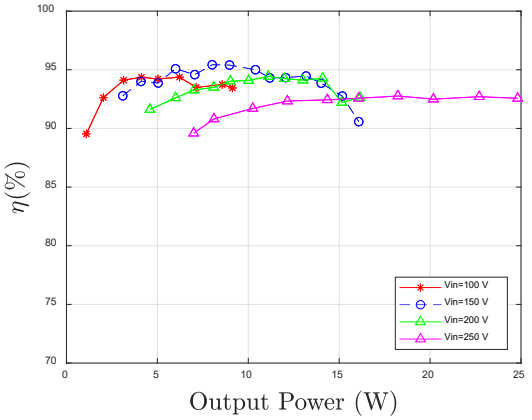


Fig. 15. Efficiency vs output power for gain G = 0.33 and for different input voltages.

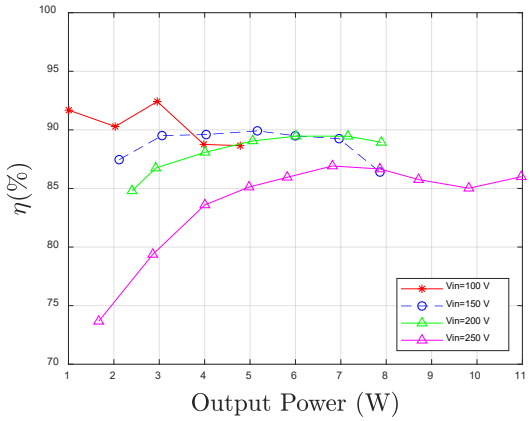


Fig. 14. Efficiency vs output power for gain G = 0.167 and for different input voltages.

while increasing the input voltage, because it increases V_{in}+V_{out} and then the current amplitude I, see eq. (23), and also the losses, see (2).Definitely, at the same power level, decreasing the output/input voltage ratio G decreases the efficiency. Some waveforms exhibit ripples at a frequency 2.78 MHz, which are more visible on the current i_P. These ripples come from harmonics due to exciting spurious modes (corresponding to the thickness mode). This phenomenon can be explained by comparing the Fourier decomposition of the voltage V_P with the piezoelectric impedance [22].

In Fig. 14, we have fixed the input voltage and output voltage (G = 1/3), and then we have increased the power from 6 W to 16 W to show how the waveforms evolve. We note that the time-duration of the connected stages increased by increasing the power while the time-duration of isolated stages decreased. Therefore, for low load, the operating frequency is

approaching the anti-resonance frequency (parallel resonance: L - (C // C_P)), and by increasing the power (i.e.: increasing the duration of connected stages) the operating frequency is approaching the series resonance $L - C$ (resonant frequency). Nevertheless, the efficiency remains higher than 92 % over a wide range of powers, [see Fig. 14(a) to Fig. 14(c)].

B. Efficiency

In this section, we have experimentally measured the efficiency (P_{out}/P_{in}) with using the power analyzer HMC 8015 at the input source and the output load for various operating points while taking into account the power losses of the PR and semiconductors (the drive power is not taking into account for the measured efficiency). Fig. 15 , Fig. 16 and Fig. 17 show the efficiency as a function of the output power for 3-values of gain ratio: G = 0.48, 0.33 and 0.167 respectively. The maximum output power corresponds to the limit of the maximum allowed temperature in the PR before its performances drop, which corresponds to a maximum of the current amplitude I~1 A. The measurements are done after ensuring thermal stability (after few minutes). For G= 0.48 in Fig. 15, the efficiency is higher than 95 % over a wide range of operating points. However, for some operating points, the efficiency decreases due to harmonics due to spurious excited modes (thickness modes). To avoid these thickness mode interferences leading to the degradation of the efficiency, we should select the thickness of the PR as small as possible (while ensuring the electrical insulation) compared to its diameter leading to increase the gap between the resonant frequency in radial mode and in thickness mode. As shown throughout Fig. 15 to Fig. 17, the efficiency decreases with the gain at the same output power. Fig. 18 shows a thermal picture of the prototype working at 25 W and with a current amplitude I of 1 A. The picture illustrates the losses distribution that are mainly on the PR and diodes. In addition, the heat spot is at the center of the PR as all the current flows at its center.

To sum up, the losses are mainly linked to the current amplitude I: it induces losses in the piezoelectric material (expressed by $R_P I^2/2$) but it also induces similar losses in the switches $R_{on} I^2_{eff}$ during the conduction part. In both cases, it is better, at same power level, to reduce the current amplitude I. Therefore, the current amplitude I expression given (23) can be subdivided as follow:

$$I = \frac{(V_{in}+V_{out})C_P\omega}{2} + \frac{\pi}{2} I_{out} = I_{circulating} + I_{useful} \qquad (30)$$

Where $I_{circulating}$ is the current level required before any power transfer; it is the current part necessary to charge and discharge the capacitance C_P to reach the extreme voltages, and it leads losses without any output power. This part increases with V_{in}, V_{out} and the frequency. I_{useful} is the current level required to reach the output power. At a low output current I_{out}, $I_{circulating}$ is dominant while becomes negligible at a high output current (i.e.: when I_{useful} becomes dominant). Based on this current representation, we compare our new topology with some others presented in [22] and [25] (step-down converters). In the topology [22], considering the case of (V_{in}, 0, V_{out}) sequence, the current expression is given by:

$$I = \frac{V_{in}C_P\omega}{2} + \pi I_{out} = I_{circulating} + I_{useful} \qquad (31)$$

In this case, the amplitude of the current $I_{circulating}$ is lower compared to our topology since $I_{circulating}$ is proportional to V_{in} instead of V_{in}+V_{out}, but the I_{useful} is twice higher compared to our topology limiting the efficiency and the maximal output power. In this paper, as we focus on high-to-low voltage conversion, V_{out} is quite small compared to V_{in} making V_{in}+V_{out} so close to V_{in}. For the topology shown in [25] and by considering the case of (V_{in}-V_{out}, 0, V_{out}) sequence and G < 0.5, the current expression is given by:

$$I = \frac{V_{in}C_p\omega}{2} + \pi I_{out} * \left(1 - \frac{V_{out}}{V_{in}}\right) = I_{circulating} + I_{useful} \qquad (32)$$

Where the current $I_{circulating}$ is proportional to V_{in}, which is lower compared to our topology where our current $I_{circulating}$ is proportional to V_{in}+V_{out}. In return, I_{useful} is always higher compared to our topology for a gain ratio of G < 0.5. [25] is more adapted for high gain ratio (0.5<G<1), where the current I_{useful} becomes lower than in our topology. In TABLE IV, we have compared 3 Step-down DC-DC converters based on a piezoelectric resonator for a gain of 0.1 and I_{out} = 500mA (omitting the thermal limitation and the physical properties) with considering the electric model of the PR shown in TABLE II. As detailed above, our topology offers the lowest I and power losses in the PR at the same output power and voltage

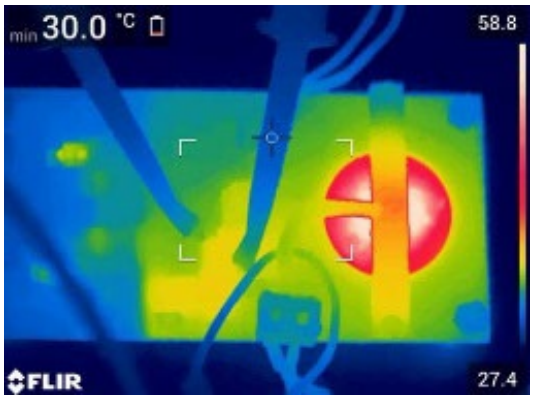


Fig. 18. Thermal image of prototype at V_{in}= 250 V, G=*1/3*, P_{out}= 25 W and I=1 A, $\Delta T = 28\,°C$.

TABLE IV
COMPARATIVE BETWEEN 3-STEP-DOWN DC-DC CONVERTERS
V_{in} =200 V, V_{out} = 20 V, f = 95 kHz and P_{out} =10 W

	Our topology	[24] : V_{in}- V_{in}, 0, V_{out}	[20]:V_{in}, 0, V_{out}
I	1.33 A	1.91 A	2 A
P_{loss} (PR)	0.53 W	1.1 W	1.3 W

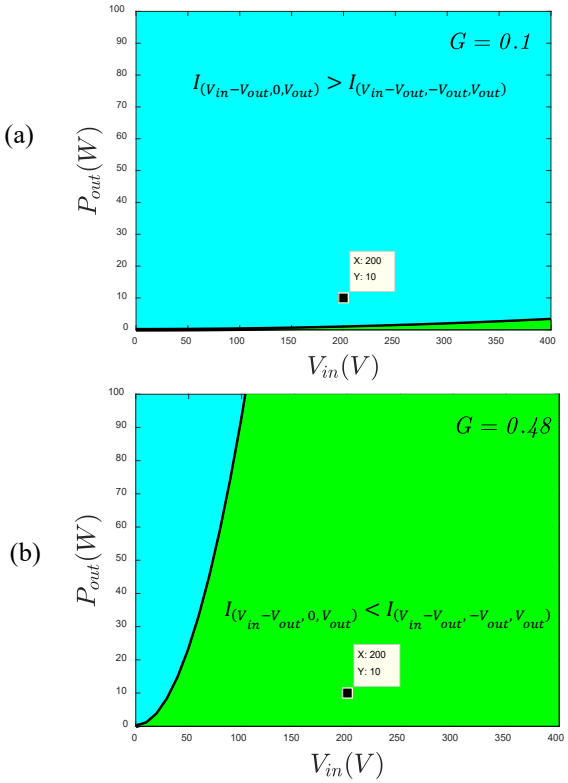


Fig. 19. Comparison between switching sequences: $I(V_{in}\text{-}V_{out}, 0, V_{out})$ is the lowest in the green zone and $I(V_{in}\text{-}V_{out}, -V_{out}, V_{out})$ is the lowest in cyan color for: (a) G=0.1 and (b) G=0.48.

conditions. For high-to-low voltage applications, we need to select a topology that ensures multiple connections with the output voltage to maximize the extracted energy from the PR and reducing its power losses (i.e., *high utilization factor* [25]). This comparison allows designing the PR and semiconductors by considering current and loss constrains. A deepening comparison between the various conversion cycles can be done by comparing the current amplitude I in same desired conditions: P_{out}, V_{in} and G. For instance, we have compared our topology with [24]. Equation (33) gives in which case our topology is offering higher performances (lower I at the same conditions).

$$I_{(V_{in}-V_{out},0,V_{out})} - I_{(V_{in}-V_{out},-V_{out},V_{out})} = \frac{(1-G)P_{out}}{GV_{in}} - GV_{in}\frac{C_P\omega}{2} \geq 0 \quad (33)$$

Therefore, equation (34) gives a criterion where our topology gives a lower current I compared to [24] as function of P_{out}, V_{in} and G. In Fig. 19, we have plotted P_{out} as a function of V_{in} for a gain G=0.1 and 0.48 by using (34). In the green zone, [24] offers lower losses while in cyan it induces upper losses. Our conversion cycle is well suited for a wide range of operating conditions and particularly for low voltage ratio G. [see Fig. 19].

$$P_{out} \geq V_{in}^2 \frac{G}{\pi\left(\frac{1}{2G}-1\right)}\frac{C_P\omega}{2} \quad (34)$$

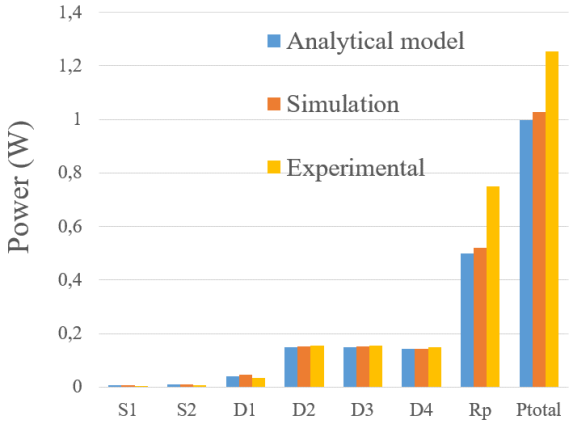


Fig. 20. Loss distribution comparison for: V_{in}= 250 V, G=1/3, P = 25 W.

TABLE V
KEY PARAMETERS FOR 3-PRS IN THICKNESS MODE VIBRATION.

	D (mm)	Th (mm)	L (μH)	C (nF)	C_P (nF)	R_P (Ω)	f_r (MHz)	Q	k_t (%)
PR1	12	2	133	0.17	0.775	4	1.04	200	42.7
PR2	25	2	34	0.735	3.3	0.39	1.049	500	43
PR3	40	2	11.7	2.01	8.44	0.5	1.038	300	45

C. *Loss distribution*

Fig. 20 illustrates the loss distribution for each components for V_{in}= 250 V, G=1/3 and P_{out}= 25 W. In this figure, a comparison between the analytical model estimation (using the timing and amplitude of I obtained by solving the model for f=95 kHz and PR's model shown in TABLE II) with simulation (SPICE calculation) and experimental results is presented. The losses of the switches are determined by $R_{dson}I_{eff}^2$ during the conduction stage, and the loss of diodes are calculated by using $V_f I_{cond}$ also during their conduction stage. As shown in Fig. 20, the estimated loss by using the analytical model exhibited a good accuracy compared to the loss obtained in simulation and experimental results for the switches and diodes. However, the PR losses obtained experimentally are higher compared to the ones obtained in simulation and the analytical model. Indeed, the supplementary are due to exciting spurious mode that induce losses, as demonstrated in [21]. Therefore, to improve the analytical model (or the simulation) in order to fit the experimental results, the PR's equivalent model can include the full impedance, where each spurious mode can be represented by LCR series circuit in parallel with the capacitance C_P. However, the analytical model becomes more complex.

D. *Output power vs Frequency*

As stated, the conversion cycle operates with a variable frequency that is between the resonant and anti-resonant frequency. For low power, the operating frequency is near the anti-resonant frequency where the amplitude I is only required for charging/discharging the capacity C_P. For high power, the

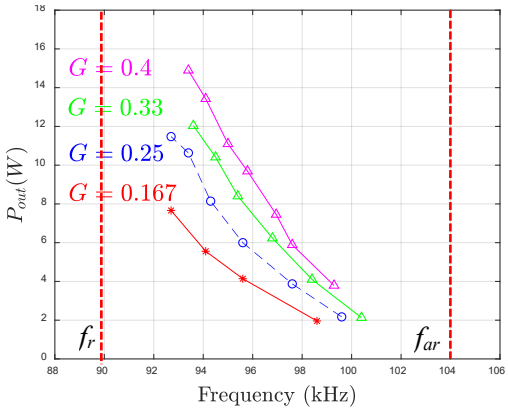


Fig. 22. Output Power vs Frequency, for V_{in}= 150 V and G=0.4, 0.33, 0.25 and 0.167.

operating frequency decreases to approach the resonant frequency. A small part of I crosses C_p, approaching the short-circuit resonance (i.e., series frequency). Fig. 21 illustrates how the frequency evolves as a function of the output power over different gain levels. As shown, the operating frequency decreases by increasing the power. Thus, for closed-loop operation, the operating frequency of PR should be measured, and the control of the switches must be synchronized with i like in [22]-[26].

E. Thickness mode operation

In this part, we have investigated the thickness mode operation at a high resonant frequency in order to increase the power density. To do so, we have selected an operating frequency around 1 MHz. Therefore, the thickness (th) of the PR is determined by (35), which depends on the selected operating frequency (1 MHz in this case) and the frequency constant of the thickness mode named N_t (N_t = 2090 m.Hz for C-213). TABLE V shows the equivalent electrical model of three PRs with a diameter of 12, 25 and 40 mm that operate at the resonant frequency of 1 MHz in the thickness mode. The electrical models are obtained experimentally by using an impedance analyzer.

In addition, the experimental measurements are done with the same electrical contacts as presented in Fig. 11. As it is shown

$$N_t = \frac{fr}{th} \tag{35}$$

in TABLE V, the effective quality factor (measured) is lower than 500 over three the PRs instead of the value given by the supplier Fuji, Q = 2500. This decrease of the quality factor is due to the contact resistance, which needs to be improved in the future. In addition, the thickness mode vibration is highly disturbed by the spurious radial modes. To reduce the impact of spurious modes, we can increase the ratio Diameter/Thickness that allows increasing the distance between the thickness and the radial mode in the frequency domain. So, the ratio Diameter/Thickness can be taking into account in the design of the PR's geometry.

(a) : V_{in}=200 V, V_{out}=60 V, P_{out} =30 W , η=78%.

(b) : V_{in} =200 V, V_{out} = 60 V, P_{out} = 100 W , η = 83.5%.

(c) : V_{in} =200 V, V_{out} = 60 V, P_{out} = 138 W, η = 84 %.

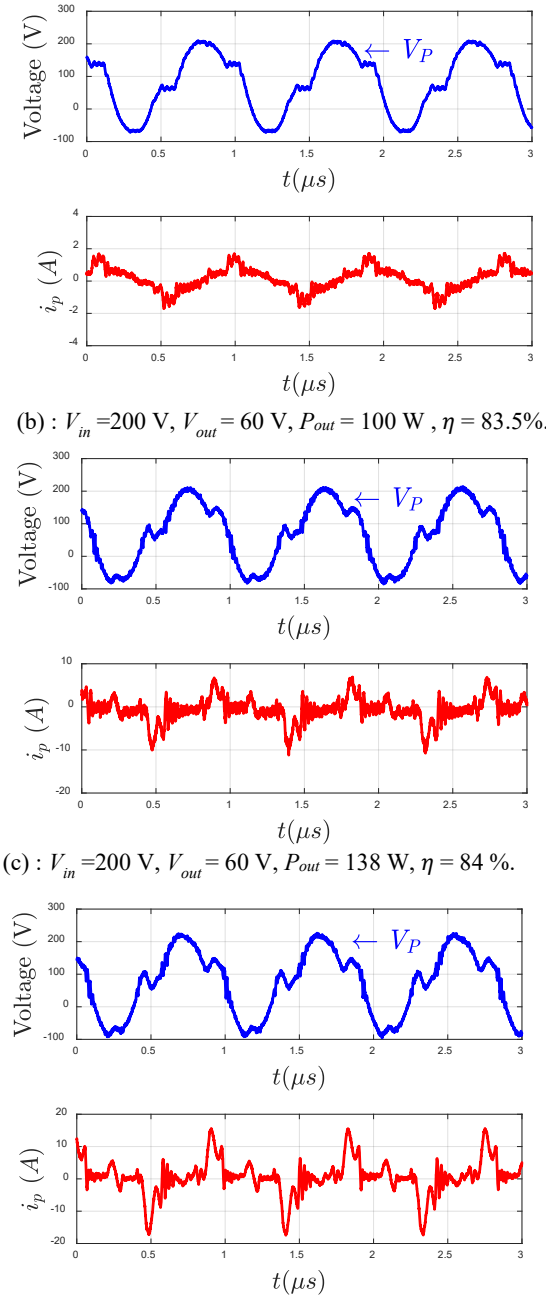


Fig. 21. Experimental waveforms for V_{in} = 200 V_{out} = 60 V and f = 1.086 MHz for: (a) PR1, (b) PR2, (c) PR3.

Fig. 22 exhibits the waveforms of the PR's voltage and current for the three PRs at the same operating frequency f=1.086 MHz, and for an input voltage of 200 V and a G=0.3. The waveforms are corresponding to the desired waveforms shown in Fig. 6. As shown in Fig. 22, the output power is scaled-up by increasing the area at the same operating conditions (voltages and frequency). However, due to the poor quality factor (*i.e. high power losses*), the scaling up of the output power is limited by temperature. Indeed, for an output power exceeding 100 W, the temperature measured for the PR2 and the PR3 reaches 100°C. In addition, high frequency

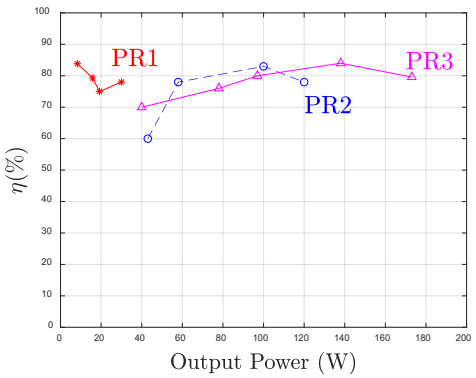


Fig. 23. Efficiency vs Output power in thickness mode vibration for: V_{in} = 200 V_{out} = 60 V.

oscillations (20 MHz) due to exciting spurious mode can be observed in the current i_P leading to additional power losses.

In Fig. 23, we have plotted the efficiency as a function of the output power for an input-output voltage of 200 - 60 V and for the three PRs. A high efficiency of 84% is obtained for PR3 at 138 W (while omitting the thermal stability, as the PZT has a curie temperature of 320°C and the supplier recommends not exceeding one third of curie temperature of the material otherwise PR may depolarize in an irreversibly way). The efficiencies measured over the power range and for all the PRs are lower than the expected, since the quality factors are drastically dropped (Q < 500) compared to the values given by the supplier (Q = 2500). Also, the electrical contacts provide a supplementary losses as all the current exchanged with the PR flows through a single point. Nevertheless, we have obtained a maximum output power of 175 W with an efficiency of 80% for the 40 mm diameter disk, which is corresponding to a power density of 69.6 W/cm^3 (by considering only the volume of the PR). The highest power density is obtained for the lower area (PR1) that corresponds to a power density of 176.8 W/cm^3. Thus, Piezo-based DC-DC converters can be suitable for high power density applications [30], [31].

VII. CONCLUSION

A new electrical energy transfer mechanism based on a piezoelectric resonator is investigated in this paper. A new topology of a DC-DC power converter is proposed and assessed successfully. The operating principle composed of six stages ensures the energy and the electric charge balance, which enables to obtain high efficiency and high power densities thanks to the high quality factor and the high coupling coefficient of the piezoelectric material such as the PZT. The soft switching operation allows reducing the power losses due to switching. This paper also presents a simplified method to determine the duration of each stage. Moreover, we have demonstrated experimentally the feasibility of a power converter based on the PR achieving a high efficiency over a wide range of operating points. A high efficiency of 93.8 % is reached for a high output power of 50 W with input-output voltage respectively of 250 − 117 V. In addition, the thickness mode operation @ 1MHz was experimentally validated and shown high output power over 100 W. Indeed, an output power of 100 W was achieved for an input-output of 200-60 V and for a volume of the PR not exceeding 1 cm^3. However, there remain many possibilities and opportunities still to be explored in order to increase the efficiency and the power density, such as the frequency rising by reducing the size of the PR, parallelization of piezoelectric resonators, synchronous rectification or exploring other piezoelectric materials [27]. It can be concluded that the DC - DC power converters based on the PR holds great promises for improvements in terms of miniaturization and integration with high efficiency and high power densities for high-to-low voltage and low-to-medium power applications.

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