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Graphical Abstract

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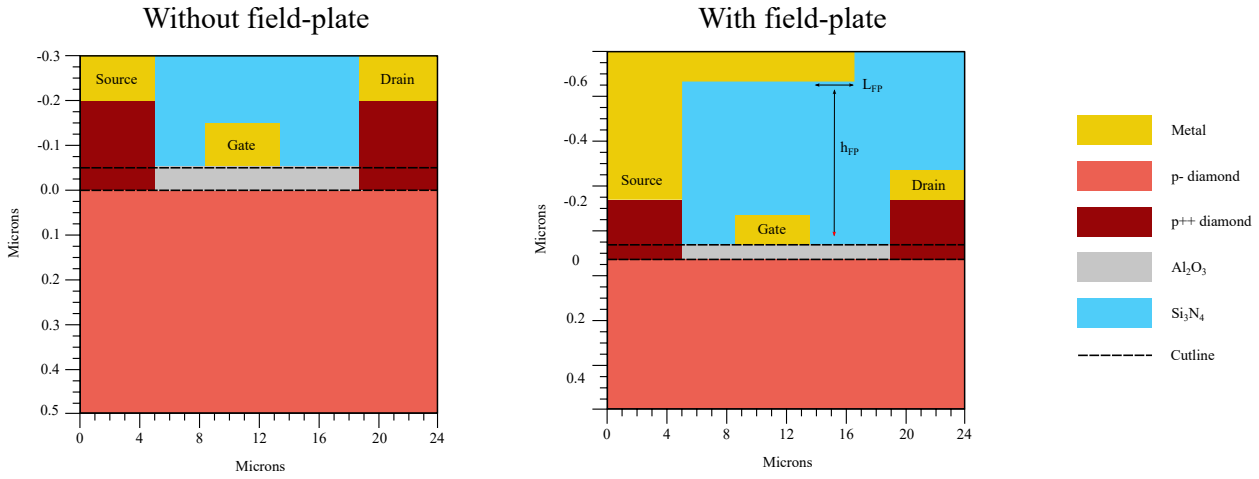
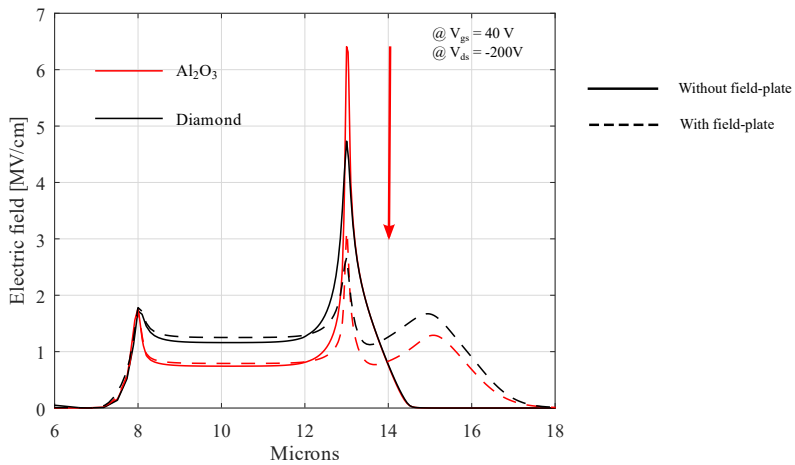




Highlights

Field-Plated D3MOSFET design for breakdown voltage improvement

Marine Couret, Damien Michez, Juliette Letellier, Anne Castelan, Julien Pernot, Nicolas Rouger

- A source field-plate D3MOSFET is designed to reach a targeted 1 kV of breakdown voltage.
- The device exhibits a 75 mΩ.cm^2 specific on-state resistance and a breakdown voltage larger than 600 V in simulations.
- Experimental studies on the passivation layer made of Si_3N_4 reaches a critical electric field between 8 MV/cm to 11 MV/cm.

Field-Plated D3MOSFET design for breakdown voltage improvement

Marine Couret[a], Damien Michez[a,b], Juliette Letellier[b], Anne Castelan[a,c], Julien Pernot[d], Nicolas Rouger[a]

[a] *Université de Toulouse, LAPLACE, CNRS, UPS, INPT, F-31071 Toulouse, France*
[b] *DIAMFAB, F-38042 Grenoble, France*
[c] *Institut Catholique d'Arts et Métiers, ICAM, F-31000 Toulouse, France*
[d] *Université Grenoble-Alpes, CNRS, Institut Néel, F-38042 Grenoble, France*

Abstract

As commonly reported in other power devices, the lateral deep-depletion diamond MOSFET (D3MOSFET) suffers from an electric crowding effect at the gate-edge towards the drain. This behavior leads to a premature breakdown of the gate-oxide (made of Al_2O_3) below the expected performances of diamond material. The current article focuses on the design of a field-plated D3MOSFET in order to improve the device breakdown voltage up to 1kV. Based on 2D TCAD simulations, the field-plate geometrical features are optimized to reach the targeted specification, with an expected breakdown voltage larger than 600 V. The improved architecture requires the addition of a passivation layer made of Si_3N_4 that must reach a critical electric field around 10 MV/cm. Therefore, a characterization campaign of this passivation layer is performed based on MIM capacitors. Measurements on a 400 nm thick Si_3N_4 layer show promising results with a critical electric field between 8 MV/cm and 11 MV/cm.

Keywords: Diamond, D3MOSFET, Power device, Breakdown voltage, Field plate, Fabrication process

1. Introduction

Thanks to its ultrawide bandgap of 5.5 eV and related high critical electrical field above 7 MV/cm, together with a high free hole mobility of more than 2000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, diamond offers theoretically the best performances for unipolar power devices [1]. Moreover, the high thermal conductivity of 22 W/(m.K) for diamond material makes it an excellent asset for power applications to reduce the size of the thermal packaging [2]. For those multiple reasons, the interest within diamond-based transistors has grown over the past years with the development of several architectures for diamond devices as summarized in [2, 3]. As such, field effect transistors (FET) have been demonstrated, including inversion MOSFET [4], deep depletion MOSFET [5, 6] or Metal Semiconductor FET [7]. A survey of the different architecture performances is presented in figure 1 showing the specific on-state resistance according to the breakdown voltage. While lateral diamond transistors such as MESFETs or MOSFET with NO_2 doping have shown breakdown voltages above or larger than 2kV [8, 9, 7, 10, 11, 12], diamond MOSFETs using the deep depletion regime have only shown a breakdown voltage around 200 V [5, 6]. However, it was reported for this architecture, the highest peak electric field in off-state (above 5 MV/cm), with stable and efficient transistor characteristics above 250°C [6]. The premature breakdown has been attributed to an electric field crowding effect at the gate-edge, as typically reported on lateral power devices, inducing an electrical breakdown of the Al_2O_3 gate-oxide layer around 200 V [1]. This outcome, also observed in Ga_2O_3 power devices, can be overcome with the employment of field-plate as demonstrated in [13, 14, 15]. For the field-plate design, it is necessary

to introduce a passivation layer commonly made of SiO_2, Al_2O_3 or Si_3N_4. As the dielectric material must sustain very high electric fields, its critical electric field must be as high as possible. Therefore, the main objective of this article is to present a field-plate design adapted to a lateral deep-depletion-diamond MOSFET architecture with a requested breakdown voltage of 1 kV. Based on 2D TCAD numerical simulations, the device architecture will be presented together with its figures of merit. Then, a focus on the field-plate will be made with a design methodology for its geometrical parameters. The impact of the field-plate on the device performances will be assessed regarding both the breakdown voltage and the dynamic properties. Concerning the device fabrication process, a particular interest will be dedicated to the passivation layer development and the characterization of its critical electric field. Finally, the article will be concluded.

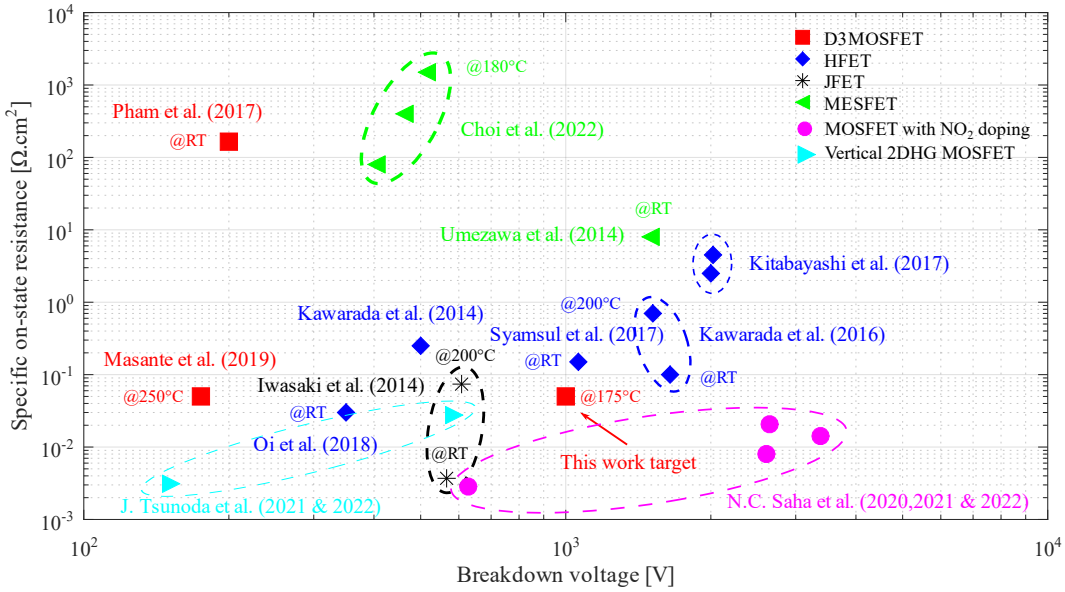


Figure 1: Specific on-state resistance vs. breakdown voltage performances of power diamond FETs reported in the literature. Experimental points are taken from [5, 6, 7, 8, 9, 10, 11, 12, 16, 17, 18, 19, 20, 21]

2. D3MOSFET design

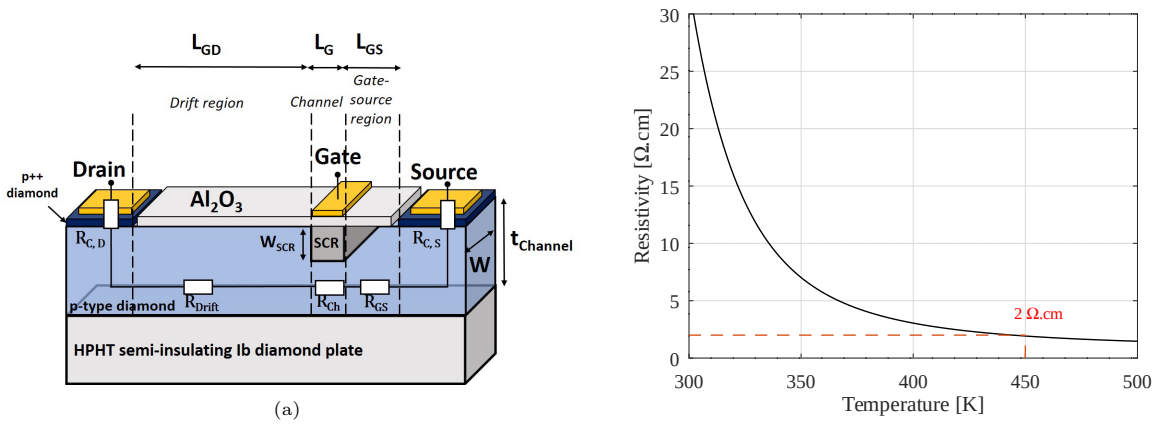
2.1. Description

The presented device is a lateral deep-depletion-diamond MOSFET which is directly based on the architecture proposed in [1] as displayed in figure 2a. The principle of the D3MOSFET is a lateral conduction between the drain and the source ohmic contacts made through a p- bulk diamond layer (boron doped) grown on a Ib diamond semi-insulating substrate. Using the 1D ionization integral [22] with the coefficients from [23] for diamond material, the doping for the channel, N_a, is decreased down to $8{\cdot}10^{16}$ atom.cm^{-3} considering a 1D breakdown voltage of 1400 V in non-punch through (NPT) condition implying a drift length, L_{gd}, larger than 3.35 µm. This decreased doping density will thereby reduce the constraints on the breakdown voltage. From this doping density value, it is rather simple to calculate the corresponding resistivity of the channel layer using equation (1). The models for the free holes density [24, 25], and the hole mobility [26] are dependent of the temperature, the boron-doping density and the compensation level

in donor atoms. Note that, in this study, the compensation level, N_d/N_a, is set to 4 %. From figure 2b, it can be observed a large reduction of the resistivity with increasing temperatures, demonstrating the benefits of using diamond devices at elevated junction temperatures. At 450 K, the targeted temperature for the device operation, the resistivity reaches a value of 2 Ω.cm.

$$\rho(T, N_a, N_d) = \frac{1}{q \cdot \mu_p(T, N_a, N_d) \cdot p(T, N_a, N_d)} \tag{1}$$

where μ_p is the hole mobility and p is the free holes density.



(a) (b)

Figure 2: (a) Schematic cross-section of a deep-depletion diamond MOSFET (D3MOSFET) and (b) Resistivity according to the temperature for a D3MOSFET with a boron-doped channel at $N_a = 8 \cdot 10^{16}$ atom.cm^{-3} and a compensation level in donor atoms of $N_d/N_a = 4$ %.

Moreover, in order to keep an equivalent threshold voltage of 30 V compared to the device reported in [1], the thickness of the channel, $t_{channel}$, is increased up to 500 nm. This value does not take into account the depletion caused by the PN junction from the substrate but only the depletion induced by the gate bias, meaning that the thickness of the channel will be larger than 500 nm. Regarding the sizing of the D3MOSFET, the gate-drain length is fixed to 6 µm as the device must (i) sustain the 1D breakdown voltage of 1.4 kV, which implies a drift length larger than 3.35 µm and (ii) account for the future field-plate architecture which requires an increase of the gate-drain distance. Finally, the gate length, L_g, and the gate-source length, L_{gs}, are respectively fixed to 5 µm and 3 µm due to process limitations and technology constraints. The resulting device presents a specific on-state resistance, $R_{on,s}$, calculated from equation (2), of 75 mΩ.cm² at 450 K. This value can be further optimized, while reducing safety fabrication margins (lower L_g and L_{gs}) but it is out of scope of this contribution. Nonetheless, as presented in figure 1, this would be a strong improvement for these lateral diamond MOSFETs.

$$R_{on,s}(T) = \rho(T)\frac{(L_{gs} + L_g + L_{gd})^2}{t_{channel}} \tag{2}$$

2.2. Simulation results

Using the 2D numerical simulations from Silvaco ATLAS, the working principle of the D3MOSFET is verified. Figure 3a presents the device transconductance for a V_{gs} ranging from -10 V to 60 V at low electric

field (V_{ds} = -1 V). This large scale allows us to observe all the device working regimes: the accumulation regime for V_{gs} < -5 V, the device on-state for V_{gs} up to 30 V and the device off-state for V_{gs} beyond 30 V. One can also note that the device is normally-on as a negative current around 1.2 mA/mm is flowing between the source and the drain at a V_{gs} of 0 V. For the three operation modes, the hole concentration and the current flowlines are also displayed in figures 3b for the accumulation regime, 3c for the device on-state and 3d for the device off-state. As the bulk mobility is considered during the simulations, an accumulation of holes underneath the gate is observed during the accumulation mode at V_{gs} = -10 V, which leads to current flowlines confined into a very thin layer. The device depletion mode is shown at a V_{gs} of 10 V with a partial depletion of the channel layer during the device on-state. The channel is fully-depleted for V_{gs} larger than the threshold voltage of 30 V and no current can flow from the source to the drain.

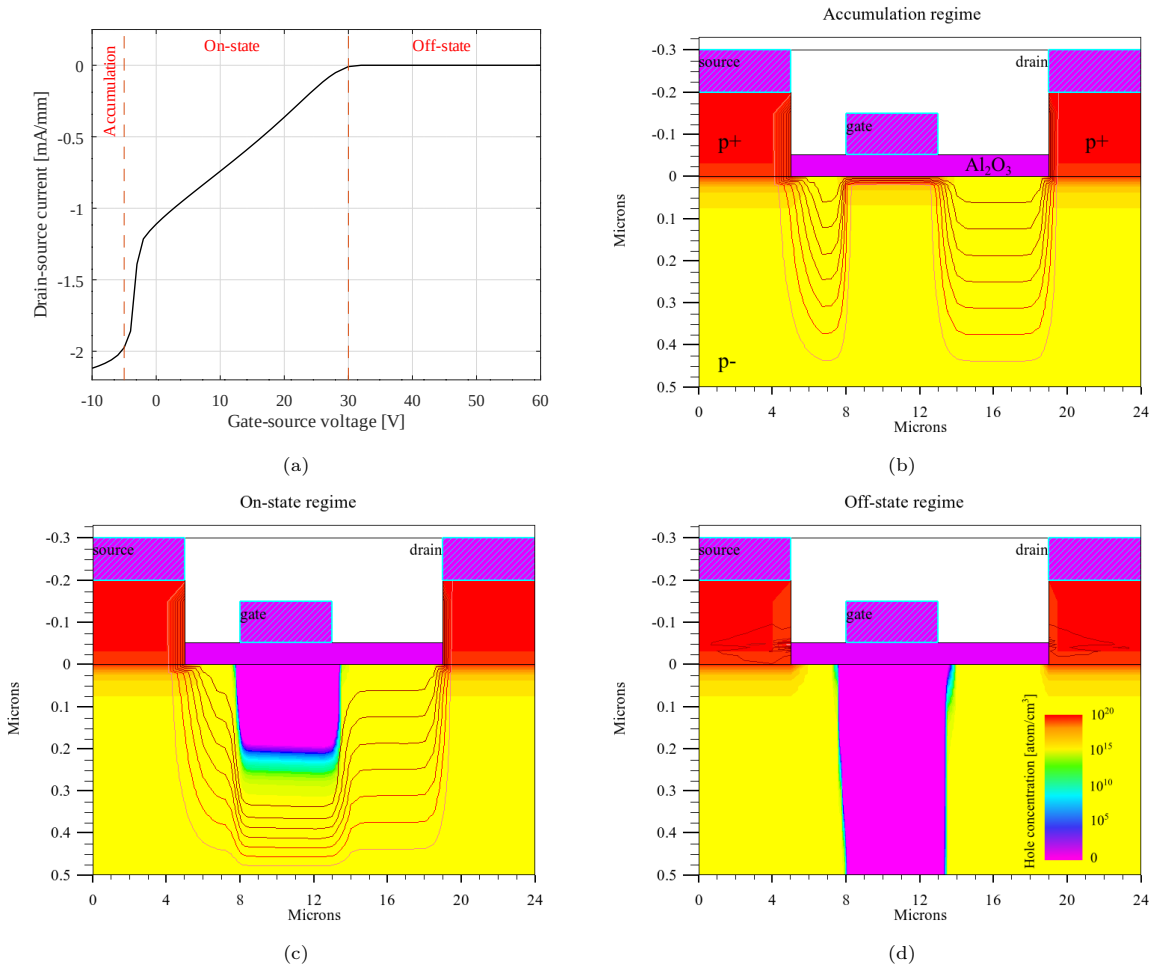
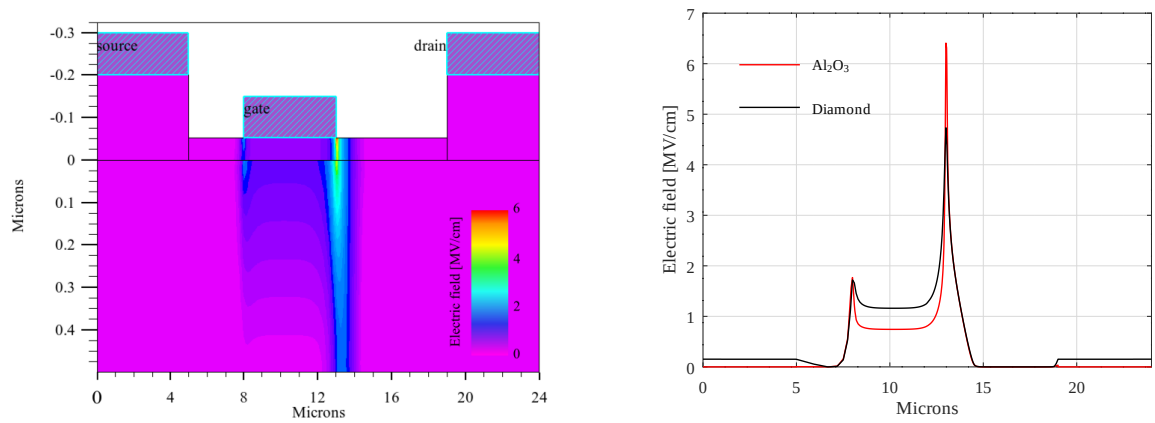


Figure 3: (a) Drain current vs. Gate voltage at T = 450K. Hole concentration and current flowlines in (b) the accumulation mode at V_{gs} = -10 V, (c) in the on-state mode at V_{gs} = 10 V and (d) in the off-state mode at V_{gs} = 40 V.

2.3. Limits associated with the elementary lateral D3MOSFET

Concerning the device breakdown voltage, figure 4a presents the 2D cartography of the device electric field for V_{gs} = 40 V and V_{ds} = -200 V, in off-state. As a reminder, the theoretical 1D breakdwon voltage

with a similar vertical device in NPT is 1.4 kV. From this graph, we observe an electric field crowding effect under the gate, at the drain-side, in both diamond and gate-oxide layers. The corresponding electric field along a lateral cutline is reported in figure 4b where a maximum value of 6.6 MV/cm, respectively 5 MV/cm, is observed in the gate-oxide, resp. in the diamond, layer. It is important to note that the value of the peak is largely dependent of the mesh grid used during the simulations. Here, the mesh spacing in the vicinity of the gate-edge at the drain side is fixed at 50 nm. Therefore, the reported values for the peak electric field in both diamond and oxide layers are only an estimation, mainly as a trade-off between accuracy, convergence and simulation time, and the values could be larger than the one reported using a thinner mesh spacing. However, in any cases, the peak electric field in the gate-oxide leads to a premature breakdown of the device as the theoretical critical electric field of the 50 nm thick Al_2O_3 is estimated around 6.8 MV/cm [1]. Thus, while the active layer of the device can normally reach much higher critical electric fields (between 7.7 MV/cm and 10 MV/cm for diamond material [2]), the transistor is limited here by the gate-oxide layer and will not be able to reach the 1D breakdown voltage of 1.4 kV.



(a) (b)

Figure 4: (a) Finite element simulation of the electric field distribution in the off-state with a drain bias of -200 V and a gate bias of 40 V. (b) The lateral electric field profiles on the oxide surface (red) and the top surface of the diamond (black) are extracted from the simulation.

3. Field-plated D3MOSFET design

3.1. Description

One common solution used to improve the breakdown voltage of power devices is the design of a field-plate such as in Ga_2O_3 [13, 14, 15] or GaN [27, 28] based devices. The purpose of this architecture is to smooth the electric field over a greater distance and thus reduce the electric field peak at the gate edge. A typical architecture is displayed in figure 5 which is called the source field-plate. This topology requires the addition of a passivation layer underneath the field-plate and of a thick metal layer to realize the field-plate. Regarding the state-of-the-art of dielectric material, the silicon nitride, Si_3N_4, presents the best figure-of-merit with a $\epsilon_R \cdot F_{BR}$ product of 75 MV/cm [29]. Moreover, power devices have already demonstrated high breakdown voltages using Si_3N_4 as a dielectric material [15, 30]. In order to improve as much as possible the

device voltage capability, two parameters, displayed in figure 5, need to be optimized: the thickness of the passivation layer, h_{FP}, and the extension of the field-plate at the drain side, L_{FP}. Although the geometry in an actual device would be different, the simplified structure of figure 5 has been considered as a good trade-off between accuracy and complexity.

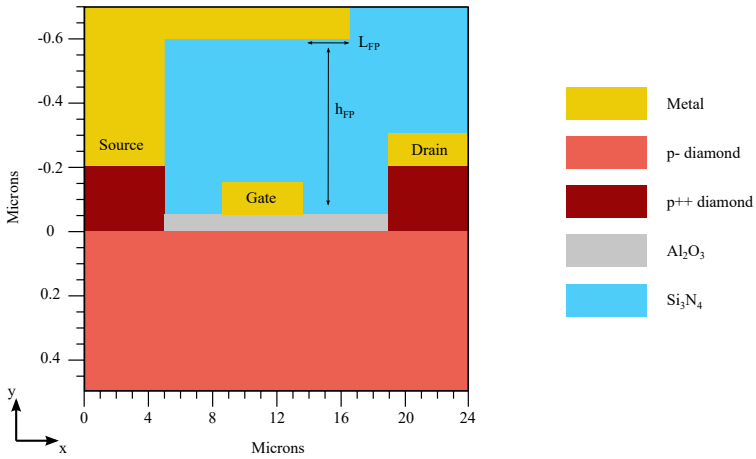


Figure 5: Schematic of a source-field-plate D3MOSFET with a passivation layer made of Si_3N_4.

3.2. Design optimization

The optimal sizing of the field-plate is performed through 2D numerical simulations using Silvaco ATLAS by varying the two geometrical features, meaning L_{FP} and h_{FP}, and by tracking the device electric field at the hot spots. The sensitive spots are displayed in figure 6a within: (i) the diamond, (ii) the gate-oxide and (iii) at the field-plate edge with the corresponding cutlines along the x-axis. Indeed, the addition of the field-plate leads to a relocation of the hot spot at the field-plate edge with a larger peak electric field observed than under the gate in the diamond and gate-oxide material. Therefore, for each variation of the geometrical features, the maximum electric field is evaluated and reported in figures 6b, 6c and 6d for the cutlines along the x-axis within the diamond, the gate-oxide and at the field-plate edge. Here, the simulation results for the source field-plate are presented for V_{gs} = 40 V and V_{ds} = -200 V. From these simulation results, one can clearly see the benefits of the field-plate on the peak electric field in both diamond and gate-oxide layers. Indeed, the peak value in the diamond, respectively gate-oxide, has decreased from 5 MV/cm, resp. 6.6 MV/cm, without the field-plate to an average value of 3 MV/cm, resp. 3.4 MV/cm, with the presence of a field-plate.

Concerning the peak electric field variation for various geometrical features, the same trend can be observed within the diamond and gate-oxide layers with a decrease of the peak electric field with increasing L_{FP} which is consistent with the fact that the electric field will be smoothed over a larger distance. Also, the peak electric field is increasing with increasing h_{FP} which is also consistent as the field-plate will be more efficient close to the gate-edge. On the contrary, an opposite behavior is observed for the peak electric field evolution at the field-plate edge. Indeed, the peak value is increasing with increasing L_{FP} since the border of the field-plate is closer to the drain metal, thereby increasing the electrical constraint. Moreover, for the same reason, the peak electric field is increasing with decreasing h_{FP}. Those simulations results show us that a trade-off must be found between the decrease of the electric field within the diamond and

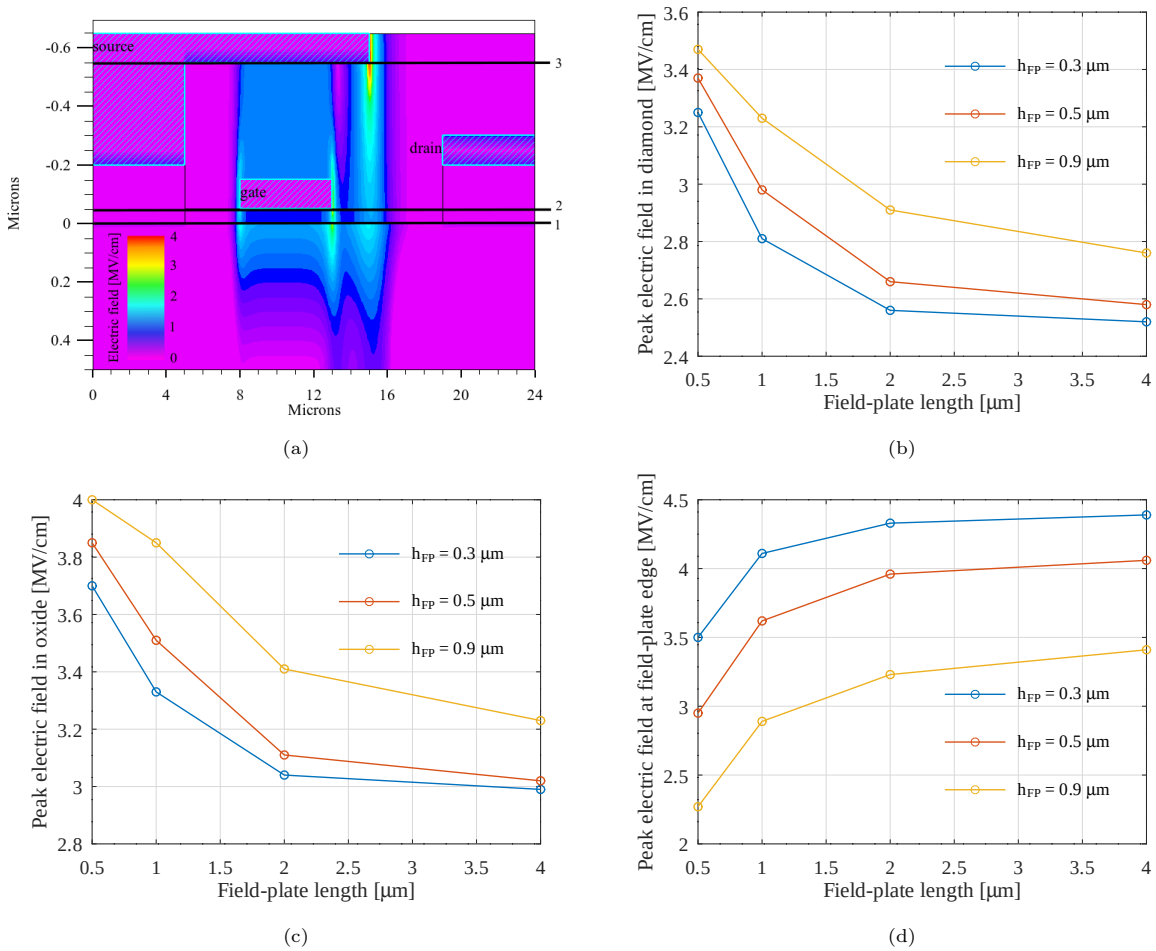


Figure 6: (a) Finite element simulation of the electric field distribution in the off-state with a drain bias of -200 V and a gate bias of 40 V with highlighted lateral cutlines. Electric field evolution according to the drain extension of the field-plate for different field-plate heights in (b) the diamond cutline, (c) the gate-oxide cutline and (d) the field-plate edge cutline.

gate-oxide material and the peak electric field observed at the field-plate edge, within the silicon nitride. Therefore, thanks to the simulation results and due to the limitations of the fabrication process, the field-plate extension at the drain side, meaning L_{FP}, will be comprised between 1 µm and 3 µm while the passivation layer thickness, meaning h_{FP}, shall be between 400 nm and 600 nm. For ease of comparison with the non-field-plated device, it is fixed $L_{FP} = 2$ µm and $h_{FP} = 500$ nm for the rest of the section.

3.3. Expected performances

The evolution of the peak electric field along the V_{ds} for an optimized structure is displayed in figure 7 for the source field-plate architecture. This figure shows the peak electric field value within the diamond (in black), the gate-oxide (in red) and in the silicon nitride (in blue) together with their corresponding critical electric fields in dashed lines. From this graph, one can clearly see that the peak electric field in both diamond and gate-oxide layers is nearly constant along the V_{ds} which demonstrates the benefit of the field-plate. Meanwhile, the peak electric field at the field-plate edge is largely increasing with increasing V_{ds}

up to a value close to 10 MV/cm around 1 kV of off-state voltage.

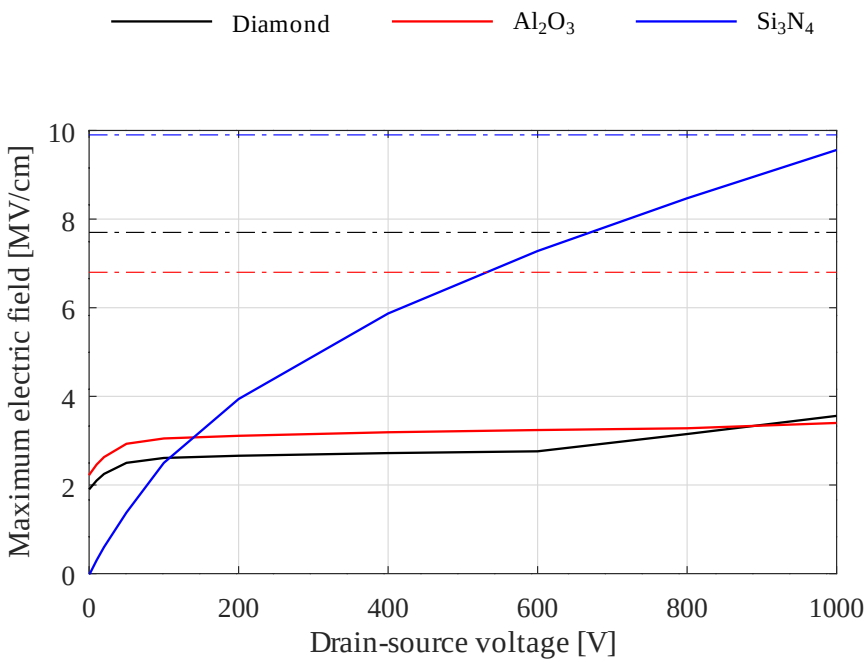


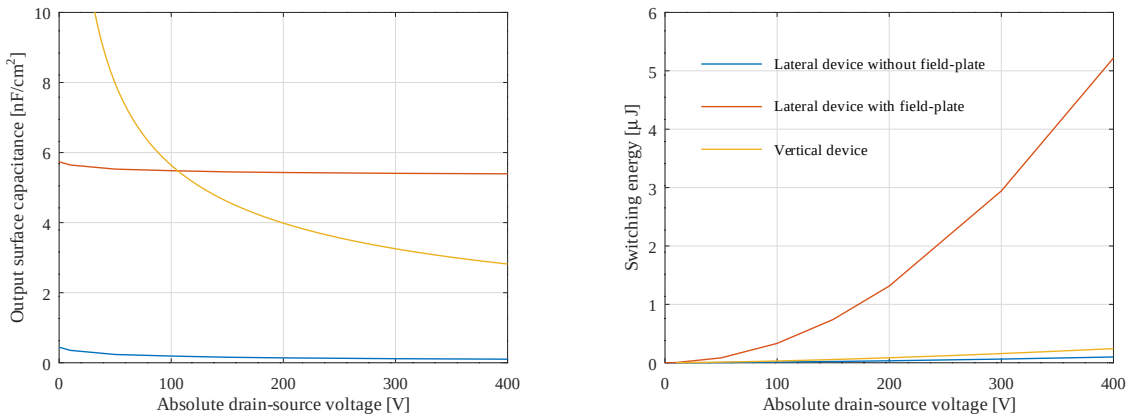
Figure 7: Maximum electric field evolution along the V_{ds} within the diamond (black curve), the gate-oxide (red curve) and the passivation layer (blue curve) for a source-field-plate. Is also displayed in dashed lines, the theoretical critical electric field of each material.

Despite the improved breakdown voltage, the passivation layer addition underneath the field-plate leads to an increase of the device total oxide capacitance, and, thereby, of the device output capacitance. This aspect is highlighted in figure 8a, where it is displayed the evolution of the output surface capacitance according to the drain-source voltage for the field-plated and non-field-plated diamond lateral device. The corresponding surface used for the calculations is $S = (L_{gs} + L_g + L_{gd}) \cdot W$, W being the total gate width. From this graph, it is clearly observed an increase of the output surface capacitance from 0.5 nF/cm^2 for the non-field-plated device to 5.5 nF/cm^2 for the field-plate one. Moreover, on this figure, both architectures are compared to a vertical diamond one as similarly described in [31]. In that case, the device specific on-state resistance and the output capacitance are calculated using equations (3) and (4). The doping density and the drift layer thickness are the ones calculated using the 1D impact ionization integral of section 2. Concerning the active surface of the vertical device it is fixed in order that the on-state resistance of both architectures (vertical and lateral) is identical, thereby leading to similar conduction losses. Compared to the lateral devices, we can see that the output surface capacitance is largely decreasing with increasing drain-source voltage with a minimum value around 3 nF/cm^2 at $|V_{ds}| = 400$ V, larger than the estimated output surface capacitance for the lateral device without the field-plate.

$$R_{on,s} = \rho(T) L_{drift} \tag{3}$$

$$C_{oss} = \epsilon_R \frac{S}{L_{drift}} \sqrt{\frac{BV}{V_{ds}}} \tag{4}$$

where ϵ_R is the dielectric permittivity of diamond material, L_{drift} is the drift layer thickness, S is the active surface and BV is the device breakdown voltage of the vertical device.



(a) (b)

Figure 8: (a) Output surface capacitance and (b) the corresponding switching energy according to the drain-source voltage for various device architectures : one vertical architecture and two lateral devices with and without the presence of a field-plate.

Based on the estimated output capacitances, the switching energy of the three architectures are calculated in figure 8b. On this graph, one can see that the non-field-plated lateral device exhibits the lowest switching energy with a value of 0.01 µJ at $|V_{ds}|$=400 V compared to 0.02 µJ for the vertical architecture and 5 µJ for the field-plated one. Therefore, the improvement of the breakdown voltage leads to a degradation of the switching energy due to the increase of the device MOS capacitance. The increase of the MOS capacitance could be further limited by increasing the thickness of the Si_3N_4 as the corresponding oxide capacitance is inversely proportional to the oxide thickness. However, it will lead to the increase of the peak electric field in the diamond and gate-oxide layers. Once more, a trade-off must be found between those two figure-of-merits.

4. Evaluation of the Si_3N_4 electrical properties for field-plate processing

According to the previous simulations, the use of a Si_3N_4 source field plate on the D3MOSFET should allow to increase the breakdown voltage up to 1kV. But this is true only if the real material properties are the same as the one used in the simulations. The goal in this section is to show that the material, that will be used for the real device, has a dielectric constant close to 7.5 and a breakdown field close to 10 MV/cm. For this purpose, metal insulating metal (MIM) capacitors have been manufactured and characterized.

4.1. Design and manufacturing process of MIM capacitor

MIM capacitors are initially fabricated on three 1 cm^2 silicon subtrates. The first step is the deposition of the bottom metal contacts by evaporation.The metal stack consists of 30 nm Ti, 40 nm Pt and 50 nm Au. Then, 400 nm of Si_3N_4 are deposited by PECVD (Plasma-Enhanced Chemical Vapor Deposition), this

corresponds to one of the values used in the simulations. Finally, the top metal contacts are deposited with a standard lift off process. Same metals have been used than the bottom contact. Figure 9 shows a schematic cross-section of the MIM capacitors (a) and an optical micro-graph of one of the samples (b).

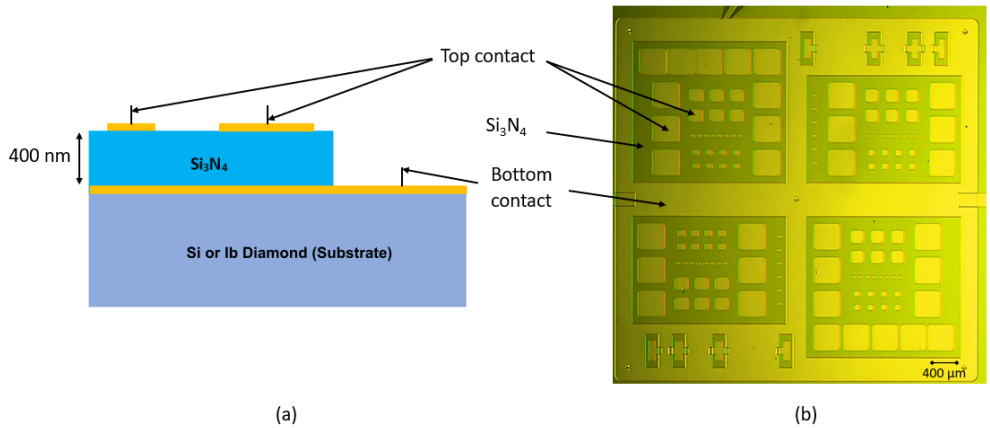


Figure 9: Design of MIM capacitors : (a) Schematic cross-section of MIM capacitors, (b) MIM capacitor device optical micro-graph.

Each device has several sizes of square MIM capacitors and other test devices. Corners are rounded to avoid field peaks. In this paper we will only focus on MIM capacitors with areas between 400x400 µm^2 and 50x50 µm^2.

4.2. Measurements and results

All measurements are made under vacuum (P $\approx 10^{-4}$ mbar) and at room temperature. To obtain the dielectric constant and the breakdown field of Si_3N_4 two types of measurements are realized. The capacitance is measured to calculate the dielectric constant using equation (5). Measurements are done with a Modulab XM MTS at 10 kHz frequency. The capacitance limit detection of this equipment is 0.1 pF.

$$\epsilon = \frac{eC}{\epsilon_0 S} \tag{5}$$

In equation (5), ϵ is the dielectric constant, e is the thickness of Si_3N_4, C is the capacitance, ϵ_0 is the vacuum permittivity, and S is the surface area of the capacitor. Here we make the approximation that the surface area of the capacitor is equal to the top contact surface. Then, the breakdown field is calculated by plotting the current-voltage characteristic of the component until reaching the breakdown voltage and using the equation (6). An example of this characteristic is shown on figure 10. Measurements are done with a 2410 Keithley which has a current detection limit of 10 pA.

$$E_c = \frac{V_{BD}}{e} \tag{6}$$

where E_c is the breakdown field and V_{BD} is the breakdown voltage. Results presented are the average of what is obtained for the 3 processed samples. According to the measurements made, the dielectric constant is equal to 6.6. Table 1 shows the values obtained for the breakdown electric field. The larger the electrical contact, the lower the breakdown field. This is due to a higher probability to have defects when contacts

are larger. According to the results, and the graph of figure 7, the improved D3MOSFET transistor should therefore have a breakdown voltage between 700 V and 900 V which agrees with the targeted values.

4.3. Validation of results on diamond substrates

To support the obtained results, MIM capacitors were then performed on two diamond samples with the same procedure as in section 4.1. The aim is to show that the properties of Si_3N_4 stay the same on diamond substrate Ib and IIb 4x4 mm². They only have 50x50µm² MIM capacitors. Current versus voltage characteristics of a MIM capacitor is shown on the figure 10.

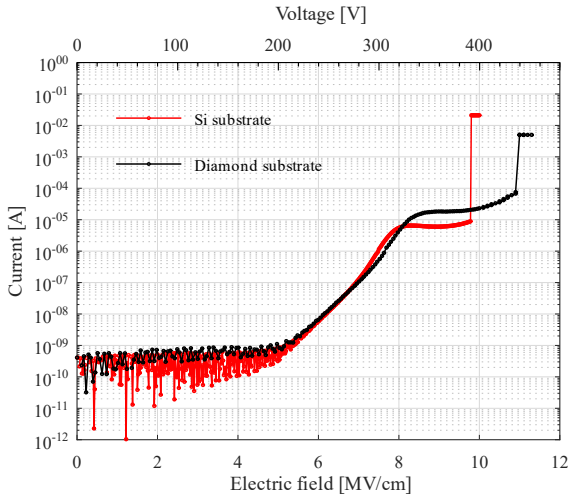


Figure 10: Current versus electric field characteristics for 50 x 50 µm² MIM capacitor on diamond and silicon substrates.

The results obtained are added to table 1.

	Breakdown electric field [MV/cm]	
Metal contact sizes [µm x µm]	Si samples	Ib Diamond samples
400 x 400	7.9 ± 0.2	
200 x 200	8.3 ± 0.2	
100 x 100	8.8 ± 0.1	
50 x 50	9.1 ± 0.3	10.7 ± 0.3

Table 1: Summary table of the results obtained on the electric fields of breakdown of Si_3N_4 on silicon and diamond samples.

With the breakdown electric fields obtained on these samples, it would be theoretically possible to have a device with a breakdown voltage of more than 1000 V. The difference of results between silicon and diamond samples has not yet been explained, but some hypotheses can be done. During the PECVD deposition, constraints appear in the deposited layer and the smaller the sample, the more the layer is constrained. This could be an explanation. It is also possible that the deposition process is not perfectly stable and that the properties of Si_3N_4 vary a little from one time to another. Nonetheless, the obtained values for the two different substrate materials validate the suitability of Si_3N_4 as a source field plate dielectrics.

5. Conclusion

The feasibility of a lateral field-plated deep depletion diamond MOSFET has been investigated. The study was based on 2D TCAD simulations in order to determine the geometrical features of the field-plate. The simulations results show a potential breakdown voltage between 700 V to 900 V, close to the targeted value of 1 kV. Investigations were also performed regarding the passivation layer made of Si_3N_4 required for the field-plate architecture. Measurements on MIM capacitors on both silicon and diamond substrates have shown encouraging results with an extracted critical electric field between 8 and 11 MV/cm, consistent with the 10 MV/cm used during the simulations. Therefore, based on the different analysis, the field-plated architecture for the D3MOSFET device could allow a large increase of the breakdown voltage compared to the former designs and compete with other diamond architectures such as HFET or MOSFET with NO_2 doping.

Credit authorship contribution statement

Marine Couret - Conceptualization, Methodology, Software, Validation, Formal Analysis, Investigation, Writing - Original Draft **Damien Michez** - Conceptualization, Methodology, Validation, Formal Analysis, Investigation, Writing - Original Draft **Juliette Letellier** - Conceptualization, Methodology, Writing - Review and Editing **Anne Castelan** - Methodology **Julien Pernot** - Methodology **Nicolas Rouger** - Conceptualization, Methodology, Validation, Writing - Review and Editing, Project administration, Funding acquisition

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The figures raw data presented in this manuscript are available on Zenodo [32].

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