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***Abstract*— This work presents a new method of noise model implementation for circuit simulations, which enables the generation of Lorentzian-type spectra. The importance of Lorentzian noise modeling is explored in contrast to classic 1/f or Random Telegraph Noise (RTN) modeling, in terms of PSD, total noise power, and device-to-device noise variability reproduction, through analysis of experimental data. The Verilog-A modeling methods for both types of Lorentzian noise are demonstrated and validated, using a Lambert-W function charge-based drain current model. Finally, fundamental digital and analog circuits such as the Ring Oscillator are used to showcase the usefulness and applicability of the "VERILOR" model in circuit noise simulations.**

***Index Terms* – Low-frequency noise, G-R noise, Lorentzian noise, Random telegraph noise, Noise Variability, Tri-Gate Nanowire MOSFETs, Verilog-A, Circuit noise**

I. INTRODUCTION

With the incorporation of new materials and device architectures under the demand of "More Moore" and "More than Moore" technology roadmaps, defect-related effects such as low frequency noise (LFN) are attracting more attention by the semiconductor industry. The LFN level increases with the device downscaling [1], while there is also the appearance of Lorentzian spectra instead of 1/f-like [1]. This type of power spectral density (PSD) shape may originate either from oxide trap-related random telegraph noise (RTN) signals (leading to 1/f in large area oxides) or generation recombination (G-R) centers in the MOSFET channel region [1]. Whatever the origin or PSD form, LFN results to instabilities in both digital [2] and analog circuits [3], therefore its accurate modeling is crucial for the reliable design and safe operation of circuits.

While various works have been presented on the time-domain modeling of the RTN effect for circuit simulators [2,4], there are very few that concern the modeling of Lorentzian noise sources directly in the frequency domain [5]. The latter could, on one hand, significantly reduce the noise simulation time, and on the other hand enable a direct and accurate simulation of the PSD for circuits, such as the oscillators, where the noise is important to be studied in the frequency domain. Moreover, the pre-existing PSD modules in Verilog-A are limited to 1/f and white noise, therefore the Lorentzian type of noise needs a dedicated module to be developed. In this work, we present a method for the implementation of Lorentzian noise spectra in Verilog-A, in a way that can automatically generate Lorentzian or 1/f noise depending on the trap density and the oxide area, for all bias conditions. After underlining the advantages of Lorentzian modeling with regards to 1/f and time domain modeling of RTN, with the help of a Lambert-W function charge-based drain current model [6], we demonstrate our module's applicability in circuit simulators, and how it can enable precise noise variability studies at a circuit level. Finally, some circuit noise application examples are shown, revealing for example how a ring oscillator's (RO) phase noise can be impacted by the presence of a Lorentzian-type PSD.

II. SIMULATION SET-UP AND TEST DEVICES

In order to explain the motivation for our modeling idea, and how it can prove very useful for emerging technology devices, we used experimental results from measurements performed on Tri-Gate Nanowire SOI p-channel FETs, fabricated by CEA-LETI [7]. They consist of a 145 nm thick buried oxide, a Si film of H = 11 nm and a 2 nm Equivalent Oxide Thickness (EOT) HfSiON gate dielectric with TiN metal gate. Drain current PSD measurements were performed with the programmable bias point probe system NOISYS. Both the device- and circuit-level noise simulations were performed with the Cadence Spectre simulator.

III. LORENTZIAN NOISE MODELING

As already mentioned, the miniaturization of the devices increases the probability of the existence of isolated traps as opposed to large oxide areas. In this case the main LFN source stops being 1/f-like but instead appears a Lorentzian-like dependence: plateau at low frequencies and $1/f^2$ dependence above a certain cut-off frequency f_c, as described by (1), where S(0) the plateau at 0 Hz.

$$S(f) = \frac{S(0)}{1 + (f/f_c)^2} \quad (1)$$

In many publications RTN is modeled in the time domain [2,4]. The advantage of this method is that the state of a circuit can be accessed at any time and so possible errors due to RTN can be examined. However, concerning variability studies or multiple traps with huge spans of time constants, transient circuit simulations can take very long, while the situation becomes even more difficult when increasing the number of components in a circuit.

To overcome time-consuming issues, but also be able to directly perform noise spectrum simulations, the RTN modeling in the frequency domain becomes crucial. To do so, the authors of some publications use the LFN variability level, σ(log(S)), extracted from experiments or models and add the +/- 3σ to the 1/f average spectrum [8], in an effort to cover the extreme LFN level variations induced by RTN. By doing this, although the safe design of a circuit in terms of LFN is succeeded, the LFN level itself might be significantly overestimated or underestimated. To outline this phenomenon, we show in Fig. 1 a set of 93 experimentally measured input-

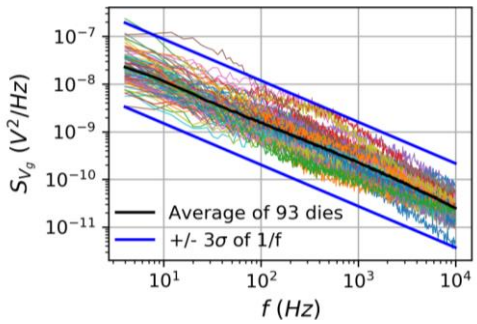

Fig. 1. Measured input-referred gate voltage noise spectra on TriGate Nanowire MOSFETs, plotted together with the log-mean spectrum and the +-3σ 1/f spectra based on the 1/f variability modeling. (W_{eff} = 52nm / L = 30nm, V_g = 1V, V_d = 50mV).

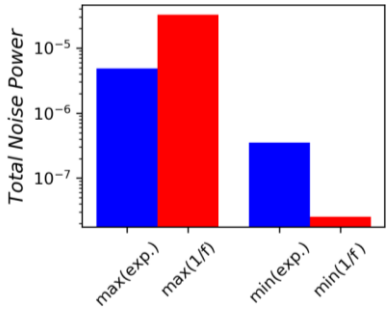

Fig. 2. Experimental minimum and maximum noise power along with the +/- 3σ power of 1/f variability model in red.

referred gate voltage noise spectra, along with the +/- 3σ limits added to the average 1/f, with σ(log(S_{Vg})) extracted at 20 Hz. We chose a very small gate area device so as to increase the noise variability and the probability of RTN traps. As shown in Fig. 1, the +/- 3σ spectra fails to accurately estimate the maximum and minimum extreme conditions. Furthermore, what's even more important is not the value of the PSD at a certain frequency, but the total noise power of the fluctuations for each die calculated by integrating the PSD over the whole frequency range, as in (2):

$$\sigma_{Vg}^2 = \int_{f_{min}}^{f_{max}} S_{Vg}\,df \tag{2}$$

The maximum and minimum total noise power of the experimentally measured spectra and the ones taken from 1/f +/- 3σ were calculated using (2) and are depicted in Fig. 2. The huge difference observed in both the maximum and minimum noise power between data and 1/f model reveals both the importance and the need for a different type of modeling approach for highly downscaled devices. This difference can be nonetheless understood, if we take as an example the expected noise power of a 1/f and a Lorentzian spectrum that coincide at 10Hz (Fig. 3(a)), a typical frequency for the extraction of characteristic noise levels. Combining (1) and (2), the Lorentzian integral can be explicitly expressed through (3):

$$\sigma_{Vg,Lor}^2 = S_{Vg}(0) f_c \left(\tan^{-1}\frac{f_{max}}{f_c} - \tan^{-1}\frac{f_{min}}{f_c}\right) \tag{3}$$

Concerning the flicker (1/f) noise spectrum, its total power can be easily calculated through (4),

$$\sigma_{Vg,Flick}^2 = S_{Vg}(1) ln(f_{max}/f_{min}) \tag{4}$$

where S_{vg}(1) the 1/f PSD value at 1 Hz.

Using (3) and (4), we obtained the total noise power of the Flicker and Lorentzian spectra shown in Fig. 3(a), and plotted in Fig. 3(b) versus a varying bandwidth f-f_{min}. It is worth noting that, while the Lorentzian PSD amplitude is 2 orders of magnitude below 1/f at the lower and the higher edges of the bandwidth, the total noise power of the Lorentzian spectrum becomes significantly higher (1 order of magnitude), even for a bandwidth equal to its cut-off frequency f_c.

We proceed to emulate the experimental variability using a PSD level generator, that considers a Lorentzian noise spectrum for each RTN fluctuator and their sum for each die, as already done in [9], through (5):

$$S_{Vg}(f)_d = \sum_{k=1}^{N_{T,d}} \frac{4\Delta V_{t,k}{}^2 A_k \tau_k}{1+(2\pi f \tau_k)^2}$$
$$\Delta V_{t,k} = \frac{q(1-x_{t,k}/t_{ox})}{WLC_{ox}}, A_k = \frac{\tau_k}{\tau_c+\tau_e},\ \tau_k = \left(\frac{1}{\tau_c}+\frac{1}{\tau_e}\right)^{-1} \tag{5}$$

where $N_{T,d}$ is the total number of active traps for die 'd', k the index, ΔV_t the RTN amplitude, A the space mark ratio, τ_c and τ_e the mean capture/emission time constants of each trap. N_T was chosen for every die from a Poisson distribution with an average $<N_T> = N_t WL t_{ox} \Delta E$, where N_t the oxide trap density per volume per energy and ΔE the total energy bandgap. Moreover, for the calculation of τ_c and τ_e we implemented a simplified SRH-like approach, as in (6):

$$\tau_c(V_g) = \tau_0 \frac{Q_i(V_t)}{Q_i(V_g)}\ ,\quad \tau_e = \tau_0 e^{\frac{\Delta E_T}{kT}} \tag{6}$$

where τ_0 is a time constant distributed exponentially between 1 ns and 1 ks, and Q_i is the inversion charge density calculated using Lambert-W function. ΔE_T is the difference between the trap and the Fermi energy levels, ranging between -5kT and 5kT, in order to cover all possibly active traps for every bias.

As it is shown in Fig. 4, although the 1/f variability (Monte Carlo results) follows well the experimental data at 20 Hz, where we extracted the σ, it fails to do so at higher frequencies, i.e. 120 Hz, and its prediction is even worse regarding the total noise power, σ^2_{Vg}, estimated by (2). On the other hand, our model, using (5) and (6), can reproduce well the experimental variability in all cases, proving its usefulness and accuracy for circuit-level LFN simulations.

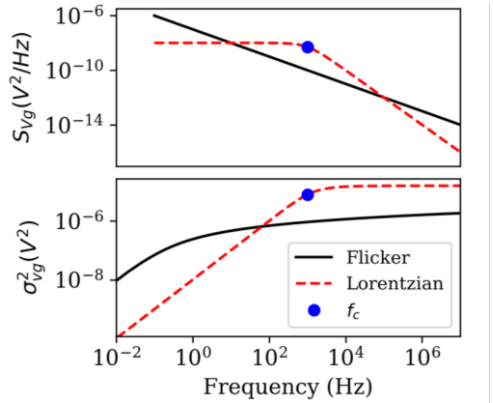

Fig. 3. 1/f versus Lorentzian noise (with f_c at 1kHz), in terms of PSD versus frequency (top) and total noise power versus bandwidth (bottom). The 1/f magnitude coincides with Lorentzian plateau at f = 10 Hz.

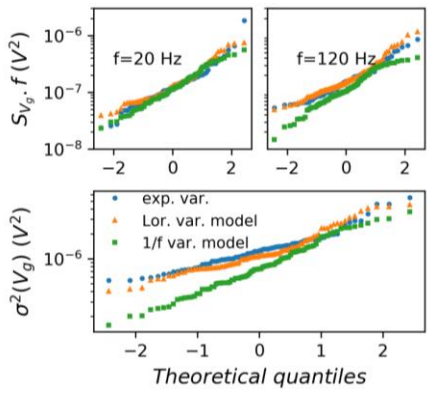

Fig. 4. Quantile Plots of measured input-referred gate voltage PSD in two frequencies 20 and 120 Hz (top) and total power (bottom).

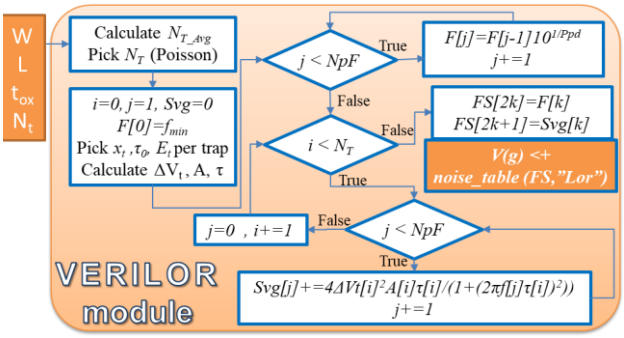

Fig. 5. Flowchart of the VERILOR module. *NpF: total number of points in spectrum; Ppd: points per frequency decade; f_{min}: starting frequency*

IV. Proposed "VERILOR" Model

A. Automatic noise table method

Since there is no possibility for declaring a noise source in Verilog-A through a PSD function different than 1/f (*flicker_noise*) or thermal (*white_noise*) noise, we developed our module using the third option: the *noise_table* function. The latter takes an array of pairs of values (frequency and PSD) as input, leaving the SPICE simulator to interpolate the in-between regions. Therefore, after the automatic creation of a table with frequency values, with a resolution and bandwidth that can be user-controlled, the table of PSD values actually uses (5) and sums up the Lorentzian contributors from all active traps. The calculation of N_T, ΔV_t, A and τ follows the procedure described in Section III, like in [10], where a similar module was presented for RTN modeling in the time domain. In the end, the frequency (*F*) and PSD (*Svg*) tables are intertwined (odd/even indexes) together in a new table, *FS*, that is loaded in the *noise_table* function and inserted as a noise source at the FET gate. The flowchart of our VERILOR module is shown in Fig. 5.

B. Model validation

In order to confirm the validity of our model and its Verilog-A implementation, we simulated the LFN induced by three individual traps, in a single device. We compared the simulated spectra against (5), using the same trap parameters (x_t, τ_0, E_t). As demonstrated in Fig. 6(top), model and theory are in full agreement in terms of PSD shape. In Fig. 6 (bottom) we also illustrate how a g-r noise source from the channel can also be implemented on top of 1/f, by adding both *flicker_noise* and *VERILOR* contributors.

V. Simulation Examples with "VERILOR" Module

A. Scaling: from Lorentzian to 1/f noise and CNF

We performed additional simulations for different gate areas and corresponding total number of traps. As we demonstrate in Fig. 7 (top), the VERILOR module can automatically reproduce Lorentzian-like spectra in highly scaled areas and 1/f-like in larger ones. On top of that, it is able to generate a 1/f noise level that is in total agreement with the area-normalized carrier number fluctuation (CNF) model from weak to strong inversion (Fig. 7 (bottom)).

B. Time-domain RTN and dynamic variability

When it comes to simulating RTN in circuits, if what matters is the RTN amplitude and not so much its sudden transition events, VERILOR can be combined with the simulator's Transient Noise module, to fairly reproduce the power of the RTN signal, as shown in Fig. 8. Both methods (classic RTN time-domain model [10] and frequency domain VERILOR module) lead to the same spectra, and to time-domain signals of the same RMS power. Therefore, the level of dynamic variability can be accurately predicted by VERILOR, even with no RTN module in the time domain.

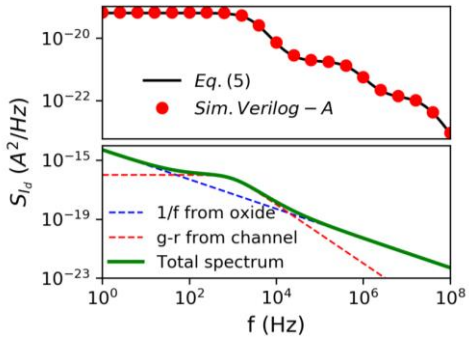

Fig. 6. PSD comparison between the Lorentzian spectrum obtained by our Verilog-A model and the calculated one using the same parameters (x_t,τ_0,E_t) (top). G-R noise on top of 1/f in Verilog-A (bottom).

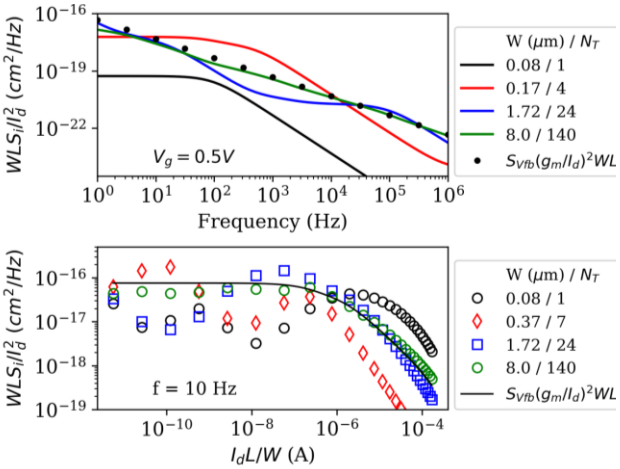

Fig. 7. Area-normalized PSD of I_d versus frequency at V_g=0.5V (top) and versus normalized current for f = 10 Hz (bottom), for 4 different W and corresponding N_T, along with CNF model. (L = 0.3μm)

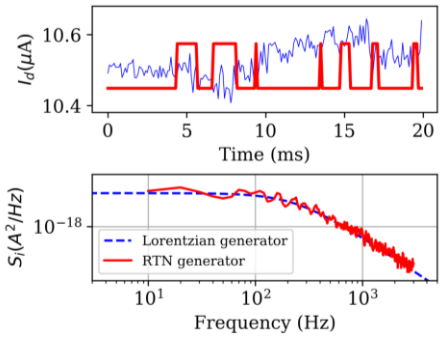

Fig. 8 Drain current transient signal of LW-based MOSFET (top), for direct RTN generator and Transient Noise signal based on the Lorentzian spectrum (bottom), which agrees with the RTN spectrum.

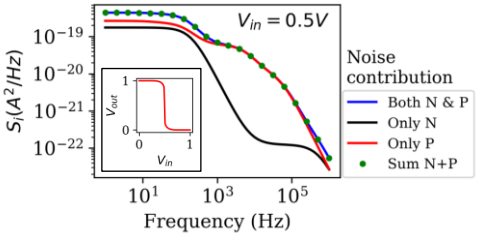

Fig. 9. Output current PSD of LW-based CMOS inverter (inset showing I/O curve) versus frequency for V_{in}=0.5V, along with separate noise contributions from each MOSFET, and their sum. (W=80nm/L=30nm).

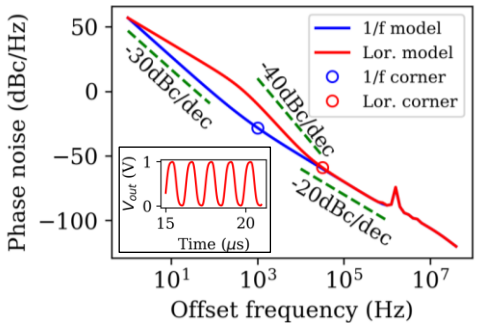

Fig. 10. Phase noise of LW-based 3-stage CMOS ring oscillator (signal in inset) versus offset frequency for 1/f and Lorentzian noise. The 1/f magnitude coincides with the Lorentzian plateau at 1 Hz.

C. Frequency domain and LFN variability

As an easy and direct way to verify that the VERILOR module can be successfully used in a circuit with many transistors, we compared the total output noise to the sum of the individual device spectra for a CMOS inverter (Fig. 9) with highly scaled devices (only a handful of active traps). Moreover, in circuits like oscillators, the LFN up-converts to phase noise close to the oscillation frequency, f_0, making the frequency domain noise simulation crucial. Using the VERILOR module, we estimated the impact of Lorentzian noise on a 3-stage Ring Oscillator's phase noise. As can be seen in Fig. 10, while 1/f up-converts to $1/f^3$, a Lorentzian spectrum up-converts to $1/f^2$ close to f_0 and then $1/f^4$ after the Lorentzian's cut-off frequency, f_c. As a result, for a scenario where 1/f coincides with the Lorentzian at 1 Hz, the phase noise becomes significantly higher around f_c, while the corner frequency, i.e. where LFN meets the thermal noise level, is shifted upwards by more than one decade.

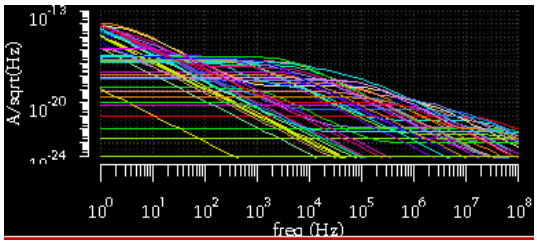

Fig. 11,. Screenshot of noise variability (60 dies) simulation results in Cadence Spectre, using the VERILOR module. (W=80nm/L=30nm)

This observation underlines the importance of Lorentzian noise modeling in RF/mixed signal circuits, where the operation bandwidth is a critical Figure of Merit. The opposite (lower phase noise and corner frequency) could also take place, if the Lorentzian has a lower plateau, due to the device-to-device variability as explained in III. Thus, it is important to showcase (Fig. 11) how the VERILOR module can also reproduce the LFN variability effect in a circuit simulator, using the physics-based approach of (5)-(6).

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