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***Abstract*—Surface electrode ion trap is highly promising for practical quantum computing due to its superior controllability on the trapped ions. With advanced microfabrication techniques, silicon has been developed as ion trap substrate for delicate surface electrodes design as well as monolithic electro-optical components integration. However, the high RF loss of silicon hinders the possible large-scale implementation. In this work, we demonstrate a through silicon via (TSV) integrated ion trap, which has low RF loss due to the elimination of wire bonding pads on the surface and the miniaturization of form factor. We also fabricate two types of conventional wire bonding (WB) traps with or without a grounding screen layer. The RF performance of different ion traps are tested and compared, in terms of on-chip *S*-parameter, post-packaging resonance and resulting power loss. The results show that TSV trap has low S21 (~0.2 dB at 50 MHz), high *Q* factor (~22) and low power loss (0.26 W) as compared to WB traps. In addition, 3D finite element modelling is employed for electric field visualization and RF loss analysis of different traps. The extracted results from the modelling show a decent agreement with the measurements. In addition to various RF tests, the design, fabrication and ion trapping operation of different ion traps are presented. This work provides insights into RF loss of ion trapping device and offers a new solution for RF loss reduction.**

***Index Terms*—Surface Electrode Ion Trap, TSV, RF Test, *S*-parameter, Finite Element Modelling**

I. Introduction

Quantum computing offers excellent efficiency in handling problems which are intractable even for most advanced supercomputers (e.g., large numbers factoring, complex functions optimizing and quantum phenomena simulation), due to the fact that quantum bit (i.e., qubit) is able to represent $|0\rangle$ and $|1\rangle$ simultaneously [1]. Currently, the most popular candidates for physical qubits implementations are superconducting circuit and trapped ion. With the elimination of strict cryogenic environment as well as the development of surface electrode ion trap, trapped ion has shown its superior scalability as compared to the superconducting circuit [2]. Considering the requirement for large number of physical qubits (on the order of 1,000,000) for practical quantum calculations [3], a highly scalable quantum computation system is preferred.

In a surface electrode ion trap, ions are confined above the electrode surface at a certain height (i.e., trapping height) by a combined electric field generated from co-planar RF and DC surface electrodes. The center where ions are trapped has a minimum pseudopotential as compared to the surroundings [4]. For a typical ion trap design, RF electrodes width together with the gap width between them will determine the ion trapping height, whereas DC electrode are used to confine ion in axial direction and compensate stray electric field [5]. On the other hand, laser beams are used for ion cooling with Doppler cooling or sideband cooling technique. Similarly, lasers or microwaves are adopted to manipulate the internal state of ions and flip the qubit between $|0\rangle$ and $|1\rangle$. The readout of ion state is achieved by coupling one state ($|0\rangle$ or $|1\rangle$) to a cycling transition and collecting the emitted fluorescence, while no similar transition arises for the other state [6].

With the well-established fabrication techniques and the promise of silicon photonics integration, ion traps on silicon substrates have drawn great attention in the ion trapping community [7]. However, the challenge of high RF loss of silicon shall be overcome to fulfill the requirement for large-scale integration [8, 9]. One possible solution is to protect lossy silicon substrate from RF signal penetration. For this purpose, a grounding plane can be inserted between surface electrodes and silicon substrate [10-12]. Besides, in a work reported by Niedermayr et al. [13], an intrinsic silicon substrate is used at cryogenic environment to freeze out the charge carriers and transfer silicon into a good insulator. Another solution is to fundamentally reduce the parasitic capacitance, which dominates the RF loss of ion trap. In principle, by increasing

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the thickness of dielectric layer (e.g., SiO_2) between surface electrode and silicon substrate, the loss issue can be mitigated. However, to achieve this, the required dielectric layer thickness is >10 μm, where the deposition and patterning are not compatible with CMOS process [7]. On the other hand, minimizing the parasitic through electrodes area reduction without affecting ion trapping performance is called for.

For this propose, we present the integration of through silicon via (TSV) into ion trap in place of wire bonding. By eliminating the large wire bonding pads and corresponding parasitic, we anticipate that a low-loss trap can be achieved. Glass interposer with redistribution layer (RDL) on the surface is used to locate the TSV integrated trap. The traps that use wire bonding with or without grounding plane are also fabricated. RF characterizations (e.g., S-parameter measurement and resonator test) are conducted on these traps and the corresponding results are evaluated and benchmarked. Meanwhile, the finite element modelling (FEM) is used for extracting the electric field distribution and analyzing RF related performance. The results from measurement and simulation are compared. Note that the superior RF performance of glass interposer over silicon counterpart has been demonstrated in our earlier work [14]. Based on that, in this work, we aim to highlight that the integration of TSV into ion trap is able to allow comparable, or even more favorable performance as compared to the conventional approach using grounding plane, where a quantitative analysis in terms capacitance, equivalent series resistance and power loss is provided.

In addition to form factor reduction, the integration of TSV also benefits for the laser path. Vias located in the half space underneath electrodes will never disrupt the laser beams [15]. Also, electrodes design with complex geometry becomes feasible since higher degree of freedoms are offered by the TSV, micro bump and RDL.

This work begins with a brief introduction of trapped ion based quantum computing and the motivation of TSV integration into ion trap in Section I. The ion trap design related specifics are given in Section II, where the reduction of electrodes surface is underlined and its possible effect to ion trapping performance is discussed. In Section III, fabrication processes of various traps are presented with details. Section IV and V compare the RF related performance of different traps obtained both from measurement and simulation. The ion trapping performance of TSV integrated ion trap is given in section VI. Section VII discusses the heating dissipation issue encountered by TSV trap and proposes possible solutions. Finally, key findings and conclusions are highlighted in Section VIII.

II. Ion Traps Design

Two categories of ion traps that respectively use wire bonding or through silicon via as interconnections are designed. In wire bonding category, a version with grounding plane underneath is also developed. They are labelled as WB, WB-GND and TSV trap accordingly.

For both WB and WB-GND traps, a 5-wire geometry (DC-RF-DC-RF-DC) is adopted for surface electrodes design (Fig. 1(a)) [16], where the dynamic electric field from two symmetric RF electrodes is used to trap the ions in radial plane. The central three electrodes (RF-DC-RF) have a width of 80 μm. The dimensions of other surface electrodes are proportional to this electrode width. In addition to the core geometry for electric field generation, wire bonding pads are required as extensions for all the surface electrodes. Due to the laser path blocking issue, the bonding wires shall be kept with a sufficient distance to the trapping center. This further increases the occupied area of bonding pad and restricts the design flexibility of surface electrode itself. The final size of WB traps are ~ 8 mm × 8 mm.

The TSV trap geometry is modified based on that of WB trap, in which only core region is preserved but wire bonding pads and connecting circuits are transferred to an interposer located underneath, as demonstrated in Fig. 1(b). A vertical signal transmission path is thus created from RDL on the interposer to the surface electrodes on the TSV trap through TSV and micro bump. The elimination of wire bonding pads drastically reduces the form factor of TSV trap (to ~ 2 mm × 3 mm) as well as the corresponding parasitic.

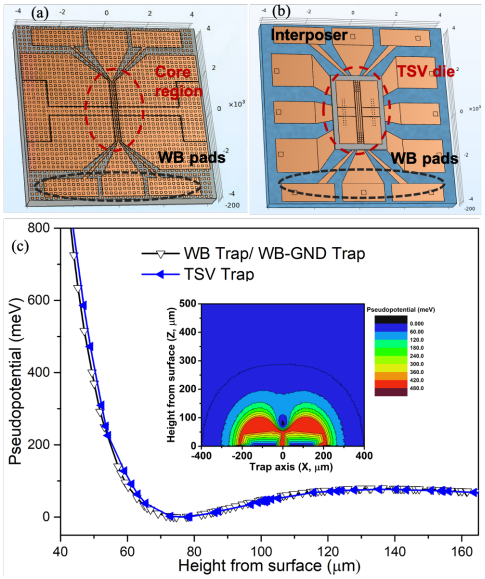

Fig. 1. (a) 3D model for WB-GND trap in finite element modelling. A grounding plane with meshed pattern is placed between surface electrode and silicon substrate. WB trap features identical geometry but lacks grounding plane. (b) 3D model for TSV trap. Core region of WB trap is reserved, whereas wire bonding pads are transferred to interposer. (c) Pseudopotential distribution in vertical direction of different traps. Inset: pseudopotential distribution in radial plane. Ions will be trapped at the point that has minimum pseudopotential.

TABLE I
Electrical and Thermal Materials Properties Employed in Simulation

Material Properties	Si	SiO_2	Cu
Conductivity (S/m)	10	0	6E7
Relative permittivity	11.7	4.2	–
Relative permeability	1	1	1
Thermal conductivity @ 300 K (W/(m·K))	150	1.2	380
Heat capacity @ 300K (J/(kg·K))	700	730	385

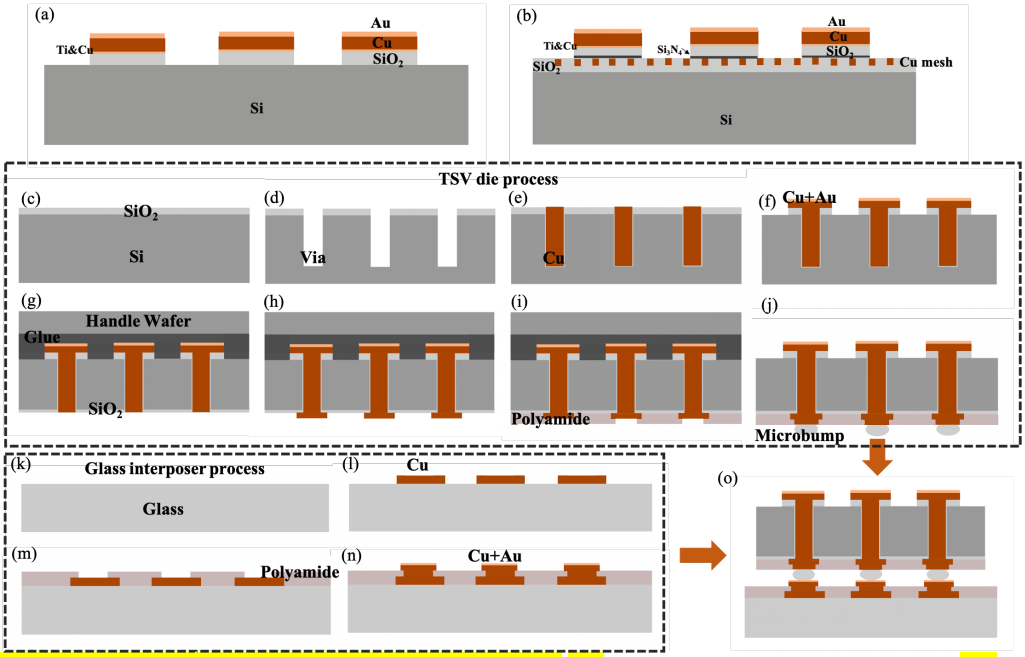

Fig. 2. (a) Schematic of fabricated WB trap. (b) Schematic of fabricated WB-GND trap. (c-f) Front-side fabrication process of TSV trap. (g-j) Back-side fabrication process of TSV trap. (k-n) Fabrication process of glass interposer. (o) Fabricated trap and interposer are aligned and bonded together.

To evaluate the possible effect from the wire bonding pad elimination, a finite element modelling (FEM) is conducted. Taking advantage of the COMSOL Multiphysics, the electric field distribution above electrode surface of different traps can be visualized and analyzed. By searching the minimum potential point, the theoretical ion trapping position can be pinpointed. Similarly, the trapping depth (i.e., potential difference between trapping point and saddle point) before and after bonding pads elimination can be extracted (Fig. 1(c)). As expected, we find the change in terms of trapping height (~76 μm) and trapping depth (~80 meV with an RF signal of 200V and 60 MHz) are negligible. Note that three dimensional models of different ion traps are built in the simulation according to the exact dimensions. The various electrical and thermal properties of materials are shown in Table I [17]. Though 3D model is not required for above-surface electric field visualization, it becomes indispensable in the following RF related simulations.

III. Ion Traps Fabrication

WB, WB-GND and TSV traps are all fabricated with standard CMOS back-end process on a 12-inch wafer fabrication platform. The detailed fabrication process of WB and WB-GND traps are given in the previous work [18]. The schematics of fabricated WB trap and WB-GND trap are respectively shown in Fig. 2(a) and (b). Here we highlight some key steps during fabrication.

Regarding the WB trap fabrication, 2 steps of lithography are used. The first one is to etch 3 μm SiO_2 insulation layer, whereas the other one is to define Cu and Au electroplating process. We did not introduce additional barrier layer between Cu and Au due to two following reasons. First, based on the result from XPS depth profiling, the formed Au-Cu interface is kept sufficiently far from the Au surface [17]. Second, the widely-used barrier layer Ni is ferromagnetic, making it unsuitable in the application of ion trap. The electrode geometry is same as the SiO_2 layer geometry underneath, preventing exposed dielectric from charging and inducing stray electric field. Adhesion and seed layer etching in the narrow gaps between electrodes is a challenge. The time of isotropic wet etching shall be closely controlled since any over etching could result in undesired undercut of electrodes.

Before the patterning SiO_2 insulation layer and surface electrodes, WB-GND trap fabrication requires one additional lithography for Cu grounding plane formation, in which 1 μm Cu damascene process is employed. The grounding plane is designed with a mesh structure instead of a solid plane to balance the trade-off between the RF loss reduction and the stress induced by CTE mismatch between Cu and SiO_2.

TSV trap fabrication mainly consists of three parts: the fabrication of TSV die on Si substrate, the fabrication of interposer on glass substrate, and the alignment and bonding of TSV die and interposer.

In the fabrication of TSV die on Si substrate, we adopt via-first approach, in which TSV is etched and filled before surface electrode patterning. First, a 2.4 μm SiO_2 layer is deposited onto Si wafer by chemical vapor deposition (CVD) as insulation layer (Fig. 2(c)). A photoresist with thickness of ~7 μm is used to define the 20 μm diameter via etching. To form 100 μm deep blind via in Si substrate (2.4 μm SiO_2 is first etched), ~400 cycles of Bosch etching process is required (Fig. 2(d)). Next, a 0.75 μm SiO_2 is deposited onto via sidewall to insulate the TSV core (Cu) from Si substrate. Before the electrochemical plating (ECP) of TSV core, barrier (0.2 μm Ta) and seed (1 μm Cu) layer are deposited by physical vapor deposition (PVD). To completely release the stress due to the CTE mismatch between

TSV core and Si substrate, annealing of 30 minutes at 250 °C in N_2 environment is required. The chemical-mechanical polishing (CMP) after annealing is adopted to remove the Cu overburden as well as barrier and seed layers (Fig. 2(e)). Subsequently, the ~3 µm (2.4 + 0.75 µm) SiO_2 insulation layer is patterned with the similar process as WB trap (Fig. 2(f)). It should be noted that an additional SiN layer (~0.1 µm) is required to protect the exposed Cu core surface from photoresist. Before the ECP process of 3 µm Cu and 0.3 µm Au as surface electrodes, this SiN layer is removed. After etching of barrier and seed layer, the wafer frontside is temporarily bonded with a handling wafer and the fabrication of wafer back side starts.

The device wafer is first grinded to a thickness of ~110 µm, followed by ~10 µm Si etching. A 3 µm SiO_2 layer is then deposited for back side insulation. To expose TSV, both CMP and etching are required (Fig. 2(g)). Afterwards, the first lithography on the wafer back side is performed to define the patterning of RDL (3 µm Cu). After the RDL ECP, a polyamide layer (5 µm HD8930) is coated to protect the RDL from oxidization (Fig. 2(h, i)). Note lithography-defined openings are made on this polyamide layer, where micro bumps would be placed. Since the micro bump has a diameter of 25 µm (10 µm Cu and 15 µm SnAg), a thick photoresist (~30 µm) is required in the last lithography. After ECP of micro bump, the device wafer is separated from the handling wafer (Fig. 2(j)). During de-bonding process, we find some cracks on the chips at the wafer edge. As a result, the achieved yield of the device wafer (silicon) is ~80%. However, with appropriate process optimization, we are confident that this cracking issue can be solved in the future fabrication.

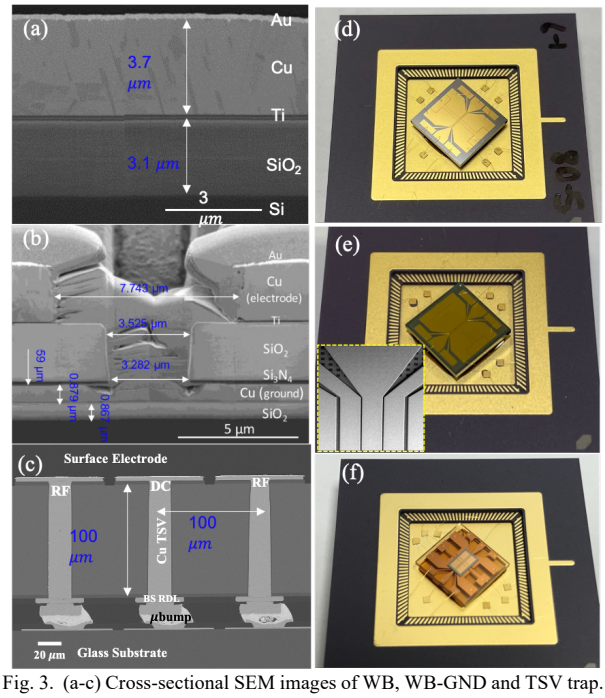

Fig. 3. (a-c) Cross-sectional SEM images of WB, WB-GND and TSV trap. TSV has a depth of 100 µm and a diameter of 20 µm. (d-f) WB, WB-GND and TSV traps assembled into CPGAs. Packaged WB-GND trap has a SEM inset showing the meshed grounding plane.

We select glass instead of silicon as interposer substrate due to its high resistivity and low permittivity, which are beneficial for RF loss reduction. The detailed comparison of interposer itself performance in terms of RF loss reduction was provided in the earlier work [14].The fabrication of glass interposer also requires three steps of lithography, which are correspondingly used for RDL patterning, passivation layer opening and to define ECP of under bump metallization (UBM) (Fig. 2(k-n)). To completely remove the oxidized metal seed residue between neighboring RDL circuits, additional dilute hydrofluoric acid and H_2 plasma etching are used. The obtained yield of interposer wafer (glass) is as up to 99%.

After diced into small chips, individual TSV die and glass interposer are assembled together (Fig. 2(o)). Three paired markers which are respectively located at the backside RDL of TSV die and frontside RDL of glass interposer are used for alignment. A reflow process with temperature of up to 220 °C is conducted to melt the micro bumps and to form solid connection. The cross-sectional SEM images and post-package optical images of different traps are shown in Fig. 3. Note that the shape of micro bump has been slightly deformed after the reflow and bonding processes.

IV. *S*-PARAMETER MEASUREMENT AND SIMULATION

The use of silicon as ion trap substrate generally suffers from high loss due to the undesired RF coupling. With on-chip *S*-parameter measurement and modelling, the loss of ion trap itself can be independently characterized before connecting it with external circuits.

The *S*-parameter measurement is performed by probing the two ends of central RF-DC-RF electrodes (3-pin probe, with a pitch of 100 µm). A two-port circuit network is thus built, where an RF signal sweeping from 10 to 110 MHz (to cover ion trapping operation range) with a step size of 1 MHz is exerted. The obtained insertion loss (S21) and reflection loss (S11) of different traps are shown in Fig. 4. Due to the shielding effect of grounding plane, WB-GND trap has a lower insertion loss than that of WB trap. Also, the smooth curve of WB-GND trap reflects the favorable stability of circuit components across the frequency range. On the other hand, TSV trap feature a significant loss reduction as compared to both WB and WB-GND traps. We attribute this RF loss reduction to the effect of

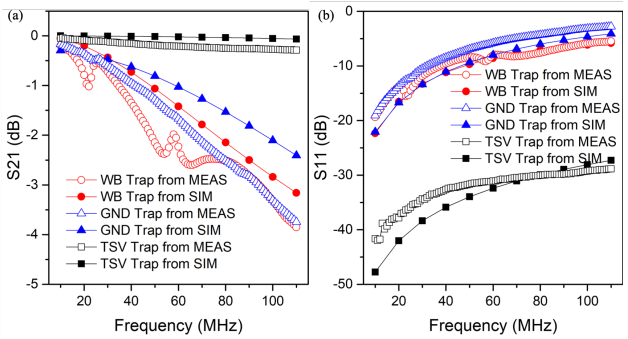

Fig. 4. The comparison of (a) insertion loss and (b) reflection loss respectively obtained from measurement and modelling for WB, WB-GND and TSV traps. A decent agreement between measurement and simulation is achieved.

parasitic components elimination of TSV trap. Generally, the high parasitic suffered by traps with large form factor will result in high loss.

At the same time, a finite element modelling of *S*-parameter is conducted. 3D models built in Section II are applied and similar lumped ports setup and RF signal settings are configured as actual measurement. The curves from simulation are plotted together with those from measurement (Fig. 4.), demonstrating a decent agreement. In addition, it is found that the thinning of silicon substrate in TSV trap also benefits RF loss reduction. Based on the simulation result, the insertion and reflection loss can be respectively reduced by 2 and 8 dB at a frequency of 60 MHz when the silicon thickness is reduced from 700 (WB/WB-GND trap substrate thickness) to 100 μm (TSV trap substrate thickness).

V. Resonance Test and Simulation

For stable and flexible RF and DC feedthrough, ion traps are assembled into a ceramic pin grid array (CPGA) package before inserted to the ion trapping vacuum chamber. Glass spacers (with height of ~500 μm) are placed underneath to raise the trap above CPGA surface for optical addressing. Bonding wires are required to connect surface electrode (WB/WB-GND trap) or RDL on the interposer (TSV trap) with bonding fingers of CPGA. Thin-layer capacitors of ~820 pF are introduced between DC electrodes and ground to filter out the high-frequency RF coupling onto DC electrodes (Fig. 3(d-f)). In ion trapping operation, an external resonance circuit consists of resistors, toroidal inductors, and capacitors (RLC) is connected with packaged ion trap to step up the RF voltage [19]. A

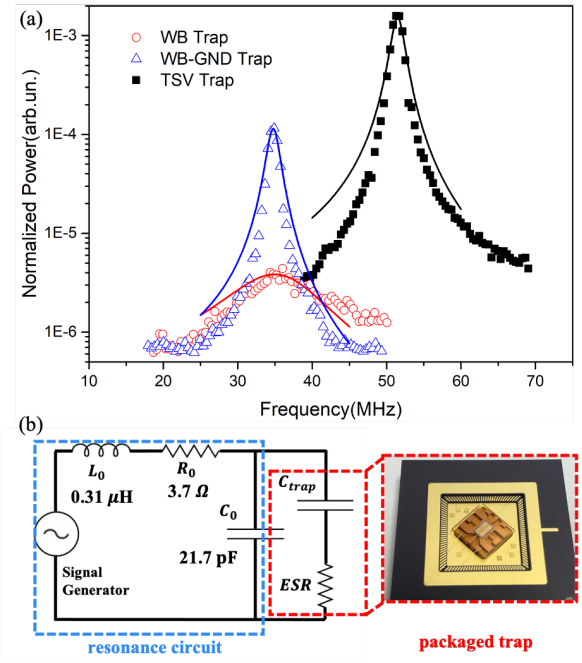

Fig. 5. (a) Resonance and fitting curves of WB, WB-GND and TSV traps connected with resonance circuit. (b) Lumped circuit model of resonance circuit connected with ion traps. The trap is further modelled as a capacitor connected with an equivalent series resistor.

TABLE II
Comparison of Different Ion Traps

Ion Traps	WB Trap	WB-GND Trap	TSV Trap
Resonance frequency (MHz)	35.1	34.8	51.5
Q factor	1.8	16.5	22.4
C_{trap} (pF)	44.7	45.8	9.1
ESR (Ω)	40.0	0.3	5.0
Power loss @ 100V (W) from calculation	38.83	0.30	0.43
Power loss @ 100V (W) from simulation	39.74	1.96	2.85

preliminary resonance test is thus performed to evaluate the RF performance of the ion trap after connecting with the resonance circuit. The corresponding lumped circuit model of the resonance circuit is shown in Fig. 5(b). The values of RLC components are initially determined by connecting the circuit with standard capacitors (wire bonded in CPGA).

After connecting ion traps into the circuit, an RF signal sweeping from 10 to 100 MHz with 1 MHz step is applied. From the obtained curves shown in Fig. 5(a), we found that TSV trap has higher resonance peak, resonance frequency, and *Q* factor as compared to WB traps. The high resonance peak and *Q* factor indicate sufficient voltage gain, which is essential for voltage step up. To provide a quantitative insight into the RF loss of different traps, we further model the ion trap as a capacitor (C_{trap}) connected with an equivalent series resistance (ESR) (Fig. 5(b)). By fitting the resonance curves, the capacitance and ESR of different traps are respectively retrieved and shown in Table II. The power loss (P_{loss}) of ion trap is expressed in equation (1) given by [16, 20]:

$$P_{loss} = \left(C_{trap}\Omega_{RF}V_{RMS}\right)^2(R_s + ESR) \quad (1)$$

where Ω_{RF} is the RF frequency, V_{RMS} is the root-mean-square RF voltage, and R_s is net series resistance of surface electrodes. After inserting corresponding values, the P_{loss} of different traps is thus determined (assuming R_s is much smaller than ESR). The calculated power loss of WB-GND trap and TSV trap is ~100 times smaller than that of WB trap (Table II). The power loss reduction is dominated by the small ESR for WB-GND trap, owing to the complete elimination of the parasitic components in silicon substrate which is effectively shielded from RF signal by the grounding plane [21]. In the TSV trap, however, both small capacitance and ESR play an important role in power loss reduction, of which the ESR is minimized largely due to the smaller dimension and thickness of the silicon substrate itself.

Meanwhile, the RF power losses of different traps are evaluated from the FEM. With similar 3D models, the Joule heating induced by the electric field inside the ion trap can be extracted. In the simulation, we apply RF frequencies based on the results of resonance test (but with same V_{RMS} of 100 V) to corresponding ion traps. The simulated heating powers agree well with those from calculation (Table II). The small deviation between calculation and simulation for TSV and WB-GND

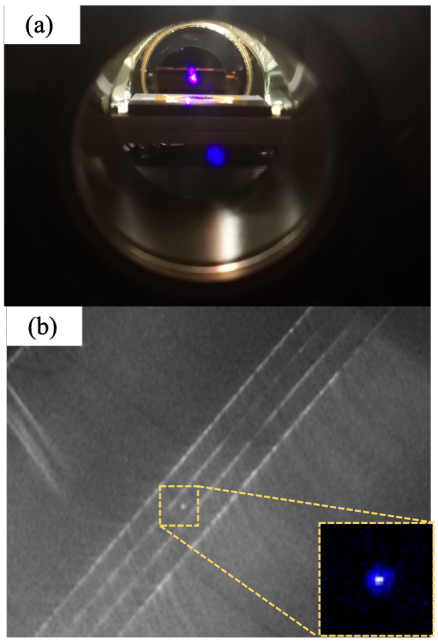

Fig. 6. (a) TSV trap in the vacuum chamber. Laser beams are above the trap surface and focusing the trapping point. (b) Image of $^{88}Sr^{+}$ ion trapped by the TSV trap. The fluorescence shows the outline of TSV trap electrodes geometry.

traps may come from the negligence of R_s in calculation.

VI. Ion Trapping Test

Due to the superior RF performance of TSV trap, ion trapping test is conducted on the TSV trap. Before ion trapping operation, TSV trap is inserted into the vacuum chamber and pre-baked for one week (Fig. 6(a)). The resultant pressure is in the range of 10^{-11} mbar, indicating the excellent ultra-high vacuum (UHV) compatibility of the trap even after the integration of TSV, micro bump and interposer.

The anomalous heating from electric-field noise above electrode surface represents limitations for various trapped-ion based applications [22]. Though the sources of this heating are still not sufficiently clear, the heating rate indeed reflects the performance of a specific ion trap from the trap design, fabrication imperfections to the electrode surface contaminations. In the TSV trap operation, $^{88}Sr^{+}$ ion is trapped at radial frequencies of 2.6 MHz and an axial frequency of 300 kHz. An image of the laser-cooled ion trapped above the surface of TSV trap surface is shown in Fig. 6(b). Using Doppler re-cooling technique [23], the heating rate of the trap is measured of ~250 mK/s, which is dominated by the low-frequency axial mode. This result is well comparable with traps of similar dimensions and operated at room temperature (300 K) [22], suggesting the TSV trap is competent for future quantum logic operations. Meanwhile, it is found that the DC voltages used for electrical field compensation are able to keep stable in a week basis. The lifetime of single $^{88}Sr^{+}$ ion (with laser cooling) is of the order of 30 minutes, which is compatible with the vacuum level [24].

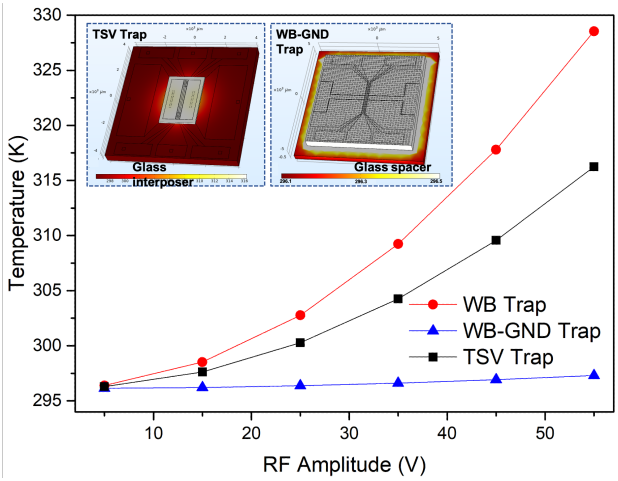

Fig. 7. Temperature change comparison of different ion traps with the increase of RF signal amplitude. Inset: Temperature distribution pattern of TSV trap and WB-GND trap at 55 V. The small contact area of micro bumps and poor thermal conductivity result in heat concentration at TSV trap.

VII. Heating Dissipation Discussion and Further Improvement

In the ion trapping test, a slight vacuum level decline is found (in the level of several 10^{-11} mbar) when the RF amplitude is higher than 85 V. We attribute this decline to the high temperature of TSV trap. Even though TSV trap has a low power loss, the poor heating dissipation may still result in the high temperature as similarly suffered by conventional 3D integrated circuits [25].

Note the heat dissipation mechanism of ion trap is dominated by the thermal conduction, while the effect from thermal convection is negligible since ion trap is operated at an UHV environment. Currently, the produced Joule heat is transferred from TSV die to the CPGA surface (assuming it has a constant room temperature) through micro bump and glass interposer. Due to the small contact area of micro bump as well as the poor thermal conductivity of glass, heat is concentrated at the TSV die and cannot be dissipated efficiently, resulting in a high temperature of TSV die.

These speculations are confirmed by the simulation. WB trap has the highest temperature increase due to its high power loss (Fig. 7.). In contrast, WB-GND trap has a low and uniform temperature distribution due to the low power loss and relatively large contact area between silicon substrate and spacer underneath (inset of Fig. 7.). On the other hand, the temperature of TSV die increases by ~20 K at an RF amplitude of 50 V whereas the glass interposer underneath is able to maintain its initial temperature (room temperature), though the power loss of TSV trap is sufficiently low. To minimize the TSV trap temperature, an adequate heating conduction path is thus required. First, dummy bumps or heat sink materials can be placed between TSV die and interposer to increase the contact area. Second, the glass substrate for interposer can be replaced by materials that have similar electrical properties but much higher thermal conductivity (e.g., sapphire and silicon with ultra-high resistivity) as compared to glass.

In addition, we want to highlight that TSV is not in contradiction with the implementation of ground plane [26]. Similar as the mesh pattern adopted in current grounding plane design of WB-GND trap, openings can be made onto grounding plane to allow TSV go through. The combination of TSV and

grounding plane will further reduce the RF loss and minimize the temperature increase. Based on simulation result, a TSV trap with grounding plane is able to maintain the temperature increase below 1 K at an RF amplitude up to 200 V.

VIII. Conclusion

To minimize RF loss of ion trap on silicon substrate, we demonstrate a TSV integrated ion trap, which has reduced form factor and parasitic due to the elimination of wire bonding pads. We benchmark the RF performance of TSV trap with original WB trap as well as WB-GND trap which has same geometry as WB trap but with additional grounding plane. The fabrications of three different traps are all performed with CMOS back-end techniques on 12-inch wafer platform. The resulting *S*-parameter measurement shows that TSV trap has extremely low on-chip loss (0.2 dB at 50 MHz) as compared to WB counterparts (up to 2 dB). Besides, based on the post-packaging resonance test results, TSV trap enable a significant power loss reduction (from 38 to less than 1 W). Also, the higher *Q* factor (~22) of TSV trap makes it more favorable in terms of RF voltage step up. A finite element modelling with 3D models of different ion traps is used for electric field visualization and analysis. The extracted *S*-parameter, RF loss power and temperature from the modelling are in decent agreement with those from measurement. The TSV trap has a comparable performance to room-temperature traps of similar dimensions regarding heating rate, ion lifetime and stability. The combination of TSV and grounding plane is proposed for future ion trap design.

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