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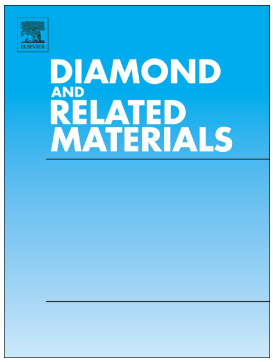

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Non-volatile tuning of normally-on and off states of deep depletion ZrO_2/O-terminated high voltage diamond MOSFET

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Abstract

Based on the stability of the deep depletion regime in diamond and the outstanding properties of this promising material for its use in power devices, p-channel deep depletion metal oxide semiconductor field effect transistors were fabricated on a (001) Ib nitrogen-doped high pressure high temperature diamond substrate. Taking advantage of the new concept of the non-volatile diamond-based photo switch, it is demonstrated that it is possible to tune the normally-on and normally-off states of the transistor by configuring the pn-junction space charge region. The devices under study was designed following an interdigital-like and a circular-like architectures presenting low threshold voltages (between 3 V and -3 V), an on/off ratio of 10^7 and a critical electric field numerically assessed of 9 $MV.cm^{-1}$ at room temperature. This new degree of freedom opens the route for diamond based power electronics.

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1. Introduction

The next step of the development of power electronics goes through the Ultra Wide Bandgap Semiconductors (UWBGS) because the bandgap is correlated with many of the figures-of-merit and because the performance increases non-linearly with it. Particularly, BFoM is related to the cubic of the critical electric field, itself related to the energy bandgap. The relationship between them is a power law dependence whose refinement is discussed in a recent study by Slobodyan *et al* [1]. The increase of the breakdown voltage promotes the UWBGS superior performance and breakdown voltage is directly related to the critical electric field. All leading then to an improvement in the specific on-resistance and breakdown voltage trade-off. Among these materials, the focus for about two decades has been on AlGaN/AlN or Ga_2O_3, which have been intensively studied for n-channel FETs operation. However, p-channel FETs are far to reach the performance from the n-channel ones due to the low hole mobility. In this line, and in addition to other properties such as the high breakdown field (> 10 $MV.cm^{-1}$) and the high thermal conductivity (> 2.200 $W.m^{-1}K^{-1}$) makes diamond [2, 3, 4] the most complete and promising material for its use in power electronics. A recent study on diamond based p-channel wide-bandgap FETs [5] shows a normally-off p-channel transistor using Hydrogen-terminated diamond surface and h-BN as the gate insulator, exhibiting a room temperature mobility of 680 $cm^2.V^{-1}s^{-1}$ following a promising direction for the development of wide-bandgap complementary circuits.

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Moreover, efforts have been done by different groups working on diamond MOSFETs to tune the threshold voltage and control the normally-on, normally-off states. In particular, low threshold voltages between -2 V and -4 V have been achieved using an inversion channel MOSFET OH-terminated [6] or two 2D-Hole MOSFETs partially oxidized [7, 8] (normally-on devices that can be tuned as normally-off).

This work presents an alternative p-channel device: a MOSFET based on O-terminated p-type diamond working in the deep depletion regime [9, 10, 11, 12] combined with a non volatile junction field effect transistor (JFET), the N-doped diamond substrate will be used as the gate of the latter. On one hand, the MOSFET, using ZrO_2 as the gate dielectric, can be electrically controlled no matter the light exposure and works in the deep depletion regimen similarly to those previously reported using Al_2O_3 as the gate oxide. On the other hand, it is well known that n-type doped diamond shows deep donor levels from the conduction band, in particular Nitrogen creates donor levels at 1.7 eV and Phosphorus at 0.58 eV. As a result, at room temperature, electrons remain bounded to the dopants and they cannot be electrically controlled, keeping the diamond layer insulating. Instead of raising temperature to activate the dopants, an alternative way to promote some of those bound electrons to the conduction band is achieved by external illumination. In this case, this promotion leading to an increase of the free carrier concentration is achievable by photon absorption. Hence, with a combination of optical and electrical signals, it is possible to control the pn-junction on/off states in a non-volatile manner. Once the light is removed, the JFET gate cannot be electrically driven anymore until a new light exposure so the system can only be electrically driven by the MOSFET.

The proof of concept of the non-volatility of a diamond pn-junction used as a photo-switch was recently published and described by Masante *et al.* [13]. In such a work, it can be found

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experimental evidence of the non-volatile character of the optically activated JFET in a sequence replicated several times to ensure the reliability. The junction with a Nitrogen-doped n-type diamond is only able to commute under an optical signal since no electrostatic modulation can occur in the dark.

The present work proposes an original way of application: we demonstrate that zirconia can be used as gate dielectric in a D3MOSFET and that V_{TH} can be tuned by controlling optically and electrically the back junction FET. This latter paves the way to the implementation of this kind of devices in circuits without the need of having complementary channel transistors. Also the device can reach a critical electric field of 9 MV.cm^{-1} located at the pn-junction showing that the mechanism of breakdown is independent of the transistor back junction-FET configuration.

2. Fabrication

The sample structure is a stack consisting of a Ib nitrogen-doped high pressure high temperature (001) diamond substrate with a p-type diamond layer on top. From the CV measurement, it has been deduced for this top layer a net doping concentration of 9.2×10^{15} cm^{-1}. The extracted free hole concentration is estimated to be 4×10^{13} cm^{-3} assuming a compensation of 10% [14].

Figure 1: Top view, cross-section and parameters of the transistors under study: a) Interdigital-like D3MOSFET (channel length, L=30 μm and channel width, W=4.2 mm). b) Circular-like D3MOSFETs: T1, T3 sharing same channel parameters (channel length, L=30 μm and channel width, W=0.75 mm); T2 with larger channel width and channel length (channel length, L=50 μm

and channel width, W=0.82 mm).

A selectively localized heavily doped p-type diamond layer was deposited on the p layer to create ohmic contacts (p+, doping concentration of the order of 10^{21} cm^{-3}). Both p-type diamond layers were grown using a microwave plasma assisted chemical vapor deposition (MPCVD) technique. The oxygen terminated p-doped diamond surface was achieved through a vacuum ultraviolet ozone treatment [15].

Fig.1 shows a schematic of the transistors design exhibiting both the top view and the cross-section of the geometries and parameters for an interdigital-like architecture (Fig.1a)) and a circular-like one (Fig.1b)). The purpose of this study is not focus on the on-state performance but the demonstration of the tunability of a device's normally-on/off behaviour thanks to the non-volatility of diamond used as a photo switch. In spite of that, the interdigital-like geometry was used in order to test new design to increase the total current by enlarging the channel width and optimizing the footprint surface of the whole device.

The sample was covered with a couple of layers of Ti/Ni (5/300 nm-thick) using the electron beam (ebeam) evaporation technique in order to, after the application of an O_2 plasma, mesa-etch the sample approximately 1 μm and avoid a short-circuited transistor. To achieve the ohmic contacts and before the gate oxide deposition, we made use of the selective metallic p+ layer on which a stack of Ti/Pt/Au (with 30/30/30 nm-thick metallic layers) were fabricated by laser lithography (Heidelberg DWL66FS) and ebeam evaporation to finally apply a standard lift-off technique.

The gate dielectric was deposited by atomic layer deposition (ALD) using a Savannah 100 deposition system from Cambridge NanoTech. The ZrO_2 was grown using a precursor of tetrakis

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dimethylamido zirconium IV and water vapor as the oxidant alternating N_2 purges. Pulse and exposure times in ALD process were 15 ms and 7 s, alternatively, during 700 cycles, typical base pressure was of the order of 10^{-1} Torr and temperature for deposition was 400 ºC.

Other two contacts were fabricated: one of them on the top of the oxide to form the MOS-gate contact, fabricated by laser lithography and ebeam evaporation with same metallic stack and thickness as for the ohmic ones. The other contact, on the back, were added by directly applying Silver paste. Finally, the electrical measurements were performed by a Keithley Source Measure Units two channel 2612B and one channel 2410 models.

3. Concept & Experimental setup

The principle of this hybrid device, as mentioned earlier and shown in Fig.2, is based on two properties of diamond: on the one hand, the use of the pn junction as an additional gate to control the space charge region (SCR) extension from the junction since N-donors in the diamond substrate can be activated by visible light (a polychromatic white LED with an optical power density of 11 mW.cm^{-2}). Hence, thanks to a fourth electrode (back electrode on the substrate), the pn-junction SCR could be configured by applying a potential difference between the Ib N-doped HPHT substrate and the source under light and then freezing the configuration by removing the light. The Ib type N-doped substrate is insulating under any external energy source because the dopants are deep donors with a high activation energy of the order of 1.7 eV. When the light is switched on, the photon absorption allows some of the bound electrons to be promoted to the conduction band and then the junction can be electrically driven to enlarge or reduce the potential barrier between the p and n sides (corresponding to reverse or forward biasing the junction). After the light being removed, recombination processes of carriers take place which recover the

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insulating property of the N-doped diamond substrate and so the electro-optically imposed potential barrier between the two sides of the junction remains fixed.

Figure 2: Working principle: gates control of the SCR (in purple) in a 600 nm-thick p-type diamond layer, to modulate the channel on/off states. a) SCR extensions when the back gate has been connected to ground under a light source and after removing the illumination, the MOS gate is connected to ground. b) Normally-on: the substrate has been biased at -5 V under a light source and after removing the illumination, the MOS is biased at V_{GS}=0 V (left) and V_{GS}=-1 V (right). c) Normally-off: the substrate has been biased at -3 V under a light source and after removing the illumination, the MOS is biased at V_{GS}=0 V (left) and V_{GS}=-1 V (right).

On the other hand, the stability of the deep depletion regime is complimentarily used to control the on/off states by biasing the MOS gate to open/close the channel. The metallic contacts distribution is shown in Fig.1 cross section.

Fig.2 presents how the SCR is extended below the gate and above the pn junction depending on the applied bias on the gate and the back, respectively. The SCR below the MOS gate is deduced from experimental CV curve. The JFET SCR extension, h, has been calculated at the pn junction interface following the equations:

$$V_{bi} = \frac{k_B T}{q} ln(\frac{N_a N_d}{n_i^2}) \quad (1)$$

$$h = \sqrt{\frac{2\varepsilon_s \varepsilon_0 (V_{bi} + V_{BS})}{qN_a}} \quad (2)$$

From Eq.1 and Eq.2 V_{bi} is the built-in potential, k_B the Boltzmann constant, T the temperature, q the elementary electric charge, N_a and N_d the B and N-doping concentrations, n_i the intrinsic

carrier concentration, h is the junction SCR extension, ε_s and ε_0 are the relative dielectric constant of diamond and the vacuum permittivity, respectively and V_{BS} the bias applied on the back contact relative to the source electrode on the front side.

The experimental setup requires then four electrodes to operate: two for the ohmic contacts (source and drain), one gate contact to control the diamond deep depletion MOSFET (D3MOSFET) and one gate contact on the back which in combination with a light source will allow the control of the junction field effect transistor (JFET). All the measurements were taken under vacuum (typically with a pressure of 10^{-4}-10^{-3} Torr) and at room temperature.

Firstly, the connections were made between the following electrodes: the one on the back contact on which a bias is applied to the substrate, and two on the source and drain connected to the ground keeping the MOS gate floating. So, we apply a bias on the back under light exposure during 10min for stabilization to later remove the light to freeze the system in a certain back side SCR extension configuration dependent on the bias applied to the pn junction waiting another 10min. After that, the electrode on the back contact is removed and the pn-junction system remains frozen. The non-optimization of the N-doped substrate acting as a photo-switch leads to a long commutation time, the 10 minutes holding time is safety precautions to be 100% sure that the device is in steady sate and to maintain reproducible states. Times of commutation of few ms have been achieved as a combination of optical wavelength and power density, temperature, doping and geometry. These results have been recently reported at a conference[16]. Further optimization and improvements in n-type back gate layers can even reduce this time constant to be more compatible with applications.

Then, in order to control the D3MOSFET we connect: the source to ground and the MOS gate and the drain to two voltage sources keeping the back floating. At this point, a quasi-static

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potential difference between drain and source is established for different MOS gate voltages to get the current-voltage characteristics.

The process is repeated according to the different configurations we can set up using the JFET: from a completely suppressed SCR caused by the forward biasing of the junction (V_{BS}=-20 V) or intermediate configurations (-20 V < V_{BS} < -3 V) resulting in a normally-on D3MOSFET, passing through the case where the depletion due to the MOS structure and the one caused by the junction meet (-3 V ≤ V_{BS} < 9 V, normally-off D3MOSFET), to finally the also normally-off case where the p-type diamond layer is fully depleted from the pn junction (V_{BS} ≥ 9V), in this later situation the channel is permanently closed and it is no longer possible to control it with the MOS gate.

4. Current density versus Voltage Characteristics

As discussed in Sec.3, the bias applied to the substrate affects the D3MOSFET behaviour from normally-on to normally-off. Typical current density as a function of drain bias for the interdigit can be found in Fig.3: from the normally-on in Fig.3a) in which the transition of the on/off states is given by a V_{GS}=3 V, followed by the off/on states in Fig.3b) in the normally-off configuration (the channel is closed at V_{GS} ≥ 0 V). The on/off ratio is 10^7.

Figure 3: Interdigital-like D3MOSFET current density characteristics as a function of drain bias for different configurations of the pn junction space charge region at room temperature: a) V_{BS}=-20 V, Normally-on starting condition. b) V_{BS}=-3 V, Normally-off starting condition. c) Transfer characteristics of a combination of a diamond D3MOSFET with a non volatile diamond JFET at room temperature showing the shift in threshold voltage and the change from normally-on to

normally-off behaviour.

A maximum saturation current density of the order of tens of μA is reached where the SCR due to the N-doped diamond substrate is completely suppressed in the p-layer with a maximum value of leakage current of tens of nA. As we extend the SCR through the p-layer from the junction, the saturation current decreases. The different transfer characteristics as a function of the bias applied to the substrate is evidence of the change in the D3MOSFET's normally-on/off behaviour as it is plotted in Fig.3c).

The geometry of the interdigital-like D3MOSFET was thought to increase the total current. Unfortunately, the results are lower than expected for large channel widths (a comparison of the total current achieved by the different transistors is available in Appendix A). The choice of the interdigit transfer characteristics was made base on the intention to show in a clearer way the threshold voltage shift.

5. Breakdown voltage and critical electric field evaluation

Similarly to how the IV characteristics were performed, the blocking capabilities has been tested by configuring optically and electrically the back pn junction to extend/remove the SCR in a desired configuration, then the illumination is removed and the back contact remains floating. Immediately after, the D3MOSFET is electrically driven to reach the off-state. Fig.4a) shows the different values for the breakdown voltage reached by T1, T2 and T3 D3MOSFETs at room temperature (T1, T2 and T3 are presented in Fig.1). T1 and T3 share the same channel parameters: they were tested in two different configurations of the pn junction SCR, T1 when the V_{BS} is set to reach the JFET off-state and the p-type layer is fully depleted (V_{BS}=5 V, JFET pn junction biased

in reverse regime) and T3 when the SCR due to the pn junction is fully removed (V_{BS}=-20 V, JFET pn junction biased in forward regime) and the SCR due to the MOS gate closes the channel. From the experimental results, it seems that the on/off behaviour configured by the JFET does not affect the blocking capability performance since similar transistors in different configurations present similar breakdown voltage. In turn, T2 presents a higher breakdown voltage as expected since the distance source-drain in this case is larger. Transistor T3 was damaged and rendered unusable after forcing the transistor to withstand high voltages, however the transistors so-called T1 and T2 were protected with a resistance in series and we found that the breakdown mechanism is nondestructive and the measure is repeatable and reliable.

Figure 4: a) Blocking capabilities tested at room temperature for circular-like transistors T1, T2, T3 configuring the pn-juntion space charge region for normally-on (T2,T3) and normally-off (T1) biasing the MOSFET in the off-state. The high voltage measurement were perform in a keithley SMU 2410 model whose limit of detection is $10^{-5}\mu$A. b) On the left, the Y-component electric field profile for a normally-on (blue) and a normally-off (orange) configuration using a circular-like MOSFET in the off-state with channel length L=50 μm and channel width W=0.8 mm. On the right, the cut line (in white) location from which the profile has been extracted. c) the corresponding electric field distribution maps for the the Y-component when normally-on off-state configuration (on the left) and normally-off off-state configuration (on the right).

Figure 5: Finite element calculation for the X-component of the electric field: a) On the left, the X-component electric field profile for a normally-on (blue) and a normally-off (orange) configuration using a circular-like MOSFET in the off-state with channel length L=50 μm and

channel width W=0.8 mm. On the right, the cut line (in white) location from which the profile has been extracted. b) the corresponding electric field distribution maps for the the X-component when normally-on off-state configuration (on the left) and normally-off off-state configuration (on the right).

Finite element calculation was used to evaluate the electric field in order to understand the breakdown mechanisms. The following parameters were introduced in the simulation for a circular-like device with a channel width of W=0.8mm and a channel length of L=50 μm (corresponding to T2): 600 nm-thick p-type diamond layer with a doping concentration of $N_a=10^{16}$ cm^{-3} and 10% compensation; 400 nm-thick N-doped substrate with a doping concentration of $N_d=10^{18}$ cm^{-3} and 70 nm-thick oxide with an oxide-diamond interface charges density of $Q_f=1.5\times10^{12}$ cm^{-2} based of previous studies on MOS capacitors [17]. Fig.4c) shows the calculation of the electric field distribution for the Y-component when the D3MOSFET is normally-on biased in off-state (Fig.4c) left map) and normally-off biased in off-state (Fig.4c) right map) by applying a potential difference between the source and the back contact under illumination and then, after removing the light source biasing the D3MOSFET to reach the off-state by applying a potential difference between the source and the gate. Through the evaluation of the electric field profile for its Y-component (Fig.4b) left), it can be observed there is no difference between normally-on and off behaviour and we found a critical electric field at the junction between 8.9 $MV.cm^{-1}$ (normally-on off-state) - 9.1 $MV.cm^{-1}$ (normally-off off-state) at V_{DS}=-650 V. Fig.5b) shows the calculation of the electric field distribution for the X-component when the D3MOSFET is normally-on biased in off-state (Fig.5b) left map) and normally-off biased in off-state (Fig.5b) right map) by applying a potential difference between the source and the back contact under

illumination and then, after removing the light source, biasing the D3MOSFET to reach the off-state by applying a potential difference between the source and the gate. Through the evaluation of the electric field profile for its X-component (Fig.5a) left), it can be observed a low electric field up to 0.24 MV.cm^{-1} at V_{DS}=-650 V.

The electric field distribution was evaluated using the circular-like T2 D3MOSFET since it has larger source-to-drain length and consequently the largest breakdown voltage. A proper evaluation of the high voltage withstand capability of the interdigital-like D3MOSFET could not be performed. The total area of interdigit is larger than the circular-like ones and so more likely to have killer defects which can affect the blocking capabilities and can lead to smaller breakdown voltage than those obtained for a small finger or circular unique gate. However, in absence of defects, interdigit should achieve similar value of breakdown to those reached by T1 and T3 as they share the source-to-drain length.

If one manage to get a low (vertical) leakage, the pn-junction will generate most of the potential gradient (electric field). As a consequence, it is evidenced (see Fig.5) that the MOS region only has a low electric field. The mechanism is nondestructive, so the transistor is capable of recovering after a while and the measurements become repeatable.

An optimization of the diamond epilayers stacks (doping, thickness and architecture) will make possible the association of complementary and efficient diamond FETs improving the on-state performance as well as the blocking capabilities. The details for future improvements in terms of current density are recently described in detail by Masante *et al*. [12]. Regarding the space-charge effects, the drain-source voltage sweep has no effect on the back gate SCR extension. The main advantage of the non-volatility of the diamond photo-switch used here for the control of the threshold voltage is that the back gate cannot electrically drive the junction during the

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MOSFET operation (no illumination).

6. Conclusion

The present study demonstrates that a combination of diamond lateral MOSFET and JFET with vertical pn gate junction can be used to tune the normally-on/off behaviour of the device controlling the threshold voltage (keeping it low with values in the range between -3 V and 3 V).

In addition, the double-gate transistor showed a nondestructive breakdown mechanism, reaching a critical electric field of 9 $MV.cm^{-1}$, this is a high electric field value, close to the theoretical vertical breakdown expected at around 10 $MV.cm^{-1}$ (but still subject to discussion). Such a breakdown occurs at the vertical pn-junction and it is independent of its SCR configuration (electrically controlled under illumination). No electric field crowding effect was observed in the vicinity of the zirconia.

This hybrid device paves the way to a potential application in complex circuits and also answers to the safety requirements of normally-off state for power electronics.

Declaration of interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability statement

The data that support the findings of this study are available from the corresponding author

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upon reasonable request.

Authors contribution

B. Soto: Conceptualization, Methodology, Data curation, Formal analysis, Writing original draft. **M. Couret:** Finite element calculation. **J. Cañas:** Conceptualization. **A. Castelan:** Finite element calculation. **N. Rouger:** Conceptualization, Resources, Writing review & editing. **D. Araujo:** Resources, Supervision, Formal analysis, Writing review & editing, Funding acquisition, Project administration. **M.P. Villar:** Resources, Supervision, Formal analysis, Writing review & editing, Funding acquisition, Project administration. **J. Pernot:** Conceptualization, Resources, Supervision, Formal analysis, Writing review & editing.

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Appendix A. Transfer characteristics: evaluation on the different D3MOSFETs

As it was mentioned above, the interdigital-like D3MOSFET was designed to have larger channel width with respect to the circular-like ones in order to increase the total current. Unfortunately, the total current of the interdigital-like D3MOSFET increases by less than one order of magnitude with respect to the circular shaped transistors, a result lower than expected. Fig.A.6 provides the total current achieved by different transistors used in this work: Fig.A.6a) related to the interdigit and Fig.A.6b) and Fig.A.6c) related to transistors T1 and T2, respectively.

Figure A.6: a) Interdigital-like D3MOSFET with channel width 4.2 mm and source-to-drain length 30 μm: total current as a function of the gate bias for different bias applied to the back substrate. b) Circular-like D3MOSFET T1 with channel width 0.75 mm and source-to-drain length 30 μm: total current as a function of the gate bias for different bias applied to the back substrate. c) Circular-like D3MOSFET T2 with channel width 0.82 mm and source-to-drain length 50 μm: total current as a function of the gate bias for different bias applied to the back substrate.

In all three D3MOSFETs, it is observed that they can operate as normally-on or normally-off depending on the electro-optically induced polarization on the back gate (N-doped substrate). These results support the use of diamond non-volatile photo-switch as a new degree of

freedom in the design and control of p-channel transistors.

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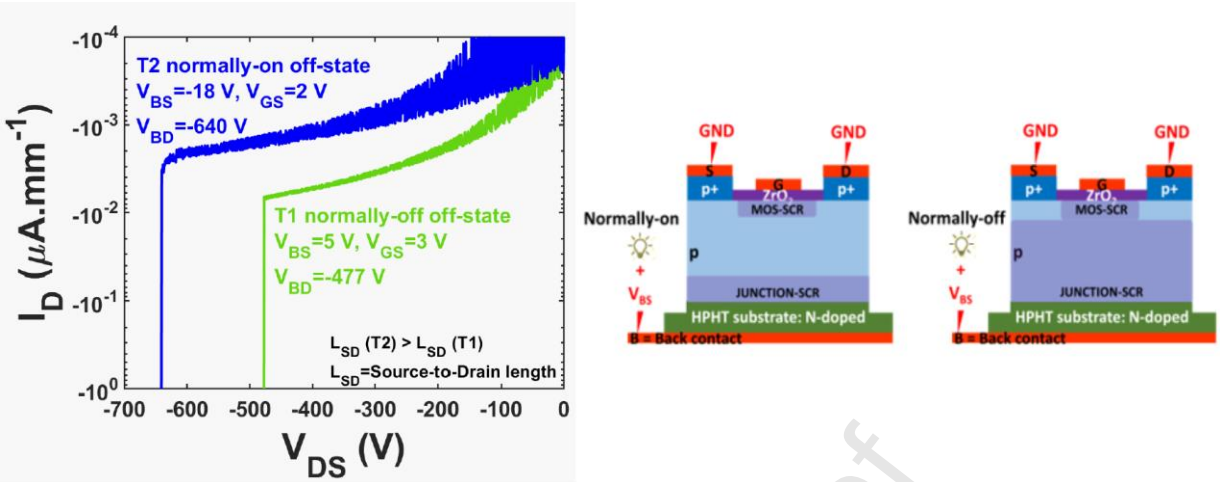

Graphical abstract

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Highlights

- Non-volatile tuning of normally-on/off behavior of an O-terminated diamond-based p-channel MOSFET
- Control of the threshold voltage: from -3 V to 3 V.
- Breakdown voltage: measured up to -640 V.
- Critical electric field evaluation: finite element calculations show a 9 $MV.cm^{-1}$ peak

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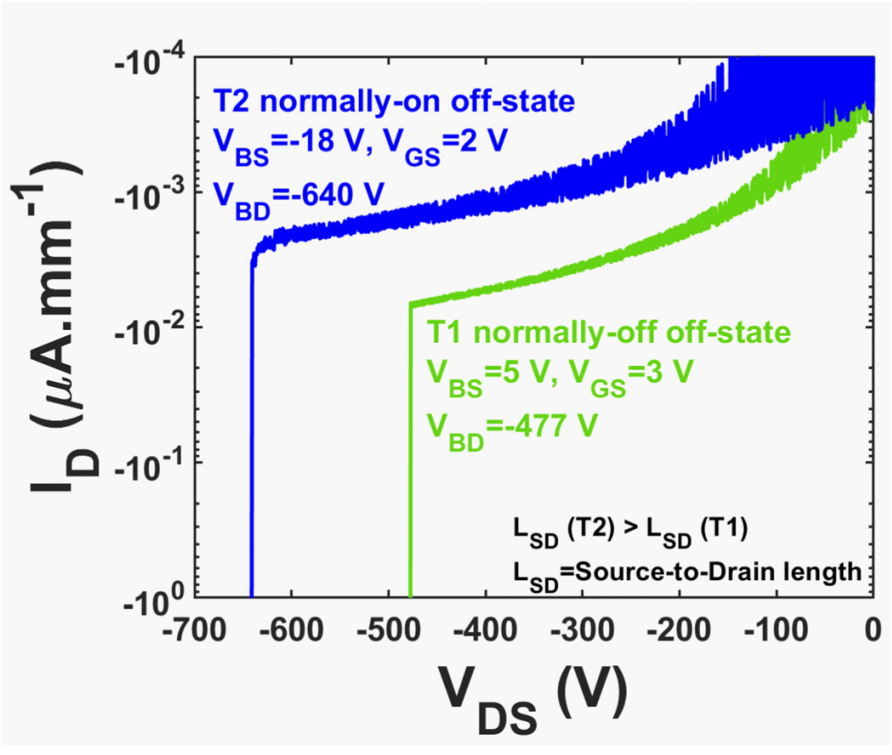

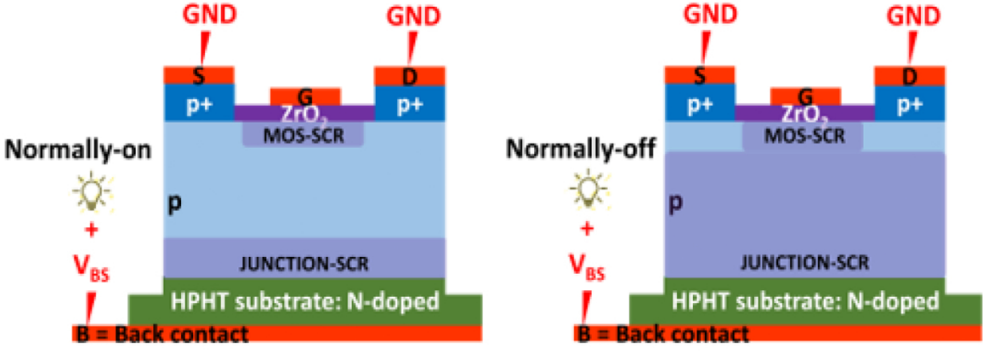

Graphics Abstract

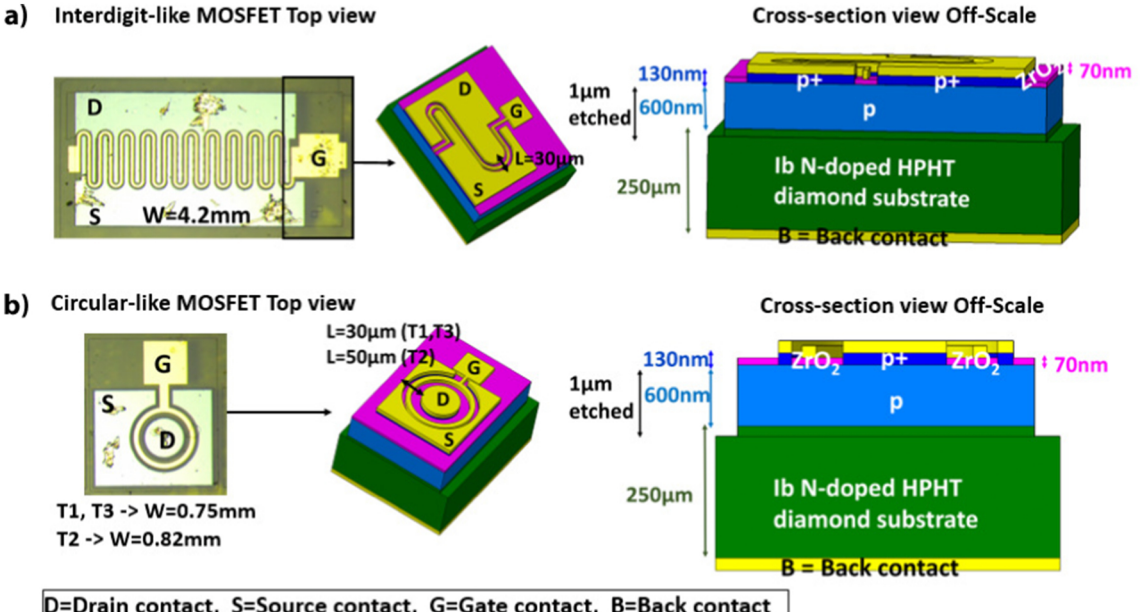
a)
Interdigit-like MOSFET Top view
Cross-section view Off-Scale
D
G
S
W=4.2mm
L=30µm
1µm
etched
130nm
600nm
250µm
p+
p+
p
70nm
Ib N-doped HPHT
diamond substrate
B = Back contact
b)
Circular-like MOSFET Top view
Cross-section view Off-Scale
L=30µm (T1,T3)
L=50µm (T2)
T1, T3 -> W=0.75mm
T2 -> W=0.82mm
1µm
etched
130nm
600nm
250µm
ZrO2
p+
ZrO2
70nm
p
Ib N-doped HPHT
diamond substrate
B = Back contact
D=Drain contact, S=Source contact, G=Gate contact, B=Back contact

Figure 1

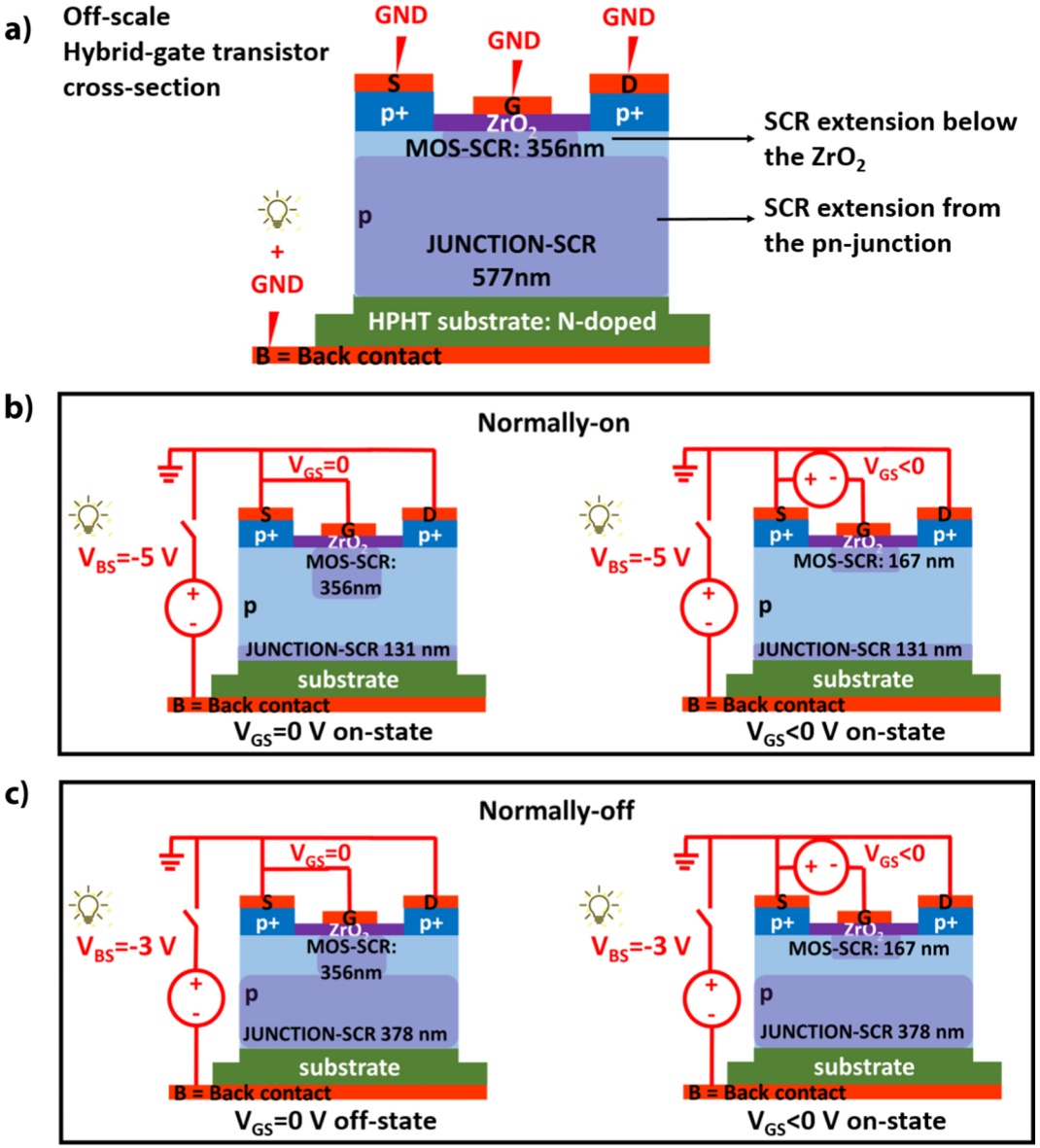
a)
Off-scale
Hybrid-gate transistor
cross-section
GND
GND
GND
S
G
D
p+
ZrO2
p+
MOS-SCR: 356nm
SCR extension below the ZrO2
p
JUNCTION-SCR
577nm
SCR extension from the pn-junction
+
GND
HPHT substrate: N-doped
B = Back contact
b)
Normally-on
VGS=0
VBS=-5 V
MOS-SCR: 356nm
JUNCTION-SCR 131 nm
substrate
B = Back contact
VGS=0 V on-state
VGS<0
VBS=-5 V
MOS-SCR: 167 nm
JUNCTION-SCR 131 nm
substrate
B = Back contact
VGS<0 V on-state
c)
Normally-off
VGS=0
VBS=-3 V
MOS-SCR: 356nm
JUNCTION-SCR 378 nm
substrate
B = Back contact
VGS=0 V off-state
VGS<0
VBS=-3 V
MOS-SCR: 167 nm
JUNCTION-SCR 378 nm
substrate
B = Back contact
VGS<0 V on-state

Figure 2

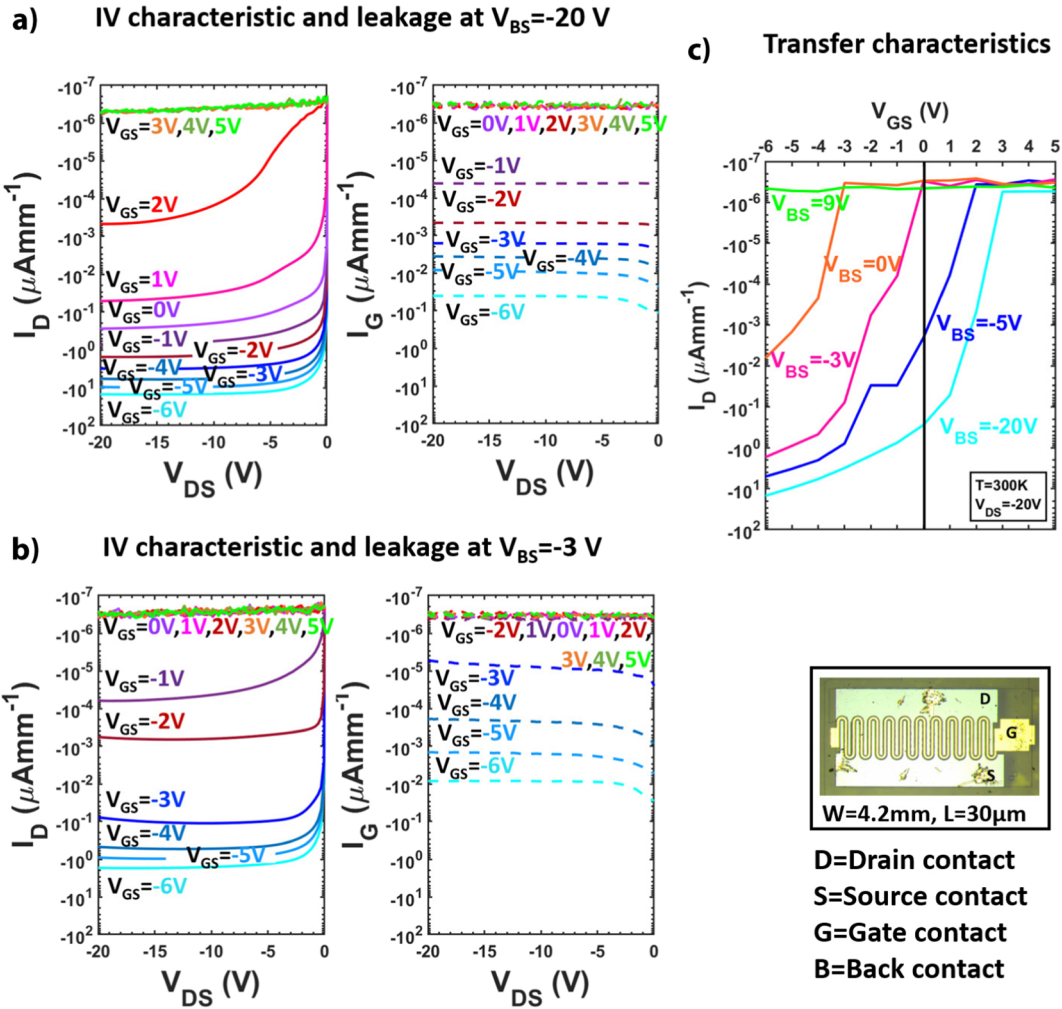
a)
IV characteristic and leakage at V_{BS}=-20 V
V_{GS}=3V,4V,5V
V_{GS}=2V
V_{GS}=1V
V_{GS}=0V
V_{GS}=-1V
V_{GS}=-2V
V_{GS}=-4V
V_{GS}=-3V
V_{GS}=-5V
V_{GS}=-6V
I_D (μAmm^{-1})
V_{DS} (V)
V_{GS}=0V,1V,2V,3V,4V,5V
V_{GS}=-1V
V_{GS}=-2V
V_{GS}=-3V
V_{GS}=-4V
V_{GS}=-5V
V_{GS}=-6V
I_G (μAmm^{-1})
V_{DS} (V)
b)
IV characteristic and leakage at V_{BS}=-3 V
V_{GS}=0V,1V,2V,3V,4V,5V
V_{GS}=-1V
V_{GS}=-2V
V_{GS}=-3V
V_{GS}=-4V
V_{GS}=-5V
V_{GS}=-6V
I_D (μAmm^{-1})
V_{DS} (V)
V_{GS}=-2V,1V,0V,1V,2V,
3V,4V,5V
V_{GS}=-3V
V_{GS}=-4V
V_{GS}=-5V
V_{GS}=-6V
I_G (μAmm^{-1})
V_{DS} (V)
c)
Transfer characteristics
V_{GS} (V)
V_{BS}=9V
V_{BS}=0V
V_{BS}=-3V
V_{BS}=-5V
V_{BS}=-20V
T=300K
V_{DS}=-20V
I_D (μAmm^{-1})
D
G
S
W=4.2mm, L=30µm
D=Drain contact
S=Source contact
G=Gate contact
B=Back contact

Figure 3

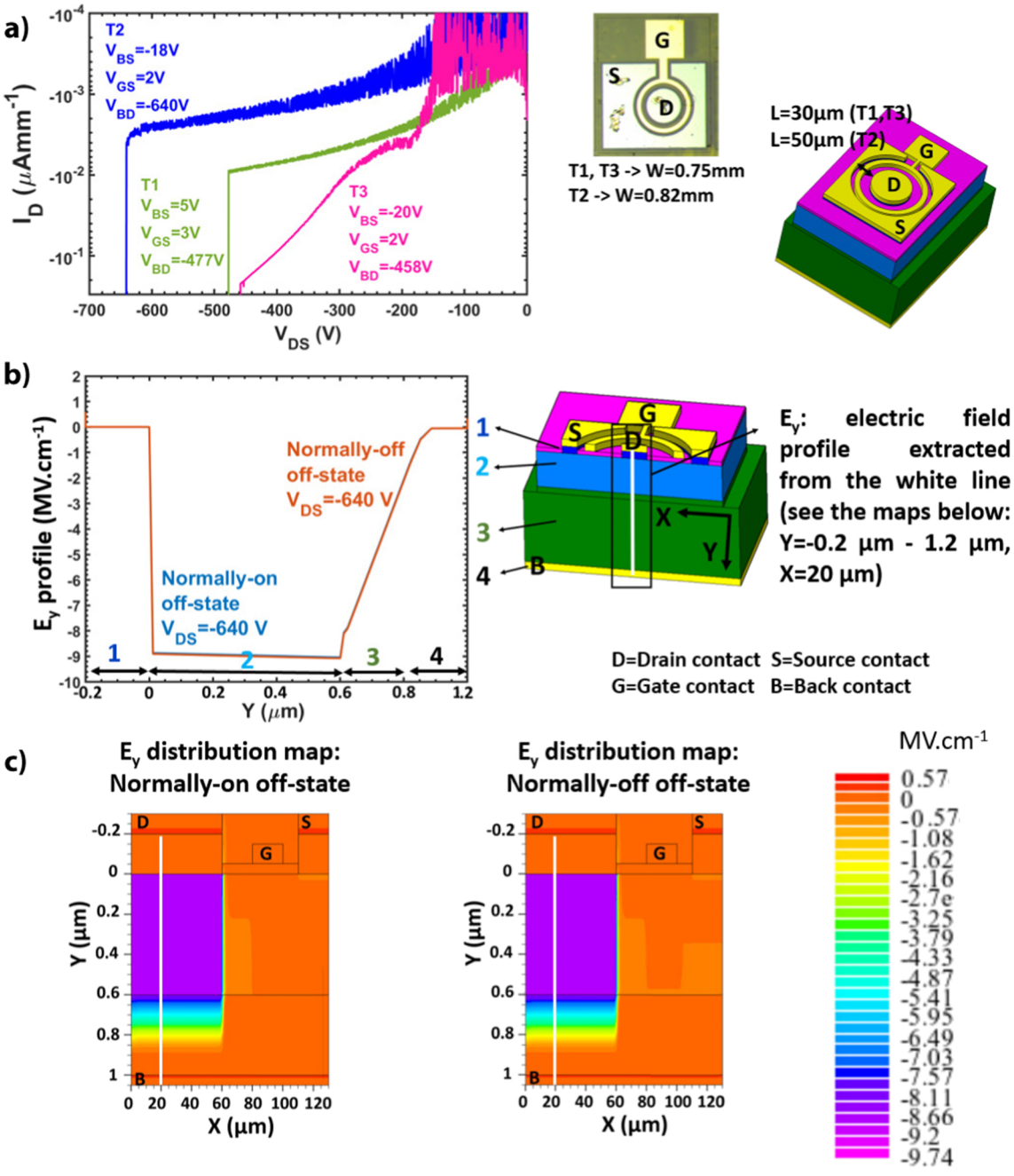
a)
T2
V_{BS}=-18V
V_{GS}=2V
V_{BD}=-640V
T1
V_{BS}=5V
V_{GS}=3V
V_{BD}=-477V
T3
V_{BS}=-20V
V_{GS}=2V
V_{BD}=-458V
I_D (μAmm^{-1})
V_{DS} (V)
G
S
D
T1, T3 -> W=0.75mm
T2 -> W=0.82mm
L=30µm (T1,T3)
L=50µm (T2)
b)
E_y profile (MV.cm^{-1})
Normally-off
off-state
V_{DS}=-640 V
Normally-on
off-state
V_{DS}=-640 V
Y (μm)
1
2
3
4
X
Y
B
E_y: electric field profile extracted from the white line (see the maps below: Y=-0.2 µm - 1.2 µm, X=20 µm)
D=Drain contact S=Source contact
G=Gate contact B=Back contact
c)
E_y distribution map:
Normally-on off-state
E_y distribution map:
Normally-off off-state
Y (µm)
X (µm)
MV.cm^{-1}
0.57
0
-0.57
-1.08
-1.62
-2.16
-2.7e
-3.25
-3.79
-4.33
-4.87
-5.41
-5.95
-6.49
-7.03
-7.57
-8.11
-8.66
-9.2
-9.74

Figure 4

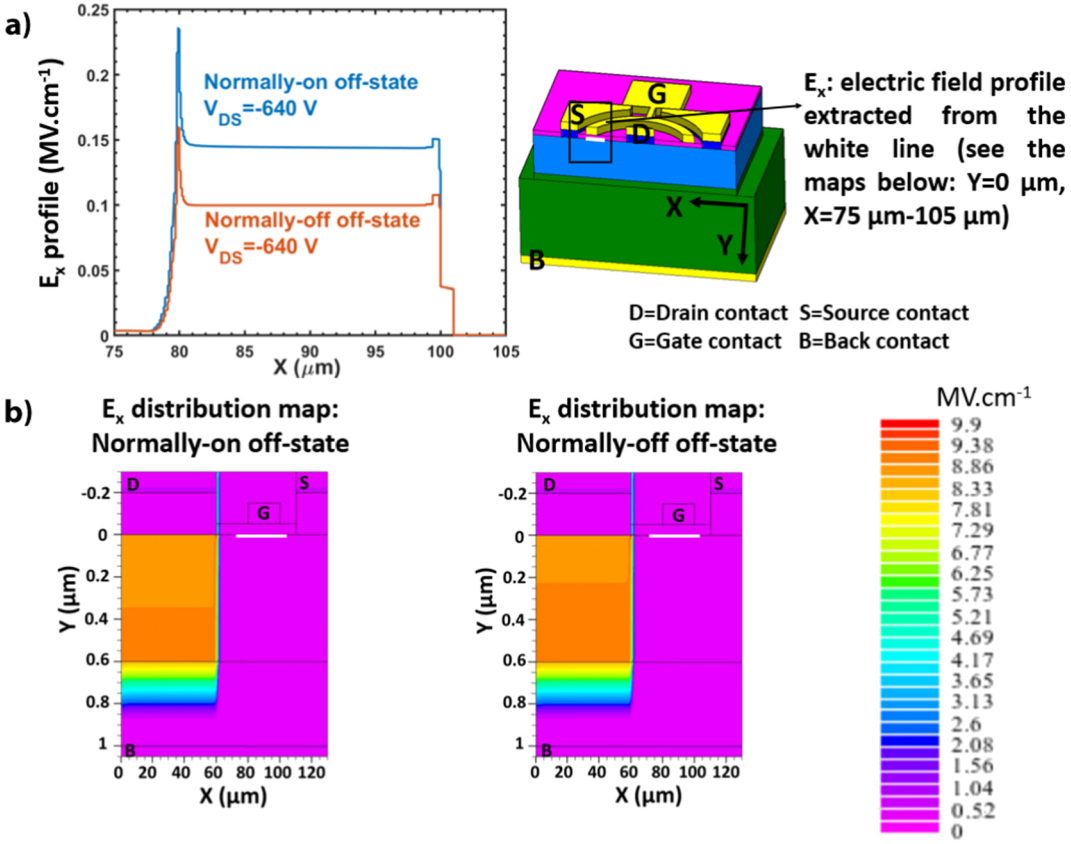
a)
Normally-on off-state
V_{DS}=-640 V
Normally-off off-state
V_{DS}=-640 V
E_x profile (MV.cm^{-1})
X (μm)
G
S
D
X
Y
B
E_x: electric field profile extracted from the white line (see the maps below: Y=0 μm, X=75 μm-105 μm)
D=Drain contact S=Source contact
G=Gate contact B=Back contact
b)
E_x distribution map: Normally-on off-state
E_x distribution map: Normally-off off-state
Y (μm)
X (μm)
MV.cm^{-1}
9.9
9.38
8.86
8.33
7.81
7.29
6.77
6.25
5.73
5.21
4.69
4.17
3.65
3.13
2.6
2.08
1.56
1.04
0.52
0

Figure 5