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Extraction of small signal equivalent circuit for de-embedding of 3D vertical nanowire transistor

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Abstract— In this paper, we present an improved methodology to extract the small signal electrical equivalent circuit of the parasitic elements using RF test-structures for a 3D vertical nanowire transistor technology. The methodology is based on the extraction of parasitic elements from a virtual open structure constructed using electromagnetic simulation and calibrated against on-wafer S-parameter measurements up to 40 GHz. The electrical equivalent circuit of the passive device was then used for de-embedding of the transistor S-parameters for extraction of intrinsic small signal parameters such as the gate capacitances.

Keywords; Test structure; equivalent circuit; parasitic components; RF measurements; de-embedding.

I. INTRODUCTION

In the context of emerging technologies for new computing paradigms such as neural networks, vertical nanowire field effect transistors (VNWFET) are a promising technology owing to their naturally 3D architectures [1]. For the purpose of circuit design for such an 3D emerging technology, it is necessary to build new and accurate compact models to capture the static and dynamic behavior of the device [2]. However, on-wafer test-structures of the devices contain parasitic elements introduced by the RF pads and interconnects necessary to probe the devices under test (DUT). The standard procedure to characterize the parasitic effects of a device at high frequencies can be divided in two parts. Firstly, the measurement system needs to be calibrated so that the reference plane is at the probe tips. This can be done using standard calibration techniques such as SOLT (Short-Open-Load-Thru). At this point all the parasitics associated with the pads and interconnects are still included in the measurements. In the second step, S-parameters of the open and short structures are measured which are then used to remove the parasitic elements external to the DUT, through a subtraction process known as de-embedding [3].

Although the process of parasitic extraction is widely used in technologies targeted for high frequency applications, this process can also be applied for technologies such as the VNWFET that are mainly

designed for computing applications with the purpose of improving the modeling accuracy that normally just relies on DC measurements [1].

In the rest of the paper, results from the RF measurements and electro-magnetic (EM) simulations are used for the extraction of parasitic elements for obtaining the electrical equivalent circuit of an open test-structure. Next, we use this open structure for the de-embedding of the S-parameters of a VNWFET [4].

II. METHODOLOGY

For the purpose of de-embedding, designed open structures were fabricated using the same process and on the same wafer as the VNWFET [4]. The open structure consists of all interconnects except for the vertical nanowires. Fig. 1(a) shows the open structure containing the RF pads, where the absence of the active device can be observed. For the demonstration of the de-embedding process, a VNWFET consisting of 81 nanowires in parallel with a diameter of 17 nm each was selected.

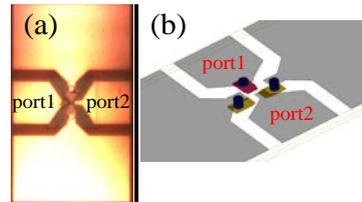


Figure 1. (a) Open structure for S-parameters measurements and (b) a 3-D view of the open structure created in ADS.

A. On-wafer S-parameter measurements

The on-wafer S-parameters were measured using a Vector Network Analyzer (VNA) from Rohde & Schwarz at frequencies up to 40 GHz, and a source monitor unit, Agilent 4142B, connected via a bias-tee. The DUTs were contacted using Ground-Signal-Ground (GSG) probes with a pitch of 100 μm .

B. Electromagnetic simulation

The 3D view of the open structure constructed for EM simulations is shown in Fig. 1(b). The ADS-Momentum

EM simulator was used for the EM simulation and computation of the S-parameters of the provided layout. The layout was imported into ADS using the GDSII file that was used for the fabrication process. The electrical properties of the material layers were then slightly adjusted to fit the measurement results.

C. Equivalent circuit of the transistor interconnections

The proposed electrical equivalent circuit of the parasitic elements can be seen in Fig. 2. Once the EM simulation has been calibrated against the measured S-parameters of the open structure, the values of different elements in the small signal circuit of Fig. 2 are estimated from EM simulations of different sections of the complete structure [3]. The impedance of the source terminal in the return path to ground was considered negligible.

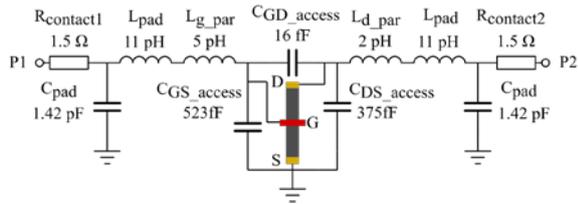


Figure 2. Electrical equivalent circuit representing the parasitic elements obtained from the open test structure.

In Fig. 3, a comparison between the measured and the simulated S-parameter of the open structure is shown. Both the results from EM simulation and the equivalent circuit exhibit very good agreement with the measured data up to 40 GHz, and especially up to 20 GHz.

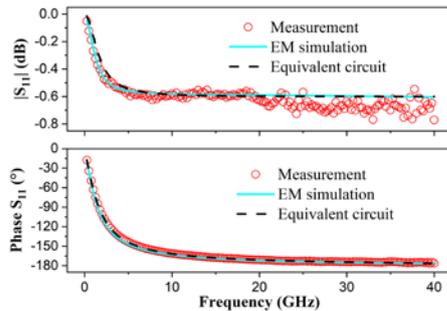


Figure 3. Comparison of S-parameter from measurement and simulations for the open test structure.

D. Transistor's de-embedding method

The de-embedding process used in this work is based on the methodology described in [5]. The ABCD matrix was used to remove the gate and drain parasitic access contributions. The capacitance C_{GD_access} was then removed by subtracting the Y-parameter.

III. DE-EMBEDDING RESULTS

The gate capacitance C_{gd} obtained from the de-embedded S-parameters of the transistor at a V_{GS} of -1 V and a V_{DS} of -0.1 V is presented in Fig. 4, depicting a

relatively flat frequency dependence of the capacitance. The data was truncated at 20 GHz due to the increased noise beyond this frequency.

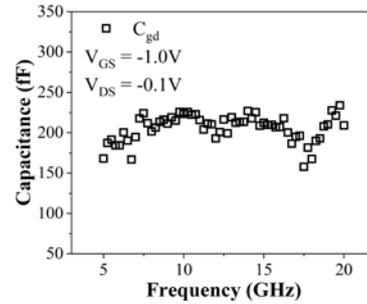


Figure 4. Small signal capacitances of the de-embedded transistor.

IV. CONCLUSION

In this work, the small signal equivalent circuit of the VNWFET's interconnects was achieved by using predictive EM simulation. This distributed model consisting of lumped elements representing the VNWFET's interconnects was then used for the de-embedding of the measurements obtained on the transistor. The extraction of capacitances could be achieved up to 20 GHz, demonstrating the promising efficiency of such a de-embedding procedure. In the future scope of this work, the extracted value of gate capacitances will be verified from 3D TCAD simulation of the transistors.

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