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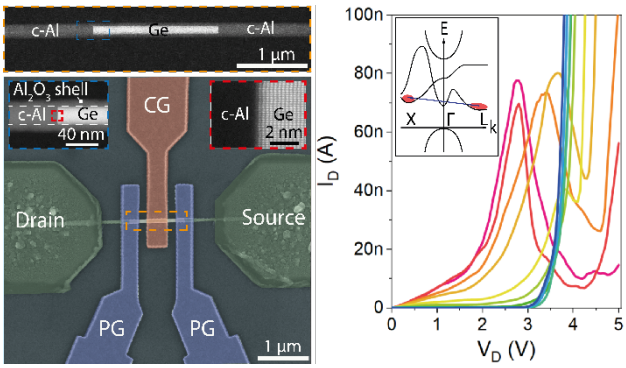
ABSTRACT

The functional diversification and adaptability of the elementary switching units of computational circuits are disruptive approaches for advancing electronics beyond the static capabilities of conventional complementary metal-oxide-semiconductor based architectures. Thereto, in this work the one-dimensional nature of monocrystalline and monolithic Al-Ge based nanowire heterostructures is exploited to deliver charge carrier polarity control and furthermore to enable distinct programmable negative differential resistance at runtime. The fusion of electron- and hole conduction together with negative differential resistance expressivity in a universal



adaptive transistor may enable energy efficient reconfigurable circuits with multi-valued operability that are inherent components of emerging artificial intelligence electronics.

KEYWORDS
germanium, nanowires, heterostructures, adaptive electronics, reconfigurable transistor, negative differential resistance

Alongside with information and communication technologies becoming ubiquitous in everyday life and thus ever more stringent constraints on computing hardware performance, complementary metal-oxide-semiconductor (CMOS) scaling is being pushed towards its physical limits.[1] In this context, the functional diversification of the elementary computing units, the transistors, is an alternative approach to advance computational complexity, enabling a hardware platform that inherently encompasses adaptability in emerging self-learning electronic paradigms.[2,3] To leverage circuit performance beyond the limits encountered in miniaturization, the research field of reconfigurable electronics has explored computational enhancement by extending the functionality of transistors.[4,5] This concept is based on the reconfigurable field-effect transistor (RFET) that fuses both basic switching functions necessary for realizing an energy efficient complementary circuit design by dynamically toggling the device either to *p*-type (hole conduction) or *n*-type (electron conduction) operation through the implementation of a dedicated program gate electrode.[6] Customized logic and physical synthesis routes have been developed for the design of combinational circuits. Benchmarks have shown that the use of runtime reconfiguration *vs*. conventional CMOS can deliver compact circuit topologies *e.g.* in multi-bit adders and arithmetic logic units having a substantial reduction in transistor count, a smaller area footprint and reduced latency length of critical paths.[7,8] Moreover, it has been shown that exclusive OR (XOR) based gates can be

efficiently applied with RFETs[9] allowing for majority based arithmetic operations[10] that have been hindered so far in CMOS.[11,12]

Another concept that has been broadly discussed to overcome the power density limits and increasing signal propagation delays of modern ultra-scaled chip architectures is multi-valued logic (MVL), replacing conventional binary systems by operation schemes with radices or bases higher than two.[13] Hence, implementing an operation scheme with higher performance employing fewer devices and interconnects compared to standard CMOS circuits, owing to higher functionality of MVL circuits can be envisaged.[14] Recently, a MVL concept based on exploiting the monostable-to-multistable[15] nature of serially connected negative differential resistance (NDR) devices was demonstrated, creating a staircase of holding states.[16] An example for a simple yet innovative logic element taking advantage of the NDR characteristic is the monostable-bistable transition logic element (MOBILE), employing two NDR devices connected in series capable to perform both NAND and NOR operations.[15,17] Furthermore, stacking more than two NDR devices, an efficient, and compact signed-digit NDR based MVL adder combining a more than five-fold improvement in circuit propagation delay and a 15 times smaller area compared to common CMOS based circuits has been proposed.[18] Distinct physical methods are currently employed to provide NDR, including resonant tunneling diodes that demand complex semiconductor epitaxial structures, which are difficult to integrate with CMOS.[19] Further, CMOS backend compatible threshold switching in metal/Nb-oxide insulator/metal structures were shown, but exhibit an inherent device-to-device variability in the applied threshold current to inhibit current controlled NDR.[20] As a third concept, the Gunn-effect discovered by J.B. Gunn[21] and C. Hilsum,[22] which is also known as the transferred electron effect in specific semiconductor systems with a multi-valley band-structure delivers voltage controlled NDR. Besides highly strained Si NWs,[23] *n*-type InSb devices[24] and diamond structures,[25] low-dimensional Ge is one of the most promising prospective materials both for the performance enhancement of RFETs and realization of NDR-based MVL through the

transferred electron effect, which is enabled by the acceleration of electrons by sufficiently high electric fields. Thereby electrons are scattered from the energetically favorable low effective mass conduction band valley to an energetically close heavy effective mass valley.[26] Accessible at room-temperature,[27] the NDR characteristic bears enormous potential for the design of MVL regarding performance metrics such as area, speed, or power.[15]

RESULTS/DISCUSSION

Here, we present the NDR-mode RFET concept capable of exhibiting both *p*- and *n*-type FET reconfigurable operability as well as gate-tunable NDR functionality as deterministically programmed by the applied terminal voltages. Thereby, the functionality of the elementary switching units is strongly enhanced, disruptive computational and analog oscillatory circuits. The key enabler for this concept is the electronic structure of the quasi-1D monolithic Al-Ge-Al nanowire (NW) heterostructure, enabling low operation voltages, reconfigurable *p*- and *n*-type polarity and furthermore accessibility to the transferred electron effect at room temperature as required for providing NDR features. Across the discussion of results, the material choice and suitability of our particular heterostructure will become evident. For device fabrication and as a simple integration vehicle, vapor-liquid solid[28] (VLS) grown, single-crystal, nominally intrinsic Ge NWs with <111> longitudinal axis orientation with diameters of approximately 30 nm are employed. The NWs are enwrapped in a 20 nm thick Al_2O_3 high-k insulator shell and are further integrated into a field effect transistor (FET) architecture. Although we chose to use a bottom-up approach, our device concept is also applicable to top-down processed structures based on Ge on insulator (GeOI) substrates.[29] For contact formation, a thermally induced exchange reaction between the Ge NWs and Al contact pads was used to embed Ge channels contacted by quasi-1D monocrystalline Al NW leads[30] with abrupt Al-Ge heterojunctions.[31,32] In contrast to common metal-germanide formation,[33] the Al-Ge exchange results in a single-

elemental metallic segment with a low resistivity of $\rho = (131 \pm 27) \times 10^{-9}$ Ωm and an abrupt metal-semiconductor heterostructure without any measureable or electrically active Al impurities within the Ge segment.[32] Further, the Al-Ge contact formation overcomes the difficulty in reproducibility and deterministically defining the phase of the intruded metallic segments as the phase stability of alternative contact materials to nanometer scale Ge, such as Ni_xGe_{1-x} and Co_xGe_{1-x} are known to exhibit strong variability and yield issues.[34,35,36,37] Figure 1a shows a high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) image of the Al-Ge-Al NW heterostructure with a Ge channel length of $L_{Ge} = 1.7$ µm. High-resolution (HR) TEM images of the Al-Ge junction of the NW heterostructure enwrapped in the 20 nm thick Al_2O_3-shell and a zoomed-in image of the abrupt Al-Ge interface, are shown in Figure 1b. To enable *p*- and *n*-type FET reconfigurable operability as well as tunable NDR functionality, we add three individual top-gates to our Al-Ge-Al NW heterostructures, two aligning atop of the abrupt Al-Ge heterojunctions and one in the middle of the Ge channel. A colored SEM image of an Al-Ge-Al NW heterostructure embedded in the three-gate FET architecture is shown in Figure 1c.

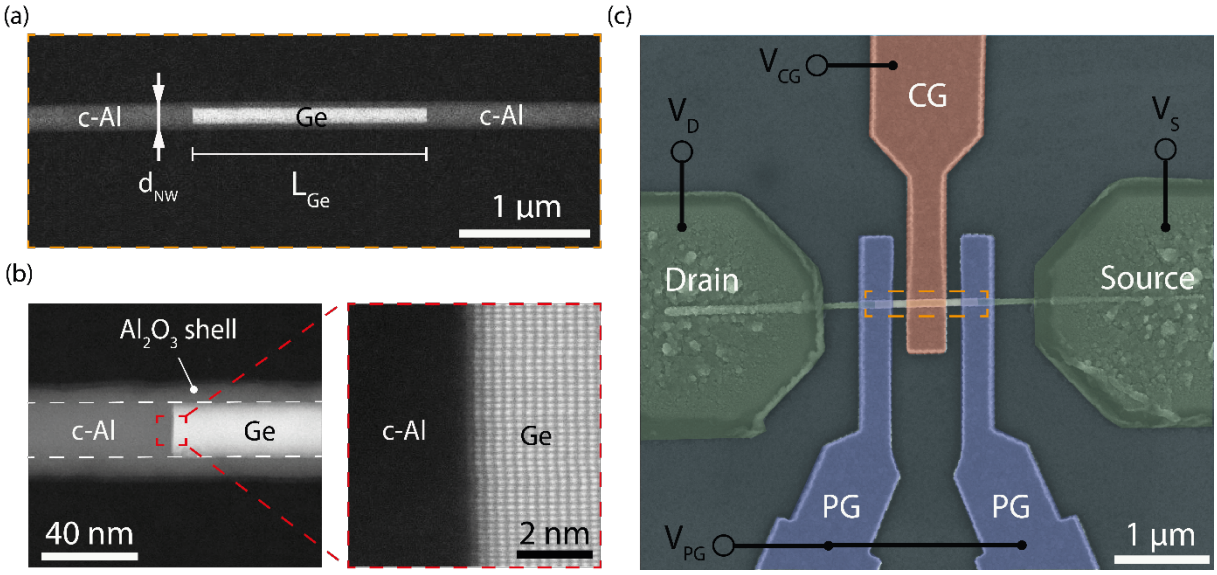


Figure 1. *Structure of the adaptable Ge nanowire transistor. (a) HAADF STEM image of an Al-Ge-Al NW heterostructure comprising a Ge segment length of L_{Ge} = 1.7 µm and a diameter*

of d_{NW} = 30 nm enwrapped in a 20 nm thick Al_2O_3 shell. (b) HR TEM images showing the entire Al-Ge interface of the NW heterostructure and a zoomed-in image, where the Ge region is oriented in the [110] zone axis. (c) Colored SEM image of an Al-Ge-Al heterostructure embedded in a three-gate FET architecture enabling RFET operation and tunable NDR functionality.

Utilizing this device architecture, we demonstrate that Al-Ge-Al NW heterostructures are capable of merging the electrical properties of unipolar *p*- and *n*-type FETs into a single type of device with identical technology, geometry and composition.[38] Consequently, reducing the technological complexity, they enable a dynamic and runtime programming of circuits at the device level.[2,39] In this configuration, the gates atop the abrupt Al-Ge junctions serve as polarity-gates (PGs) setting the charge carrier type in the channel to switch between *p*- and *n*-type operation, while the control-gate (CG) can be used to thermionically modulate the drain-current through the transistor allowing to turn the device on or off.

As seen in Figure 2, setting V_{PG} = -5 V, *p*-type operation is programmed. Transfer measurements (I_D *vs.* V_{CG}) were performed by sweeping V_{CG} between -5 V to 5 V for fixed bias voltages between V_D = -100 mV and 1 V (see respective schematic band diagram in Figure 2). Unipolar *p*-type operation is set by an upward band bending below the PGs enabling hole-injection into the Ge channel. Regulating the thermionic emission of the injected charge carriers though the Ge channel *via* V_{CG}, the transistor can be turned on (negative V_{CG}) and off (positive V_{CG}). Switching to *n*-type operation, all applied voltages are simply reversed, *i.e.* V_{PG} = 5 V, setting the junction transparent for electrons and effectively blocking the injection of holes into the Ge channel. In analogy to the previous experiments unipolar *n*-type FET operation is obtained. The on-current of the *n*-type program shows a high variation over different applied drain voltages V_D. This is perfectly correlating with the asymmetric activation energies for *p*- and *n*-type operation in Al-Ge-Al NW heterostructures, which were obtained from the slope of

the activation energy plot of $\ln(J/T^2)$ *vs.* 1000/T (Arrhenius plot).[40] A detailed description of the extraction of the activation energies is supplied in the supporting information. Whereas in the *p*-type operation no evident barrier is visible in the measurement range, a relatively high barrier was extracted for *n*-type operation (see Figure S1).[27] Importantly, compared to a single top-gate FET (see Figure S2), our multiple gate FET concept enables a suppression of source to drain leakage for both *p*- and *n*-type operation by electrostatically tuning the electrostatic shape along the Ge channel length. Through the blocking barrier formed at the drain junction, static power consumption is strongly suppressed despite the low band-gap material being employed. For comparison, we also investigated single top-gated Schottky FETs, which show a weakly ambipolar *p*-type characteristic (see supporting information). Regarding the metrics of our three-gate Ge transistor, setting $|V_{PG}| = 5$ V, a total I_{ON}/I_{OFF} ratio of approximately 3×10^5 and 4×10^2 is achieved for *p*- and *n*-type respectively. The transconductance $g_m = dI_D/dV_{CG}$ is obtained, with 90 µS/µm (*p*-type operation) and 2.1 µS/µm (*n*-type operation) (see Figure S3). Further, threshold voltages (V_{th}) of -1.4 V (*p*-type operation) and 1 V (*n*-type operation) were extracted (see supporting information). Applying $V_D = 1$ V, it was possible to achieve $J_h = 9.2 \times 10^5$ A/cm² in *p*-type operation and $J_e = 3.3 \times 10^3$ A/cm² in *n*-type operation. Compared to the single top-gate device, J_{OFF} could be significantly decreased to $J_h^{OFF} = 25$ A/cm² and $J_e^{OFF} = 16$ A/cm², about a factor of 10^3 smaller compared to the single top-gate device. Importantly, the on-currents do not show any noticeable change, as the geometry of the Al-Ge-Al heterostructure certainly remained the same. In agreement with device TCAD predictions,[41] we want to note that an enhancement of the key parameters of the proposed Ge based reconfigurable transistor are expected for thinner high-k dielectrics, enhanced interfacial layers and shorter Ge channel lengths. To confirm unipolar device operation of the proposed three-gate Ge NW transistor, Figure S4 shows the temperature dependency of *p*- and *n*-type programs. In agreement with thermionic emission theory,[42] the transfer curves in the subthreshold region are flattening with increased temperature for both operation types and an increase of the off-

current due to a higher amount of thermally generated carriers surpassing the blocking barrier is observed with increasing temperature according to the underlying transport mechanisms in the subthreshold, thermionic emission as well as thermal field emission (see equation S1). Nevertheless, an ambipolar operation is still well suppressed for both operation modes even up to T = 380 K. Further, the output characteristics for the *p*- and *n*-program are shown in Figure S5. Comparing the operation modes reveals a supra-linear output characteristic for low bias voltages of the *n*-program, with the on-current showing a high variation over different applied drain voltages V_D, which is typical for Schottky FETs.[43] In contrast, the *p*-mode characteristics exhibit a linear increase for small biases as in a conventional metal-oxide-semiconductor FET (MOSFET). These results underline the barrier extraction results in Figure S1. The demonstration of a device concept capable of resembling both *p*- or a *n*-type FET operation principally enables any logic function in a complementary design.[39] Moreover, the bidirectional nature of each transistor within a circuit enables a runtime reconfiguration of logic functions and is a clear advantage for flexible and adaptive circuit design.[4]

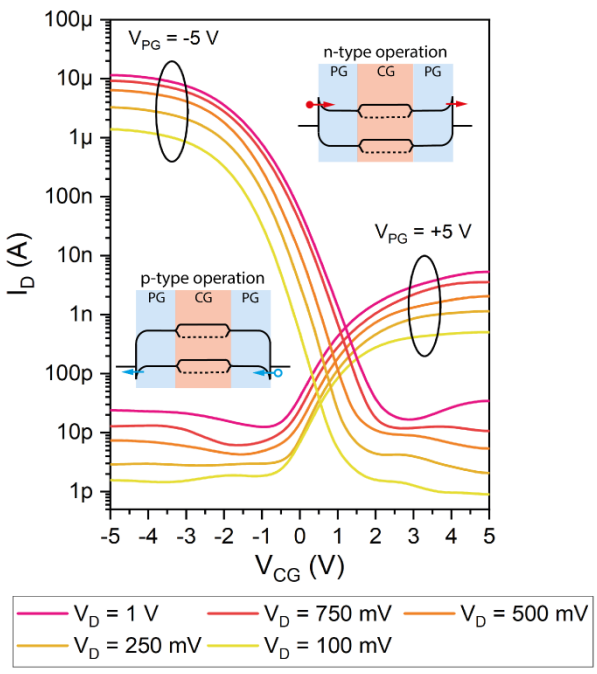


Figure 2. *Subthreshold transfer characteristic for different bias voltages between V_D = 100 mV and 1 V showing unipolar p- and n-type operation programmed by V_{PG}. The schematic band diagrams of p- and n-type device operation are inserted.*

Next, we investigate the electron-dominated transport regime of our three-gate Ge transistor. This is motivated by the previous observation of a gate-tunable NDR, where we have investigated the performance metrics and scaling capabilities of back-gated and single-top-gated Al-Ge-Al NW FETs.[27]

By applying V_{PG} = 5 V, setting the junction with a higher transparency for electrons, the downward band bending results in an enhancement of electron injection due to the barrier becoming thinner. Nevertheless, distinct to the injection of holes in the *p*-mode, only the electrons that have higher thermal energies that surpass the relatively high energy barrier are injected by thermionic emission into the semiconductor region. The high Schottky barrier for electrons is the result of our Al-Ge heterostructure, which is not available in other typical metal contacts to Ge, as with conventional metal germanide contacts. Based on the Gunn-effect originally observed by J.B. Gunn[21] and interpreted with the electron transferred effect by H. Kroemer[44] with the help of the theoretical work of C. Hilsum,[22] and B.K. Ridley – T.B. Watkins[45] a voltage controlled NDR region is observed in the output characteristics of our devices" Thereto, the injected electrons, that in our case already have a high thermal energy, surpassing the barrier gain even more energy across the channel when accelerated with sufficiently large biases to be scattered from the energetically favorable conduction band valley, characterized by a low effective mass to a heavy effective mass valley nearby.[26] Although the L- and Γ-minima are energetically close in energy (0.66 eV *vs.* 0.8 eV), *b*ased on the calculation of the coupling constants between the conduction band valleys in bulk Ge (see Table S1), it was shown that the transferred electron effect is more likely to apply involving the L- and X-minima rather than the L- and Γ-minima, with respective effective masses of m_L^* =

0.082 m_0 and $m_X^* = 0.288\ m_0$.[46] A schematic illustration of the electron transfer from the L- and X-minima is shown in the lower inset of Figure 3. A more detailed energy band-structure of Ge with all energy band-gaps is shown in Figure S6. Consequently, linearly increasing V_D while monitoring I_D for different V_{CG} between 0 V and 5 V, Figure 3 reveals voltage controlled NDR features with progressive enhancement for higher V_{CG}. To characterize this effect, the most important parameter is the peak-to-valley ratio (PVR), which is defined by $I(V_{Peak}) / I(V_{Valley})$.[17] A large and stable PVR is highly anticipated for logic applications.[15,17] As the electron concentration in the Ge channel can be modulated by varying $V_{CG,}$ a tunable PVR is observed. Consequently, starting with V_{CG} = 3 V the PVR increases from 1.2 to 7.7 at V_{CG} = 5 V. In comparison with Ge quantum dot tunneling diodes,[47] Si and Si/SiGe resonant interband tunneling diodes,[19,48] the room-temperature PVR of our best performing RFET devices is approximately a factor 10 larger. In total the characteristic of more than 10 similar devices has been measured and analyzed. All devices showed a stable and reproducible RFET and NDR characteristic.

Previously, we have also investigated the scalability of NDR in back- and single top-gated Ge NWs.[27] We found that shrinking the Ge channel length to L_{Ge} = 150 nm, a room-temperature PVR of 4.5 can be maintained and V_{Peak} can be reduced down to 0.9 V. Whereas, for this work, due to the three top-gate architecture, we have used longer Ge channels, we forecast that the current levels could be improved using a dense parallel arrangement of NWs, as carried out in Pregl *et al.*[49] by contact printing or Wind *et al.*[29] by top-down fabrication.

Moreover, as the purpose of the PGs is to lower the injection barrier for electrons (in the case of the NDR-mode), they can be used to tune the NDR. However, this was found to be limited to the peak-current, not V_{Peak}. As we were aiming for maximizing the peak current, we focused on the maximum positive voltage on the PGs of 5 V. We believe that scaling down the gate-oxide thickness, the top-gate voltages could be significantly reduced and an even better gating of the barriers at the Al-Ge junctions could be achieved.

Most importantly, as shown in the upper inset of Figure 3, our RFET device is capable of modulating V_{Peak} *via* V_{CG} between V_D = 4.1 V and 2.7 V. Hence, a cascode of devices, each biased with different V_{CG}, would result in an I/V characteristic comprising several overlapping NDR regions that could be used as MOBILE devices, enabling both NAND and NOR operations.[17,50] Moreover, this highly desired device behavior could also be effectively used for small footprint and energy efficient computational MVL, where the radix is set by the number of devices connected in series. Notably, as shown by recent circuit simulations, exploiting such characteristics, complex logic functions such as multi-value adders revealing a significantly reduced circuit propagation delay *vs*. conventional CMOS could be realized.[14,16,18]

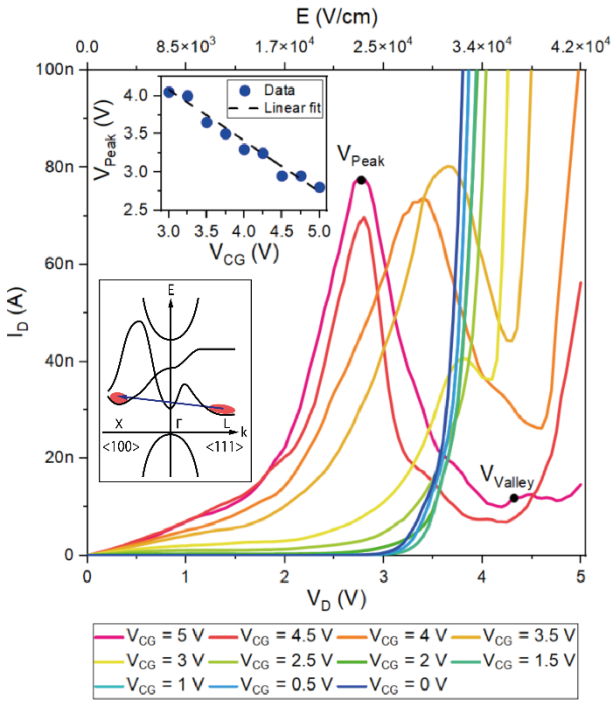


Figure 3. *I/V characteristic of a RFET device with L_{Ge} = 1180 nm for V_{PG} = 5 V and V_{CG} voltages between 0 V and 5 V showing the enhancement of NDR with increasing V_{CG}. The upper inset shows the V_{Peak} tunability on V_{CG}. The lower inset depicts a schematic representation of the band structure of Ge with indicated electron transfer from the L-valley into the X-valley enabling NDR.*

Further, Figure 4 shows the typical temperature dependence of the NDR mode, recorded for applying V_{CG} = 5 V. Due to increased thermal excitation and thus a higher electron concentration in the L-valley, the current peak before the NDR region is shifted to lower electric fields for higher temperatures. Further, associated with a decrease of transfer efficiency due to a smaller scattering mean free path related to thermal excitation of charge carriers, the PVR decreases for increasing temperatures.[15] Moreover, we note that not only the electron concentration in the L-valley increases at elevated temperatures, but both the high and low effective mass sub bands *i.e.* the Γ_1- and X-valley are also being thermally populated. Thus, the transfer of electrons from the L- to the Γ_1- and X-valley does not make any noticeable decrease of current expected from the effective mass difference. Consequently, a superposition of the thermally populated charge carriers and the electrons transferred by the Gunn-effect is evident. This can be illustrated by plotting the ratio of populations (n) at $E_{\Gamma 1}$ and E_X with respect to E_L as a function of temperature (see Figure S7).[51,52] As the ratio n_X/n_L shows a steep increase *vs*. temperature compared to *i.e.* $n_{\Gamma 1}/n_L$, the Gunn-effect appears weaker at elevated temperatures. Additionally, the efficiency of the scattering of electrons from the L- to the X-valley degrades. Despite pioneering work on the temperature dependence of Gunn-effect based on phonon scattering in highly strained Si NWs[23,53] and *n*-type InSb devices,[24] theoretical and experimental investigations of the thermal stability of NDR in Ge is still elusive.

The inset of Figure 4 shows the evaluation of the average PVR for temperatures between T = 295 K and 380 K of five similar devices. Linearly fitting the data, the average PVR decreases from 10.9 at T = 295 K to 1.2 at T = 360 K with a rate of approximately 0.1/K. Further, an average decrease of the current of about 50 % for increasing the temperature from T = 295 K to 360 K. NDR could be observed even for temperatures up to T = 360 K, which is an important prerequisite for realistic logic applications and proves the capabilities of the proposed device concept.

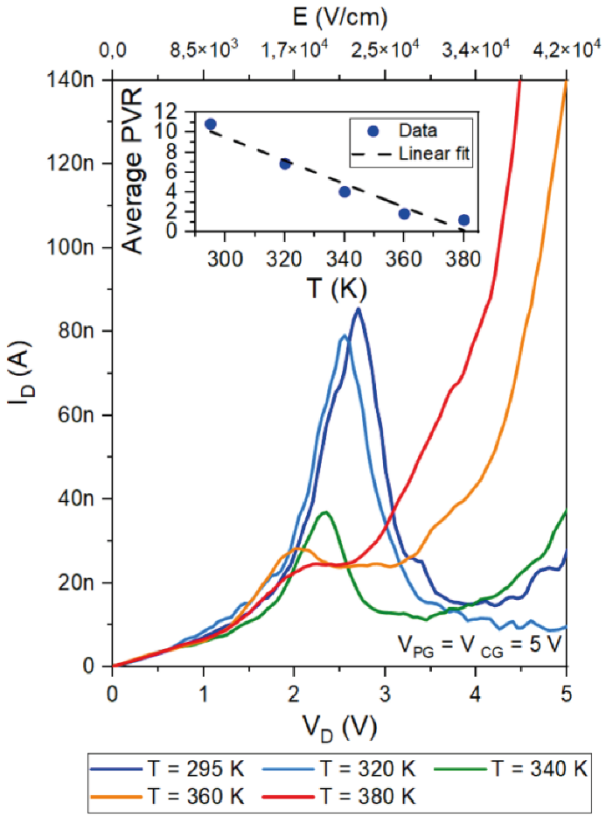


Figure 4. *I/V characteristic recorded for V_{CG} = V_{PG} = 5 V of a RFET device, recorded for temperatures between T = 295 K and 380 K. The inset shows the average temperature related PVR decrease.*

CONCLUSIONS

In conclusion, we have embedded a quasi-1D monocrystalline Al-Ge-Al NW heterostructure into a three-gate transistor architecture capable of delivering charge carrier polarity control and furthermore to enable distinct programmable NDR at runtime. NDR could be observed even for temperatures up to T = 360 K, which is an important prerequisite for realistic logic applications and proves the capabilities of the proposed device concept. Most importantly, our device concept enables a modulation of both the *PVR* and the position of the NDR peak. Hence, a cascode of devices, each biased with a different voltage on the CG, would result in an I/V characteristic comprising several overlapping NDR regions that could be used as MOBILE devices, enabling both NAND and NOR operations. Consequently, the presented NDR-mode

RFET concept offers a platform enabling applications such as static memory cells, fast switching logic circuits or small footprint and energy efficient computational MVL. In this respect, our investigations might provide a significant step towards a beyond CMOS approach enabling functional diversification and alternative computing.

METHODS/EXPERIMENTAL

Device fabrication:

The starting materials were Ge NWs with diameters of approximately 30 nm grown on a Si (111) substrate using the VLS process with germane (GeH_4, 2% diluted in He) as precursor and a 2 nm thick sputtered Au layer as growth promoting catalyst. The growth was performed in a low-pressure hot wall CVD chamber. Subsequent to the growth, the Ge NWs were coated with 20 nm high-k Al_2O_3 using atomic layer deposition. The passivated Ge NWs were drop-casted onto a 100 nm thick thermally grown SiO_2 layer atop of a 500 µm thick highly *p*-doped Si substrate. Al contacts to the Ge NWs were fabricated by a combination of electron beam lithography, 22 s of BHF (7:1) etching and 5 s HI (30%) etching to remove the Al_2O_3-shell as well as the native Ge oxide shell at the contact area, 100 nm Al sputter deposition and lift-off techniques. A successive thermally induced exchange reaction by rapid thermal annealing at a temperature of T = 624 K in forming-gas atmosphere initiates the substitution of Ge by Al.[31,32,54] Facilitating this heterostructure formation scheme allows the integration of single-crystalline monolithic Al-Ge-Al NW heterostructures with tunable channel lengths. Further, omega-shaped Ti/Au top-gates were fabricated using a combination of electron beam lithography, Ti/Au evaporation (8 nm Ti, 125 nm Au) and lift-off techniques.

High-resolution HAADF STEM:

HAADF STEM was performed on Al-Ge-Al NW heterostructures fabricated on 40 nm thick Si_3N_4 membranes using a probe-corrected FEI Titan Themis, working at 200 kV. The Al-Ge interface in the shown images is viewed along the [112] direction of observation of the Ge crystal.

Electrical characterization:

The electrical measurements were carried out at room temperature and ambient conditions using a combination of a semiconductor analyzer (HP 4156B) and a probe station. Source-measure units were used for all device terminals. Gate currents were found to be below 1 pA. To minimize the influence of ambient light as well as electromagnetic fields, the probe station was placed in a dark box.

ASSOCIATED CONTENT

Supporting Information Available:

Estimated effective energy barrier of an Al-Ge-Al NW heterostructure, analysis of the electrical transport of a top-gated Al-Ge-Al NW heterostructure, evaluation of the transconductance and extraction of the threshold voltage of the three-gate Ge RFET, temperature dependent *p*- and *n*-type subthreshold transfer characteristics of the three-gate Ge RFET, more detailed band-structure of Ge including all energy band-gaps, calculated coupling coefficients between the conduction band valleys in Ge, simplified estimation of the charge carrier population in the Γ_1- and X-valley in dependence of the temperature regime of 295 – 380 K, examples for NDR-mode RFET circuits. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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Author Contributions

# M.S. and R.B. contributed equally to this work. M.S. and R.B. performed the device fabrication. R.B., M.S. and D.F. conducted the measurements. M.A.L. and M.I.H. carried out the TEM characterization and analysis. A.L. provided helpful feedback and commented on the manuscript. M.S. and W.M.W. conceived the project and contributed essentially to the experimental design. All authors analyzed the results and helped to shape the research and manuscript.

Notes

The authors declare no competing financial interest.

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