Influence of the Cl_2 etching on the Al_2O_3 /GaN metal–oxide–semiconductor interface

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Running Authors: Meyer *et al.*

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ABSTRACT

Controlling the plasma etching step involved in MOSHEMT GaN fabrication is essential for device performance and reliability. In particular, understanding the impact of GaN etching conditions on dielectric/GaN interface chemical properties is critically important. In this work, we investigate the impact of the carrier wafers (CW) (Si, photoresist, SiO_2, Si_3N_4) used during the etching of GaN in chlorine plasma on the electrical behavior of Al_2O_3/n-GaN metal-oxide-semiconductor (MOS) capacitors.

XPS analyses show that the Al_2O_3/GaN interface layer contains contaminants from the etching process after the Al_2O_3 deposition. Their chemical nature depends on the plasma chemistry used as well as the chemical nature of the carrier wafer. Typically, Cl and C are trapped at the interface for all substrates. In the particular case of Si carrier wafer, a significant amount of SiO_x is present at the Al_2O_3/GaN interface. the capacitance–voltage characteristics (C–V) of the MOS capacitors indicate that the presence of Si residues at the interface shifts the flat band voltage to negative values, while the presence of Cl or C at the interface increases the hysteresis. We demonstrate

that introducing an *in situ* plasma cleaning treatment based on N_2/H_2 gas, before the ALD deposition, allows the removal of most of the residues except silicon and suppresses the hysteresis.

I. INTRODUCTION

In the last decade, GaN-based transistors have experienced significant adoption because of their high-power and high-frequency characteristics, along with their capacity to function at high temperatures. Conventional GaN transistors operate in a normally-on condition (*i.e.* depletion mode). For high power applications, normally-off devices (*i.e.* enhancement mode) are preferred because of the circuit simplification and safe operation1.

Varieties of approaches, including gate recessed[2,3], fluorine ion implantation[4], p-GaN cap layer[5,6] have been exploited to achieve the normally-off behavior of GaN-based devices. The gate recessed approach is a promising technology since it enables to keep high mobility and high density of electrons without compromising the voltage threshold. Among the different technical steps used in the GaN recess approaches, plasma etching is widely employed to control accurately the recessed depth. However, the etching step modifies the GaN surface composition (*e.g.* N-depleted surface, etch residues) and the surface morphology[7,8]. The deterioration of the GaN surface necessarily leads to a poor dielectric/GaN interface quality. The latter is responsible for an increase in hysteresis, frequency dispersion, and interface density states. Electrical characteristics are commonly compared regarding different dry or wet etching processes. Wang *et al.* observed the modification of the electrical characteristics when using different chlorinated-based

etching gases[9]. Vauche *et al.* showed that the interface composition influences the threshold voltage on GaN MOS-HEMT[10]. Jackson *et al.* observed modification of the interface composition and the average interface trap density[11].

To recover the GaN electrical properties, prior to the dielectric deposition, the surface passivation has been extensively studied using wet cleaning or plasma passivation[12-14]. However, the nature of the chemical bonds within the interface is not necessarily specified as most of the studies are focused on oxidation rate or stoichiometry.

In a previous study, we thoroughly investigate the GaN surface modifications after Cl_2 etching under various bias voltage and according to the carrier wafer used (Si, SiO_2, Si_3N_4, photoresist), by XPS and AFM analyses[7]. We showed that the GaN surface is differently damaged and contaminated, given that each carrier wafer produces etch by-products of different chemical nature that can redeposit on the GaN surface.

In this study, we propose to correlate the GaN surface degradation, observed after Cl_2 etching according to the carrier wafer, to the electrical behavior of GaN assessed by CV measurements. To this aim, a back-to-back Metal-Insulator-Semiconductor (MIS) capacitor is fabricated using Al_2O_3 as a dielectric. In the first part of the paper, we investigate the chemical composition of the interface between the Al_2O_3 and the etched GaN surface by means of ARXPS, and link the presence of contaminations at the interface with the electrical characteristics of GaN. In the second part of the paper, we carried out the beneficial impact of an N_2/H_2 *in situ* plasma cleaning prior to the Atomic Layer Deposition (ALD) to clean the etched GaN surface, and consequently to improve the GaN electrical behavior.

II. EXPERIMENTAL

A. *Etching experiments*

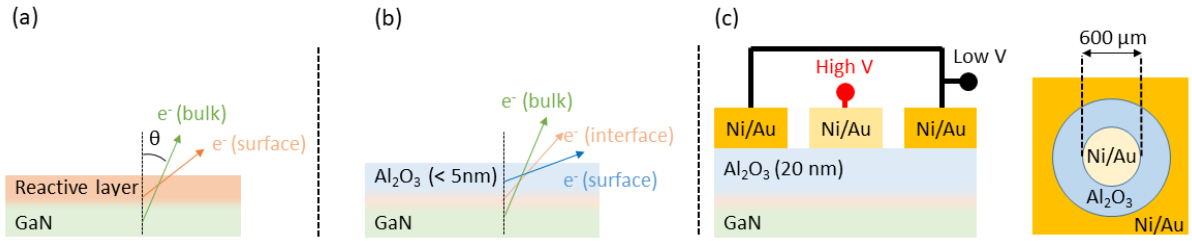

Fig. 1. Samples used for (a) XPS characterization of GaN surface after etching (b) the XPS characterization of Al_2O_3/GaN interface and (c) capacitance-voltage measurements.

The material under investigation is a GaN layer grown by metalorganic chemical vapor deposition (MOCVD) on a 200 mm p-type silicon (111) substrate. The III-N stack consists of an AlN nucleation layer, transition layers, a carbon-doped GaN layer, and a 1.5 µm-thick n-type Si-doped GaN layer ($N_D = 5 \times 10^{17}$ cm^{-3}).

The etching processes are performed in a 300 mm Centura® Advant-Edge™ MESA™ inductively coupled plasma (ICP) etch tool commercialized by Applied Materials. More details of the etching tool can be found elsewhere[15]. During the etching experiments, the 1.5×1.5 cm² GaN samples are thermally glued with a thermal paste at the center of a 300 mm carrier wafer. Several carrier wafers have been used: a bare Si wafer, or a Si Wafer on which either a 1 µm-thick photoresist is spin coated or a 100 nm-thick SiO_2 is thermally grown or a 55 nm-thick Si_3N_4 is deposited by Low-Pressure Chemical Vapor Deposition.

GaN samples are then exposed to Cl_2 plasma using the following conditions: the Cl_2 flow rate is 100 sccm, the pressure is 5 mTorr and the source power is 600 W. The

bias power is adjusted to obtain a bias potential of -100 V measured by a Retarding Field Energy Analyser (RFEA, Semion™ RFEA system). Etch time is adapted to reach an etching depth of 100 nm.

A preliminary study using 0.5×1 cm² etched GaN samples with photoresist pattern has been necessary to estimate the etch rate using Atomic Force Microscopy (AFM, Dimension Icon bruker).

B. Surface and interface composition characterization

Angle-Resolved X-Ray Photoelectron Spectroscopy (ARXPS, Thermo Avantage Theta 300) is used to analyze the GaN surface after etching (Fig. 1.a), as well as to investigate the chemical composition of the interface Al_20_3/GaN (Fig. 1.b). For this latter purpose, the etched GaN samples are cleaned in 45% KOH solution at room temperature for 5 min. Then the Al_20_3 dielectric material is deposited on the GaN sample by ALD deposition at 300°C and using Trimethylaluminum (TMA) and H_2O as precursors for aluminum and oxygen, respectively. The number of ALD cycles is set at 50, corresponding to an Al_2O_3 thickness of less than 5 nm.

The X-ray experiments use a monochromatic Al Kα X-ray source (1486.6 eV). The pass energy and the energy step size are set at 70 eV and 0.1 eV, respectively. Low-energy electrons, generated by Ar gas, are used to compensate for the surface charging during the XPS analyses. The angle-resolved capability of the Theta 300 is used for all analyses, with eight angles regularly spaced between 23.75° and 73.25° (*i.e.* collection angle) referred as the normal of the wafer. The Ga 3d core level is decomposed with a doublet, and the N 1s core level is fitted by considering the Ga $L_{2,3}M_{4,5}M_{4,5}$ auger lines. More details about the N 1s and Ga 3d fitting procedure can be found in reference[7].

Concentration depth profiles are reconstructed using the Maximum entropy method provided by the Thermo Avantage software[16,17]. For as-etched samples, the XPS spectra are calibrated by positioning the Ga $3d_{5/2}$ peak corresponding to the N-Ga-N chemical state at 19.4 eV, based on the pristine sample analysis. Note that if adventitious carbon is present on the samples, the C 1s peak is taken as a reference at 284.8 eV.

The depth profile generation requires to define a model consisting of an Al_2O_3 overlayer, the interfacial layer, and the GaN substrate, and to attribute for each layer the associated XPS peaks. The Al 2p and O 1s core levels are attributed to the Al_2O_3 layer, and the O/Al ratio is set to 1.5. The Ga 3d peak and N 1s core levels are attributed to GaN material, with the N/Ga ratio being fixed to 1. For the interfacial layer, there are no constraints regarding the other elements detected by XPS (*i.e.* Cl 2p, C 1s, Si 2s).

C. C-V electrical characterization

In order to assess the damage generated by the plasma process, back-to-back Metal-Insulator- Semiconductor (MIS) capacitors are fabricated as shown in Fig. 1.c.

A 20 nm thick Al_2O_3 layer is deposited by ALD on the GaN etch samples. Standard photolithography is performed using SUSS MicroTec MJB4 lithography equipment to define the contacts. Ni/Au (30/100 nm) metal deposition is performed by electron beam evaporation at vacuum ($\leq 10^{-6}$) mbar using a MEB550 tool from PLASSYS. After metallization, the photoresist and unwanted metal layers are stripped from the surface of the substrates using acetone.

A Keithley 4200A SCS analyzer is used to perform capacitance-voltage (C-V) measurements. Data are recorded with a sweep voltage mode (0.25 $V.s^{-1}$). All the electrical measurements are carried out under ambient conditions.

III. RESULTS AND DISCUSSION

A. Al_2O_3/GaN interface composition

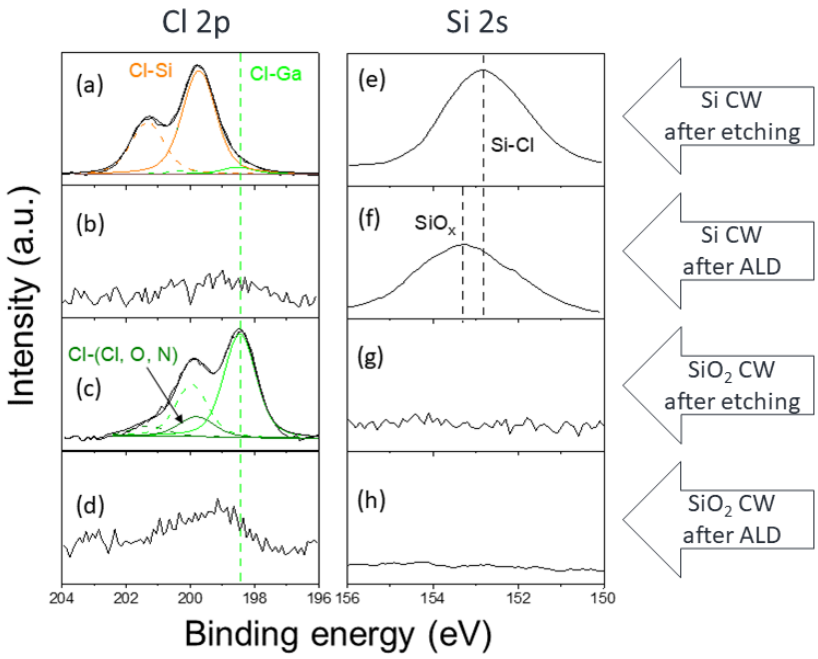

Fig. 2. Cl 2p spectra of GaN on Si (a) after etching (b) after ALD; GaN on SiO_2 (c) after etching (d) after ALD. Si 2s spectra of GaN on Si (e) after etching (f) after ALD; GaN on SiO_2 (g) after etching (h) after ALD.

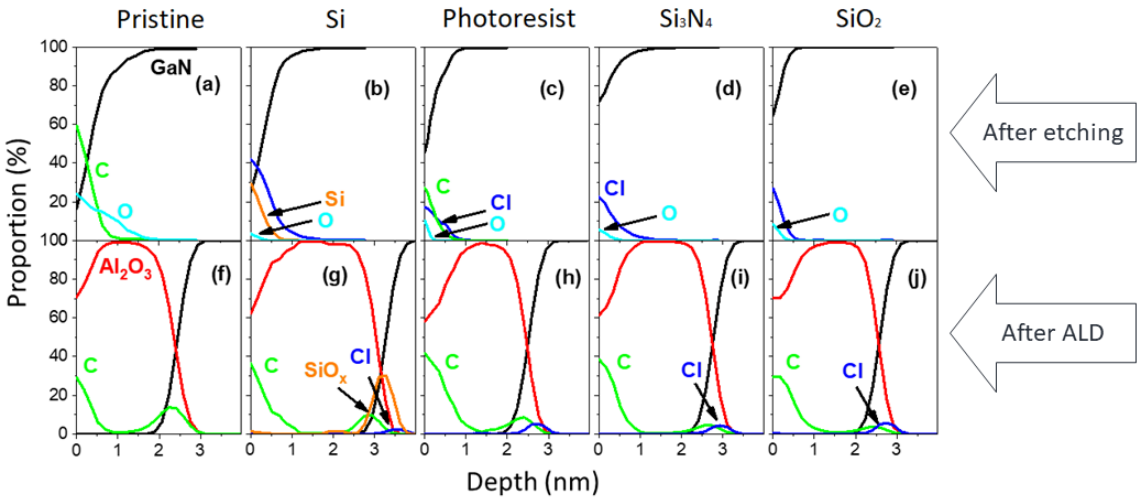

Fig. 3. Atomic concentration profile of GaN surface obtained from ARXPS measurements after etching (a-e) after Al_2O_3 deposition (f-j). GaN pristine sample (a and f), GaN etched with Si substrate (b and g), with photoresist substrate (c and h), with Si_3N_4 substrate (d and i), with SiO_2 substrate (e and j).

Set	*Binding energy (eV)*				*Concentration at the surface/interface (%)*		*Al_2O_3 thickness (nm)*
	Ga-N (Ga $3d_{5/2}$)	Al-O (Al 2p)	Cl-Ga[a] (Cl $2p_{3/2}$)	Si 2s[b]	Carbon	Chlorine	
After etching	19.4		198.7	153.1	30[c]	20-40	
After ALD	19.4	74.5	n/a	153.3	5-15	2-6	≈ 2.5

Table 1. Extracted data from XPS (Fig. 2) and ARXPS (Fig. 3). *[a]not observed with pristine GaN; [b]observed with the Si carrier wafer; [c]observed with the photoresist carrier wafer.*

Figure 2 shows the decomposition of Cl 2p and Si 2s core levels for the Si and SiO_2 cases, but similar results as the SiO_2 case are obtained for Si_3N_4 and photoresist carrier wafers. Table 1 lists the binding energy values, the concentration of contaminants (C and Cl) and the Al_2O_3 average thickness after etching and after ALD.

In our previous work, we showed that after Cl_2 etching, some contaminants are found on the GaN surface whose chemical nature is dependent on the carrier wafer used. Indeed,

during the Cl_2 process, the carrier wafer is also etched and the etch byproducts emitted can then participate in the GaN etching or redeposit on its surface. For all carrier wafers, a substantial amount of Chlorine (bonded to Gallium) was detected on the GaN surface, as evidenced by the presence of a peak at 198.7 eV on the XPS spectra in Figure 2 a/c.

In the case of the Si carrier wafer, $SiCl_x$ species are also detected on the GaN surface, as evidenced by the major contribution at 199.6 eV (Fig. 2.a), and the Si 2s peak at 153.1 eV (Fig. 2.e). $SiCl_x$ compounds were not detected when using either the Si_3N_4 or the SiO_2 wafer (Fig 2.g). In our previous study, we showed that under this plasma etching conditions, the Si carrier wafer is etched 5-10 times faster than the SiO_2 and Si_3N_4 wafers. The associated optical emission spectroscopy experiments indicated that a large amount of $SiCl_x$ and Si species are present in the plasma if a Si carrier wafer is etched, while a fewer amount of Si and SiCl was detected in the Si_3N_4 and SiO_2 cases. It is suspected that SiOCl species, that cannot be detected by OES, are emitted in the plasma during the SiO_2 etching. The Si-based species present in the plasma can then interact with the GaN substrate, explaining the presence of $SiCl_x$ compounds for the Si wafer (Fig 2.a/e). Although some traces of Si-based species may be present in the plasma in the Si_3N_4 and SiO_2 cases, Silicon-related byproducts are not detected on the GaN surfaces for the Si_3N_4 and SiO_2 cases. If present, they are under the detection threshold of the XPS technique.

Concentration in-depth profiles of GaN surfaces, after etching, are illustrated before (Fig. 3.a) and after Cl_2 plasma exposure (Fig. 3.b-e) according to the carrier wafer. As mentioned above, a non-negligible amount of chlorine is found on the GaN surface in all cases. Oxygen traces were also detected (< 10%), although the XPS analyses were quasi

in situ experiments. This oxygen contamination originates from the etching of the Y_2O_3 reactor wall. Finally, in the case of the Si carrier wafer, a large amount of $SiCl_x$ species is detected on the GaN surface, while carbon contamination is observed with the photoresist carrier wafer.

Similar XPS experiments are performed on the etched GaN, after the KOH wet treatment and the subsequent Al_2O_3 dielectric deposition, as shown with the reconstructed in-depth profiles in Fig 3.f-j. In all cases, around 10% of carbon is detected at the Al_2O_3/GaN interface. The carbon contamination comes from the air exposure, after the etching and the wet treatment. Furthermore, the chlorine concentration is found to be around 5% at the interface, suggesting that Cl contamination cannot be removed with the KOH etching (Fig. 2 b/d). A similar observation can be made for the Si contamination. The latter is not removed by the KOH wet etching (Fig. 2.f), and a Si-O chemical bond is found at the Al_2O_3/GaN interface (Fig. 3.g). This fact is supported by the Si 2s peak position shifting from 153.1 eV after etching to 153.3 eV after ALD deposition (Fig. 2.e/f). This indicates that The $SiCl_x$ species are converted into SiO_x species during air exposure and the H_2O step of the ALD.

B. Electrical characteristics

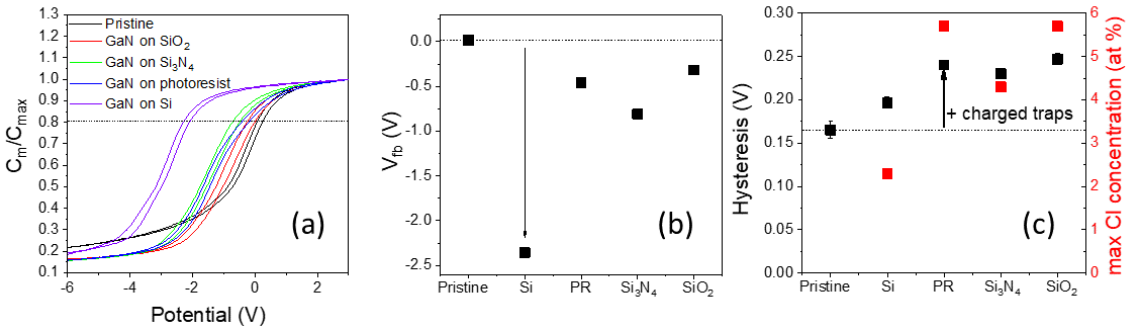

Fig. 4. (a) C-V curves (c) Flat band voltage and (c) Hysteresis of Al_2O_3/GaN MOS with different carrier wafers after Cl_2 etching.

Fig. 4 shows the normalized measured C-V characteristics of the non-etched GaN sample and the GaN etched samples with the 4 different carrier wafers. The voltage is swept from inversion (- 6 V) to accumulation (3 V) regions at a fixed frequency of 10 kHz. Flat band voltage is extracted using flat band capacitance[18-19] and plotted in Fig. 4.b. Compared to the non-etched sample, the etched samples exhibit a flat band voltage shift toward negative values. This could be attributed to the amorphization of the GaN surface or the degradation of the surface stoichiometry after such plasma conditions as reported previously[7].

Moreover, in the case of the Si carrier wafer, the significant V_{fb} shift could be related to the presence of SiO_x layer, as supported by previous studies. It was found that Al_2O_3/SiO_2 interface generates an electrical dipole layer formation at its interface[20-23]. Nevertheless, these works demonstrate an additional positive dipole strength that cannot explain the observed opposite variation of the V_{fb}. On the other hand, the formation of SiO_x/GaN generates positive charges which, in turn, causes a negative flat band voltage shift[24,25].

The Al_2O_3/GaN pristine sample exhibits a hysteresis of 0.16 V (Fig. 4.c), which is influenced by charge traps located in the Al_2O_3/GaN interface. The interface state density is probably related to the residual carbon, which behaves as a deep acceptor at the interface[11,26].

A systematic increase of the hysteresis is also found for the etched materials compared to the pristine sample value, which could be attributed to the Ga-Cl chemical bonding that generates a structural disorder.

This preliminary study highlights the impact of the contaminants brought by the plasma-etching step. Furthermore, it demonstrates that a KOH wet treatment is not efficient enough to remove those residues and the electrical degradation. The presence of carbon at the interface plays a non-negligible role on the GaN electrical characteristics. As mentioned in Sec III.a, the carbon contamination cannot be avoided by a wet treatment before the ALD deposition. That is why in the next section, we propose to evaluate a recovery process that is carried out in the ALD chamber (*i.e. in situ*), prior to the ALD deposition.

C. *Recovery of etching damages*

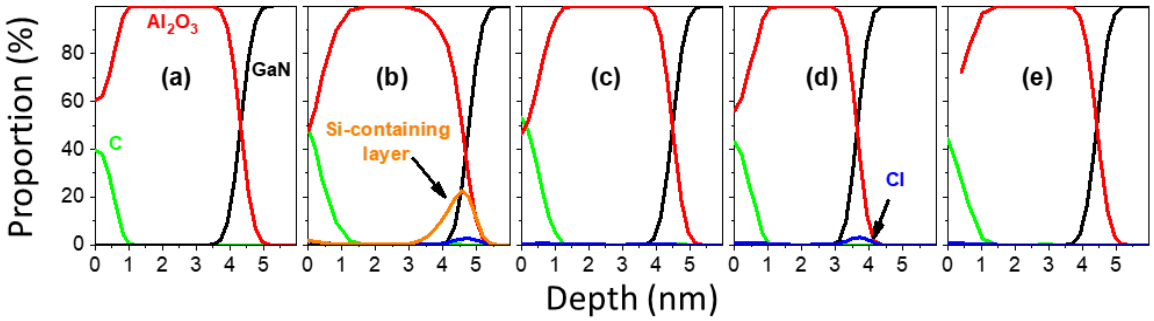

Fig. 5. Atomic concentration profile of GaN surface obtained from ARXPS measurements after dry etching, wet etching, H_2/N_2 *in situ* surface cleaning and ALD. (a) Pristine GaN (no dry etching); dry etched GaN with (b) Si (c) Photoresist (d) Si_3N_4 and (e) SiO_2 carrier wafers.

Set	*Binding energy (eV)*				*Concentration at the surface/interface (%)*		*Al_2O_3 thickness (nm)*
	Ga-N (Ga $3d_{5/2}$)	Al-O (Al 2p)	Cl-Ga (Cl $2p_{3/2}$)	Si 2s[a]	Carbon	Chlorine	
w/ *in situ* cleaning	19.2	74.5	n/a	152.7	n/a	0-3	≈ 4.5

Table 2. Extracted data from XPS decomposition and ARXPS data (Fig. 5). [a]*observed with the Si carrier wafer.*

XPS experiments are carried out on pristine and etched GaN samples, after the KOH treatment, and an *in situ* N_2/H_2 treatment of the GaN surface is performed in the ALD chamber prior to the dielectric deposition.

Improvement of the interface quality is evidenced for *in situ* cleaned samples in Fig. 5 and Table 2, with the carbon removal and a lower chlorine concentration (≈ 2%) compared to the untreated samples (see Fig. 3). Furthermore, the nucleation of Al_2O_3 is influenced by the GaN interface composition. This inference is supported by a slight increase of the Al_2O_3 thickness (≈ 4.5 nm) compared to the uncleaned samples (≈ 2.5 nm). This confirms the low reactivity of the C-terminated and the Cl-terminated surfaces,

resulting from the air exposure and plasma etching, toward the ALD reactants. Similar behavior was also found during Al_2O_3 ALD processes on Si when using NH_3/N_2 pretreatments prior to the ALD[27].

In the case of the Si carrier wafer, silicon is still detected at the interface (Fig. 5b), and the Si 2s peak is now centered at 152.7 eV (not shown), indicating a lower oxidation state. Therefore, the H_2/N_2 cleaning does not remove the silicon contamination but generates a different chemical environment for Si atoms.

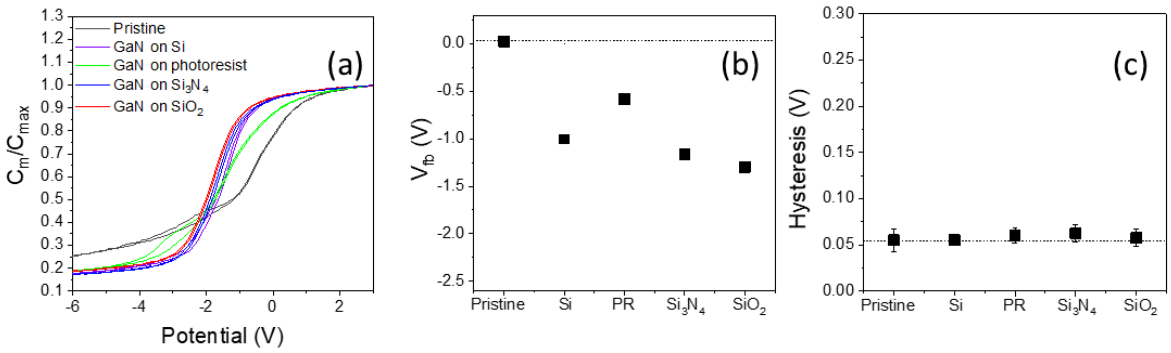

Figure 6. (a) C-V curves (10 kHz) (c) Flat-band voltage and (c) Hysteresis of Al_2O_3/GaN MOS with different carrier wafers with H_2/N_2 *in situ* cleaning.

Fig. 6 shows the normalized measured C-V characteristics after the KOH wet etching and the H_2/N_2 *in situ* cleaning process prior to the ALD.

The V_{fb} value of the pristine GaN sample is not affected by the *in situ* cleaning (≈ 0 V) (Fig. 6.a/b). A negative shift of the V_{fb} is still observed after etching, which is in the same order of magnitude with or without the *in situ* N_2/H_2 treatment, except in the case of the Si carrier wafer for which the negative shift is lower with the *in situ* treatment. XPS results of this study suggest that it is related to the change in the less oxidized chemical environment of Si.

On the other side, the H_2/N_2 cleaning has a beneficial impact on the hysteresis, which is now reduced down to 0.05 eV for non-etched and etched GaN samples (Fig. 6.c). The comparison between the two sets (with and without *in situ* cleaning) confirms that contaminants (C, Cl) act as charge traps and are responsible for the hysteresis behaviour.

IV. SUMMARY AND CONCLUSIONS

In this article, we investigate the impact of GaN etching conditions on Al_2O_3/GaN interface chemical properties and the related consequences on the electrical behavior of Al_2O_3/n-GaN metal-oxide-semiconductor (MOS) capacitors. In particular, we examine the role of the carrier wafer (Si, PR, Si_3N_4, or SiO_2) used during the etching of GaN in Cl_2 plasma.

ARXPS analyses show that after the GaN etching followed by KOH cleaning and Al_2O_3 deposition, the Al_2O_3/GaN interface layer contains contaminants from the etching process. Their chemical nature depends on the plasma chemistry, as well as the chemical nature of the carrier wafer. Typically, Cl and C are trapped at the interface for all substrates. In the particular case of the Si carrier wafer, a significant amount of SiO_x is present at the Al_2O_3/GaN interface. This implies that the KOH wet is not efficient to remove the etching contaminants. As a consequence, the capacitance–voltage characteristics (*C–V*) of the MOS capacitors indicate that the flat band voltage is negatively shifted for all etched samples and in particular when a Si carrier wafer is used, as well as hysteresis of about 0.2-0.25 V.

The V_{fb} shift and the hysteresis are probably due to the amorphization, stoichiometry degradation, and the trapped Cl and C contamination caused by the plasma process at the interface. We showed that by using an *in situ* N_2/H_2 treatment prior to the ALD deposition, the C and Cl contaminations can be mostly eliminated resulting in a reduction of the hysteresis for all samples down to 0.06 V.

ACKNOWLEDGMENTS

This research was supported by the French RENATECH network and the Nano 2022 program.

AUTHOR DECLARATIONS

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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