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A self-referenced on-chip jitter BIST with sub-picosecond resolution in 28 nm FD-SOI technology

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***Abstract*— This paper describes an on-chip instrument for the estimation of absolute and period random jitter of clock signals in the GHz range with a sub-picosecond resolution. A self-referenced technique is used to remove the need of a very clean external reference clock. The instrument has been designed in STMicroelectronics 28 nm FDSOI technology. By exploiting the fine delay control which can be achieved with this technology, simulation results haven shown a resolution down to 100 fs for GHz clock signals with a simple calibration procedure. The instrument meets the requirement of a small footprint while using a standard digital test interface to transfer data. It can be configured in different ways to suit the resolution and frequency of operation requirements.**

I. INTRODUCTION

Clock jitter is due to the deviation of clock edges relative to a reference time frame. In any system where a clock is used to time events, jitter can cause uncertainty in regular occurrences of these events. High-speed I/O interfaces, for example, use clock edges to sample bits at the receiver. Jitter in the sampling clock translates to erroneous sampling instants, thereby causing bit errors. In communication systems operating in the Gigabit/s range, clock jitter has a very large impact on the system performance in terms of Bit Error Rate (BER).

A System-on-Chip (SOC) operating with clocks in the GHz range, offering BER as low as 10^{-12} can tolerate clock jitter of a few picoseconds. However, with the continuous increase in clock frequencies, measuring clock jitter in the femtosecond range has become a necessity. Jitter measurement in this range for production testing or through prototyping design stages needs high-speed oscilloscopes or spectrum analyzers which are also often expensive. Tapping high speed clocks for off-chip measurement itself leads to inaccuracies in measurement due to RLC effects. On-chip jitter measurement could be an alternative solution to reduce the impact and the cost of jitter measurement. A complete embedded instrument can be used for monitoring noise, aging and environmental effects, for diagnostics or for parameter control in multiple applications.

Removing the need of an external reference clock is often desired to further reduce complexity. On-chip jitter measurement schemes that do not need an external reference clock for sampling the clock of interest are generally termed as self-referenced techniques. A delayed version of the clock is used as the sampling clock for jitter estimation but an accurate control of the clock delay is essential for very high resolutions.

Jitter is generally classified as random or deterministic, depending on the sources that produce it. It is described with its histogram or Probability Density Function (PDF), and characterized by its peak-to-peak or Root-Mean-Square (RMS) values [1]. For each type of jitter, different types of measurements exist such as absolute, period, cycle-to-cycle, N-period, etc. In this paper, we concentrate on absolute jitter since the other types of jitter can be derived from it.

This paper focuses on the implementation of a self-referenced jitter Built-in Self-Test (BIST) instrument that can estimate random jitter for clock signals up to a few GHz. By exploiting the fine delay control which can be achieved with a 28 nm FD-SOI technology, simulation results of a test instrument show a resolution down to 100 fs in a design that uses minimum size transistors and standard flip-flops. Both absolute (also known as timing) and period jitter can be considered following state-of-the-art theory on self-referenced techniques.

The rest of this paper is organized as follows. Section II briefly reviews the state-of-the-art on jitter on-chip testing, in particular self-referenced techniques. Section III discusses a transistor level implementation in 28 nm FDSOI technology of the basic blocks required for building this instrument, including simulations at the transistor level. Next, Section IV describes a prototype implementation of the test instrument with simulation results that demonstrate the feasibility. Finally, a summary of the results and future work is given in Section V.

II. ON-CHIP JITTER MEASUREMENT STATE-OF-THE-ART

Many approaches for measuring on-chip the jitter of a clock Signal Under Test (SUT) have been developed in the last two decades. We can distinguish two main categories of on-chip jitter measurement techniques that include, on one hand, the use of an external clock reference and, on the other hand, self-referenced techniques.

The first category includes conventional techniques that use a clean reference clock. For on-chip measurement, the most well-known approach is based on coherently undersampling the SUT with the external clock. A major advantage of undersampling is that it does not require on-chip delay lines, matched oscillators or calibration, and it reduces the noise and process-sensitive circuitry to one or several latching elements. Postprocessing of the digital signal obtained allows the extraction of the jitter PDF [2]. Earlier works using this approach were used to measure rise and fall times [3]. For high frequency gaussian jitter, it is possible to directly obtain the RMS jitter without the need of extracting the histogram [4]. Jitter RMS values close to 100 fs have been experimentally demonstrated with an external clock by undersampling signals up to 6 GHz [5]. Other on-chip techniques have used

oversampling and interpolation techniques at lower signal frequencies to reach picosecond resolution [6].

In a major departure from these approaches, the second category of on-chip techniques removes the need of an external reference clock. A delayed version of the SUT is used to sample the clock itself to extract the jitter [7]. A general block diagram of a self-referenced jitter measurement is shown in Fig. 1. The instrument consists of an NT delay block, a variable delay element, a phase comparator, and finally a counter for generating the values of the histogram bins.

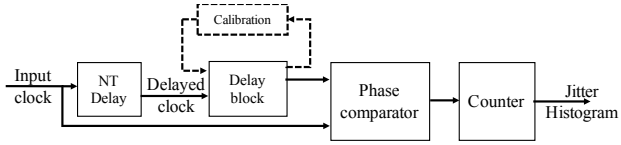


Fig. 1. Block diagram of self-referenced jitter measurement.

The self-referenced technique uses an NT delay block to delay the SUT, where N is the number of delayed periods and T the period of the SUT. The NT delayed clock will be hereafter referred to as the sampling clock. As demonstrated in [8], if N=1, the jitter in the adjacent edges is very highly correlated and it is possible to extract directly the period jitter that is measured by construction. Alternatively, by setting the NT delay to multiples of the clock period, the jitter correlation will be very low (at least for random jitter) and the absolute jitter can be extracted with a gain of $\sqrt{2}$ from the N-period jitter that is measured by construction.

The variable delay block allows sampling the SUT at various instants of time in the vicinity of the expected clock edge. The sampling clock is progressively delayed with respect to the SUT with an increment Δ at each step, where Δ is the resolution of the jitter estimate. For each delay, the SUT is sampled *n* times (i.e., during *n* cycles) in order to produce the value of the corresponding histogram bin. In each cycle, both clock signals are compared by a phase comparator and a counter stores the number of high logic levels (hits). The calculated bin values are finally assembled to produce a jitter histogram from which parameters such as RMS jitter can be calculated.

A path is included to very precisely calibrate the delay of the variable delay block. This calibration defines the resolution of the jitter measurement technique. The NT delay also needs to be calibrated although this is easier. The NT delay must approach the value of $N\overline{T}$, where $\overline{T}$ is the average period of the SUT, with a resolution Δ as for the case of the jitter estimate.

Self-referenced techniques for on-chip jitter measurement have been experimentally demonstrated with a resolution of 400 fs in [9], and 300 fs later in [5], for signals up to a few GHz. A resolution below 100 fs has been shown experimentally in [8], but with signals below 1 GHz with the use of a time-difference amplifier. Recently, an instrument with automatic calibration has been demonstrated in a 28 nm CMOS process but with picosecond resolution with signals up to 1 GHz [10]. The aim of this work is the design of a small footprint self-referenced jitter measurement instrument in 28 nm FDSOI technology that can meet a resolution of at least 100 fs for GHz signals which has yet to be demonstrated.

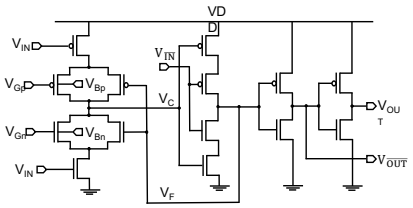


Fig. 2. Delay element [11].

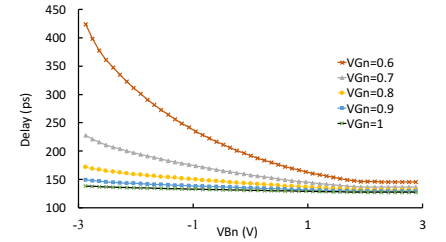
III. Implementation of Basic Blocks in 28 nm FD-SOI

A. NT delay

This block is aimed at delaying the SUT an integral number of clock cycles. In this work, we will use a chain of delay elements of the type shown in Fig. 2 [11]. The delay between the rising edges of V_{OUT} and V_{IN} is controlled. The delay element consists of a current starved inverter followed by a gated inverter stage and a final driving stage for the output signal. The gate control voltages (VGp, VGn) and body bias voltages (VBp, VBn) are used to control the delay of the current starved inverter, with VGn and VBn controlling the delay of the rising edge and VGp and VBp the delay of the falling edge. The body bias voltages act as additional fine-tuning knobs for the delay, with the gate voltages providing large tuning ranges.

Since the jitter measurement instrument targets SUTs up to a few GHz, the NT delay block must provide a SUT delay from hundreds of picoseconds up to several nanoseconds. This block is implemented as a cascade of equal delay elements which are designed using transistors of minimal size in spite of larger process and mismatch deviations with smaller sizes. The selection of a delay of N clock periods is done via a multiplexer that selects the required number of cascaded delay elements. As an example, considering delay cells made of two delay elements, for a 1 GHz signal and N=3, 15 delay cells biased with a typical delay of 200 ps each can be used, or 6 delay cells biased with a delay of 500 ps each. A lower number of delay elements will have less inherent noise, but it is necessary to consider also the sensitivity to the gate and body bias control voltage noise.

Fig. 3 shows post-layout simulations of the delay in the rising edge of a delay cell with two cascaded delay elements as a function of the gate and body bias voltages, VGn and VBn, respectively. Fig. 3(a) shows that the delay is more sensitive to gate voltage than body bias voltage. While gate voltages can be varied from 0 to 1 V (nominal supply voltage), the body bias voltage can be varied beyond the nominal supply voltage providing a wider range with precise control. For a delay of 200 ps, a value of VGn around 0.7 V can be used. For this value, Fig. 3(b) shows that delay variation with body bias control is almost linear with a sensitivity of about 20 fs/mV. The shifts due to process corners can easily be tuned with the body bias voltage, with a resolution which does not need to be better than 1mV. For VGn=0.7 V and VBn=-2.13 V that give a 200 ps delay in Fig. 3(a) in the typical case, the histogram in Fig. 3(c) shows the effect of mismatch deviations using a Monte Carlo simulation with 200 samples. A standard deviation of 10.9 ps and a mean value of 201.3 ps are obtained. This variation can be tuned with the body bias voltage, or the gate control voltage in case of extreme deviations.



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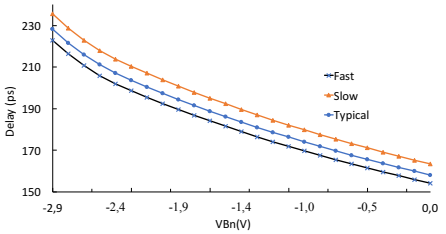

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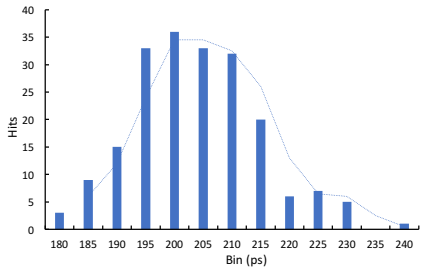

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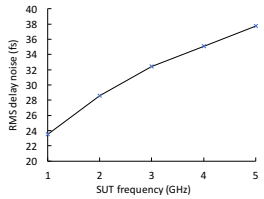


(d)

Fig. 3. Post-layout simulation of the 28 nm FD-SOI delay cell made of two cascaded delay elements. Rising edge delay variation as a function of body bias VBn for different values of the gate control voltage VGn (a), for VGn=0.7V under process corners (b), and for fixed VGn and VBn with mismatch deviations (c). (d) Output RMS delay noise of the typical single delay element.

The cascade of delay elements is calibrated for a given delay d by connecting all the delay elements to form a ring oscillator (RO). The oscillation period is given by $T_{osc}=2\,d$. If the period of the SUT is T_{in}, the target jitter resolution Δ must verify $\Delta>|T_{in}- T_{osc}|$. The RO is allowed to run for a sufficiently long duration T_m while a counter keeps track of the number N of RO cycles which needs to be in the range $N=[T_{osc}/\Delta-1, T_{osc}/\Delta+1]$ to meet the target resolution. For example, for a 1 GHz signal and Δ =100 fs, the value N=[9999, 10001] must be obtained for a measurement time of T_m=10 µs. This is the minimum time required for each step in this example for a tuning procedure that will adapt the voltage bias.

Fig. 3(d) shows the RMS delay noise at the output of one delay element obtained with a post-layout transient noise simulation of the nominal design. The noise bandwidth is set to $f_{max}=f$ and f_{min} is limited by the simulation time of 1000 SUT cycles used for the calculation of one bin histogram. As f increases, this inherent noise also increases but less delay elements are required in the NT delay block. The block must be biased so that the minimum number N of delay elements are used. Delay noise will also be due to noise via the bias voltages, but with a sensitivity of a few fs/mV, it is not expected to be larger than inherent noise. The calculated RMS delay noise at 1 GHz (24 fs) shows that it will be possible to reach the target resolution of 100 fs for signals working at several GHz with a single delay cell in the NT-delay. In addition, a delay element adds around 70 fs of RMS jitter per mV of power supply RMS voltage noise. The decoupling capacitors in the power supply have to be designed for sub mV power supply RMS voltage noise.

B. Vernier Delay Line

We consider next the implementation of the fine delay block in Fig. 1. As discussed in Section II, the delay of this block increases an amount Δ in each step, where Δ is the resolution of the jitter estimate. Conceptually, for each step in the scheme of Fig. 1, a precise delay calibration is required for obtaining one bin of the histogram. Rather than using a calibration of this delay in each step, in this work we will use a Vernier Delay Line (VDL) that allows the generation of the histogram bins with a simple calibration procedure.

As shown in Fig. 4(a), the VDL is made of two tapped delay lines, with each delay line composed in turn of delay cells. The VDL can be seen as made of a number of Vernier delay cells. The delay cell A is biased to give a delay of $\tau_A=\tau$, while cell B is biased to give $\tau_B=\tau+\Delta$. The delay d_i between the two tapped lines at the output of the i-*th* Vernier delay cell is no longer dependent on the delay of each individual delay cell, but rather on the delay difference Δ between two delay cells and the number of Vernier delay cells so that $d_i=i*\Delta$. With this, it is possible to obtain a delay resolution smaller than the delay of an individual delay cell.

The SUT and the sampling clock are fed at the two inputs of the VDL. The tapped outputs of the *i*-th Vernier delay cell are sent to a phase comparator. As a result, the SUT signal is sampled by the NT-delayed sampling clock with an additional delay $d_i=i\,\Delta$ added between both signals. For a given number of periods of the SUT signal, the number of hits at the output of the phase comparator is counted to give the value of the *i*-th histogram bin.

We use for the VDL the same delay cells as described in Section III.A. Uncorrelated mismatch deviations within a Vernier cell will affect the typical delay Δ added by each cell. It is not intended to calibrate each Vernier cell individually since this would require a large number of control and bias voltages. Instead, the delay cells of each tapped delay line are calibrated altogether, ensuring that the overall delay of the line meets the specifications. Each delay line of the VDL is configured as a RO and calibrated as discussed in Section III.A.

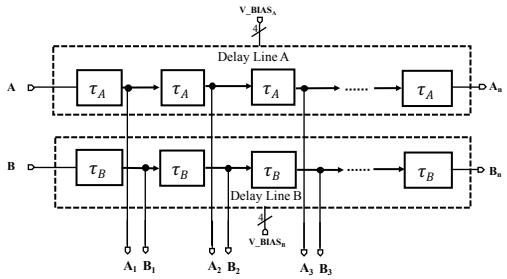
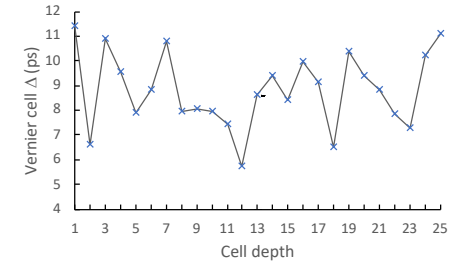
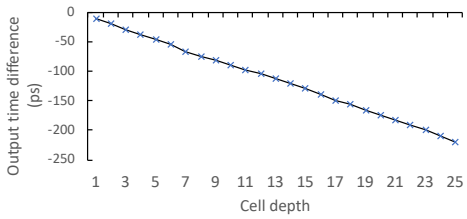


Fig. 4. Vernier Delay Line.



(a)



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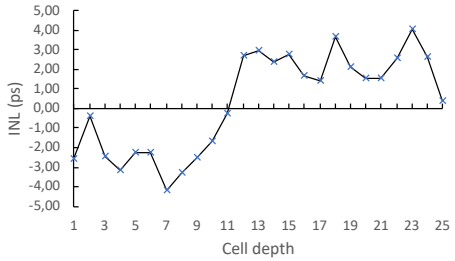


(c)

Fig. 5. VDL simulation at transistor-level in 28nm FD-SOI under process and mismatch deviations. As a function of cell depth for a random instance: (a) Δ of the Vernier cells, (b) time difference at the output of a Vernier cell, and (c) INL.

We consider a jitter histogram with 25 bins. Each of the 25 Vernier delay cells is built using exactly the same delay cells designed in Section III.A of minimum size. Bias voltages are equal for all delay cells in each delay line of the VDL. We have considered a VDL with Δ value of 10 ps and estimated the VDL variability and linearity with a Monte Carlo simulation with about 200 instances. A standard edge triggered D flip-flop as phase comparator at the output will respect set-up and hold time requirements. A nominal resolution of Δ=10 ps can be obtained by biasing delay cells A and B with VGn=0.7 V, VBn(A)=-0.36 V and VBn(B)=-1.97 V. The sensitivity to the bias voltages at these points is of 15 and 30 fs/mV for cells A and B, respectively. In order to use this VDL, we require to place at its input a Time Difference Amplifier (TDA) with a gain of 100 to guarantee Δ=10 ps/100=100 fs at the input of the TDA. For a random instance of the simulated VDL at transistor-level in 28 nm FD-SOI under process and mismatch deviations, Figs. 5(a), 5(b) and 5(c) give, as a function of the VDL cell depth, the variability of Δ, the time difference at the output, and the Integral Non-Linearity (INL) error, respectively. The average value of Δ is 8.8 ps with a standard deviation of 1.5 ps which referred to the input of the TDA results in 15 fs, below the delay noise level of a delay cell. The INL fluctuates between ±4 ps with a maximum linearity error about 2% referred to the full delay. For the whole set of Monte Carlo instances, these values do not vary significantly.

The typical time difference at the VDL output is 25x8.8=220 ps with a standard deviation of $1.5\sqrt{25} = 7.5$ ps. Since this is rather close to Δ=10 ps, the calibration of the VDL can enhance accuracy. The average delay for each delay cell in line A is 72.6 ps with a standard deviation of 2.78 ps. The total delay of delay line A will be d_A=72.6*25=1815 ps (with a standard deviation of $2.78\sqrt{25} = 13.9$ ps). The average delay for each delay cell in line B is 81.4 ps with a standard deviation of 2.03 ps. The total delay of delay line B will be d_B=81.4*25=2035 ps (with a standard deviation of $2.03\sqrt{25} = 10.1$ ps). Delay line A can be calibrated with a resolution of 1 ps by counting its oscillation cycles that must be in the range N_A=[2*d_A/Δ-1, 2*d_A/Δ+1]= [3629,3631] with a measurement time of T_A=N_A*2*d_A=13.177 μs. For delay line B, N_B=[4069,4071] with a measurement time of T_B=16.565 μs.

C. Time Difference Amplifier

In this work, we use the TDA described in Fig. 6(a) [12] which is an improvement of the one proposed in [13] with increased gain and range control. It is composed of two unbalanced SR latches. When two signals are almost simultaneously incident on an SR latch, the latch takes a longer time to come out of metastability. The latch finally settles its outputs in a state that depends on which signal advances the other at its inputs. This property is exploited to amplify the latch input time difference T_{Lin} into an output time difference T_{Lout}. As shown in Fig. 6(b) in a discontinuous trace, the characteristic gain function of a latch T_{Lout}=f(T_{Lin}) is symmetrical. The output tends to a large value when the input tends to 0, and to a small value for large absolute values of the input. The actual gain depends on the NAND gate transconductance during metastability and the output capacitance. By adding a time offset T_{off}, implemented by a chain of inverters, in opposite branches of the two latches, the gain characteristic of each latch is shifted in opposite directions as shown in Fig. 6(b) in continuous traces. The characteristic gain function of the TDA T_{out}=f(T_{in}) is shown in Fig. 6(c). It is just the difference of the characteristic gain functions of the two SR latches. The NAND outputs from the SR latches are fed to capacitors that help to further boost the gain of the TDA which should be operated in its linear region in the range [-T_{off}, T_{off}].

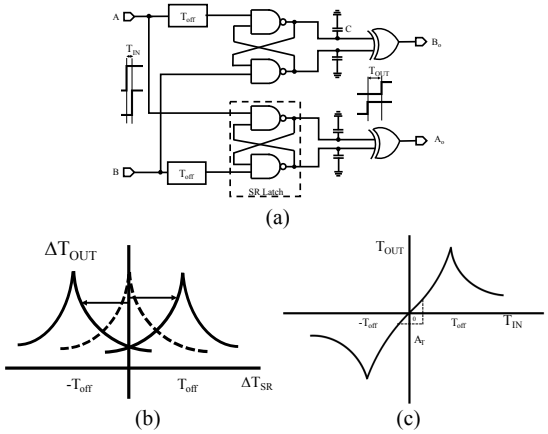


Fig. 6. TDA: (a) schematics, (b) conceptual gain characteristics of the two SR latches, and (c) conceptual gain characteristic of the TDA [12].

The TDA placed at the input of the VDL must guarantee a Δ of at least 100 fs. Fig. 7(a) shows the post-layout gain characteristic of the TDA in 28 nm FDSOI technology under process corners with an input range [-25,25] ps, which results in an output range about [-90,90] ps. The average gain is about 3.6. The worst-case INL can reach 13.9 ps giving a maximum nonlinearity of 15% referred to the output range. Since the gain must be about 100, four stages of this TDA must be cascaded. Fig. 7(b) zooms in the input range [-2.5,2.5] ps that guarantees 100 fs at the TDA input. There is no significant non-linearity in this range and the typical gain is about 2.5. Mismatches between latches and between capacitive loads result in a zero-output offset of a maximum of 250 fs. Since this is larger than the target Δ of 100 fs, this can result in a shift of the output histogram. This is easily corrected using the NT delay block.

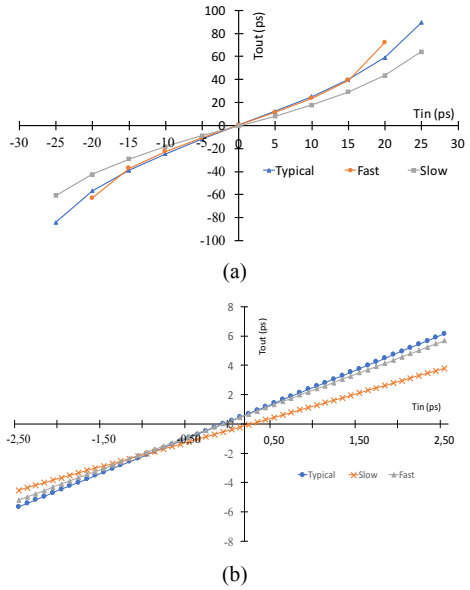


Fig. 7. Post-layout simulation under process corners of the gain characteristic of one stage of the 28 nm FD-SOI TDA for an input range of: (a) [-25,25] ps, and (b) [-2,5,2.5] ps.

The inherent noise of the TDA ultimately limits the resolution of the test instrument. Table I shows the equivalent RMS noise delay at the input of one TDA stage obtained with post-layout transient noise simulation of the nominal design. The test instrument will not be able to have a resolution better than this noise level which fits well with our target of 100 fs for GHz signals. Although noise increases with frequency, the gain of the stage also increases and input referred noise is steady. In addition, the TDA adds only around 10 fs of RMS jitter per mV of power supply RMS voltage noise.

TABLE I. EQUIVALENT INPUT RMS NOISE DELAY OF A TDA STAGE FOR THE TYPICAL DESIGN.

SUT (GHz)	RMS delay noise (fs)	Average stage gain	Input referred RMS delay noise (fs)
1	147	3.4	44
1.5	161	3.5	46
2	171	3.8	44
2.5	181	4.5	40
3	192	5.2	37

IV. TEST INSTRUMENT PROTOTYPE

The architecture of the prototype is shown in Fig. 8(a). The SUT signal is fed to the NT delay block composed of 15 delay cells which allow covering a large frequency range. All delay elements are identical, of minimal size, and controlled by 4 gate and bias voltages, two for the rising edges and two for the falling edges. N is defined by selecting the delay cell, in an expected range [1,8] which is sufficient for absolute jitter measurements as shown in [8]. A TDA made of 4 identical stages is connected between the selected output of the NT delay block and the input of the VDL. The output of any of the TDA stages can be selected as the input of the VDL.

The VDL is made of 25 stages. All delay cells are identical as those of the NT delay block. Here again, all delay elements are controlled by 4 gate and bias voltages. An edge-triggered D flip-flop is placed at the output of each VDL. A 25-to-1 multiplexer selects the output of one of these flip-flops to clock a 10-bit hit counter. Asynchronous binary counters have been implemented using T flip flops. Shift-registers implemented using D flip-flops are used for storing and transferring data.

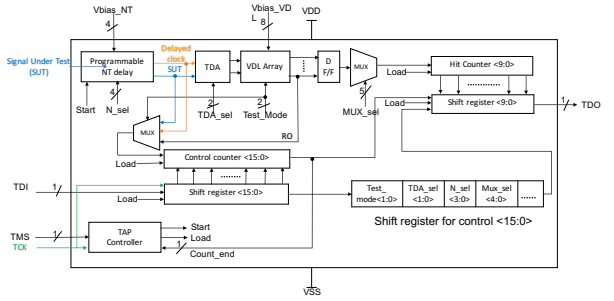
In the above discussion, only the rising edge control voltages have been considered for calibrating the NT delay and the VDL. However, if the falling edges do not vary, the duty cycle of the signals is affected and pulses at the output of the last stages of the TDA can disappear when time differences at the input of the Vernier cell are too large. It is thus required to adjust the duty cycle of the signals around 50% by controlling the falling edges also.

A control register is used to program the different operation modes which include the calibration of the NT delay, the calibration of the delay lines, the selection of the measurement bin, and the operations of shifting data in and out for instrument programming and readout. This is facilitated by a standard

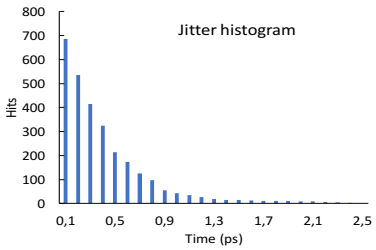
boundary scan test interface with a Test Access Port (TAP) controller. A 16-bit control counter is used to count RO cycles.

Fig. 8(b) shows the results of a noise transient transistor-level simulation of this instrument, considering a SUT at f=1 GHz with an RMS random jitter of 0.8 ps and 1500 SUT cycles for the measurement of each bin. This simulation includes a 5-stage NT delay (N=4), 4-stage TDA, 25-stage VDL and output flip-flops. The digital control circuitry is not included in the test bench. The calculated histogram of Fig. 8(b) results in an RMS jitter of 0.7 ps (after $\sqrt{2}$ correction for N=4) which fits well into the target resolution of 100 fs. Fig. 8(c) shows the layout of the main blocks with global routing.

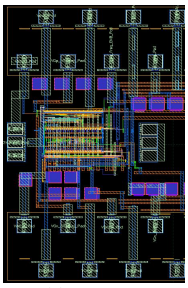
Table II compares this work with the state of the art. The size given in Table II for the full instrument corresponds to Fig. 8(a) without the TAP controller, while the minimum instrument includes a 1-stage NT delay, 4-stage TDA, 25-stage VDL and one output flip-flop.



(a)



(b)



(c)

Fig. 8. Prototype of the on-chip jitter measurement instrument: (a) architecture, (b) transistor-level noise transient simulation of the jitter histogram for a 1 GHz SUT with 0.8 ps RMS jitter, and (c) layout.

TABLE II. SELF-REFERENCED ON-CHIP JITTER MEASUREMENT

Ref.	Frequency (GHz)	Resolution (ps)	Area (mm^2)	Process
[9]	2.5 GHz	0.4 ps [(1)]	$3.2\ 10^{-3}$	130 nm
[8]	0.82 GHz	0.031 ps	$0.49\ 10^{-3}$	65 nm
[14]	5 GHz	≤1 ps	0.32	65 nm
[5]	6 GHz	0.31 ps	$15\ 10^{-3}$	65 nm
This work	1 GHz	<0.1ps [(2)]	$31\ 10^{-3}$ [(3)] $12\ 10^{-3}$ [(4)]	28 nm

[(1)] With external clean reference clock for calibration, [(2)] only simulation results, [(3)] full instrument, [(4)] minimum instrument.

V. CONCLUSIONS

This paper described an on-chip jitter measurement instrument designed in a 28 nm FDSOI process. The proposed design does not require an external clean clock, while back-bias voltages are employed to calibrate the instrument by compensating process and mismatch variations. Transistor-level simulation results show that 100 fs resolution can be achieved for GHz clock signals. The proposed test instrument is useful for applications such as technology qualification and PLL clock signal jitter monitoring.

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