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Enhancement of light extraction in 4H silicon carbide by nanostructuring the surface with high temperature annealing

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Silicon carbide (SiC) is a wide bandgap semiconductor with actual applications in power electronics due to its high thermal resistance, chemical stability and high critical electrical field [1]. However, SiC is also more and more studied for its applications in optoelectronics and nanophotonics, becoming a strong contender to conventional wavelength-conversion materials, such as phosphors, for the fabrication of white light emitting sources (LED) [2-3]. Indeed, fluorescent SiC (f-SiC), which is co-doped with donor-acceptor pairs (DAP) like nitrogen and bore or nitrogen and aluminum, presents a higher color rendering index and a longer lifetime compared to phosphor based LED [3]. More recently, it has been shown that SiC can also emit near infrared (NIR) light due to the excitation of color centers such as silicon vacancies, divacancies and nitrogen-vacancy centers [4-5]. However, one disadvantage of SiC for optoelectronic applications is its rather high refractive index (2.65 at 590 nm) compared to air. Due to that, the emitted light is totally reflected and stays trapped within the material which causes the low extraction efficiency of light of SiC [6-7]. To enhance the light extraction of SiC, nanostructuring of the material's surface has been done by various means such as e-beam lithography, nanosphere lithography, assembly of metal nanoparticles or reactive ion etching (RIE) [3-7].

In this work, we look to improve the extraction of light in 4H-SiC by changing the nanostructure of the SiC surface with the help of high temperature annealing by controlling the sublimation of Si in surface. The objective is to increase the surface roughness of 4H-SiC and thus, the reflection of the emitted light within the material decreases and its transmission through the SiC surface improves.

The samples we processed in this work are fabricated with off and on-axis n^+ -type doped 4H-SiC substrate on which were grown n^- , p^+ and p^{++} -type epitaxial layers (PIN diode structures). The off-axis SiC substrates are sliced with a 4° angle to the c -axis. Fluorinated ICP/RIE plasma etching was used to isolate the p -type zones of the surface (mesa structures) where we want to increase the roughness in order to extract the emitted light. After mesa etching, the p -doped layers of the samples were encapsulated with an AZ9260 photoresist and we used photolithography to remove the photoresist, creating windows where we want to nanostructure the surface. High temperature annealing process of 30 min plateau at different temperatures occurred then at 1700°C , 1600°C and 1500°C with a dedicated 6" RTP AET furnace with graphite resistors. For each temperature, photolithography is used on a different p -type top surface of the samples. The resin is removed by O_2 plasma ICP/RIE after each annealing and the samples are cleaned with Piranha and BHF solutions. After each annealing the samples have been analyzed by SEM FEG SU8030 Hitachi and Bruker Dimension Icon AFM.

Our results presented in Figure 1, show that the roughness of the zones which are not protected by the photoresist during annealing tends to increase with the annealing temperature. Nevertheless, the surface nanostructuring morphology differs from the samples with on and off-axis substrates (Fig. 2). The mass transport during Si sublimation at the highest annealing temperatures drives into a needle-shaped surface more pronounced for the off-axis samples. This surface state has a morphology similar to black-silicon [8] and thus expected to obtain interesting optical properties, with very low reflectivity and high absorption of visible (and infrared) light. When the annealing temperature decreases, these needles become larger and look more like peaks at an annealing temperature of 1500°C (Fig. 2). Close to the limit of the opened windows, a change of surface microstructure can also be observed as well as a light etching of the surface (Fig. 3.). The etching depth tends to increase with the temperature and when the temperature of annealing is too high (1700°C), the etching is strongly accentuated near from the limit of the opened windows.

At the conference and in the final paper, we will present in details these results completed with measurements of electroluminescence from PiN LED structures presented under these nanostructured surfaces.

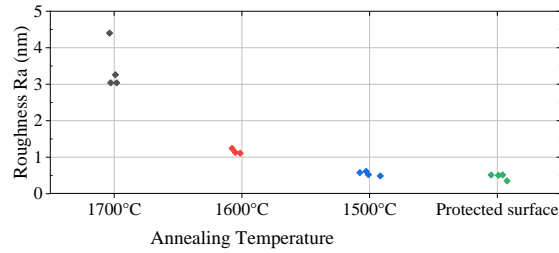


Fig. 1. Surface roughness (Ra) of the nanostructured patterns after annealing at different temperatures (1500°C, 1600°C and 1700°C) and of the protected surface of an off-axis 4H-SiC substrate with top epilayers. The protected surface is the surface covered by resin during annealing.

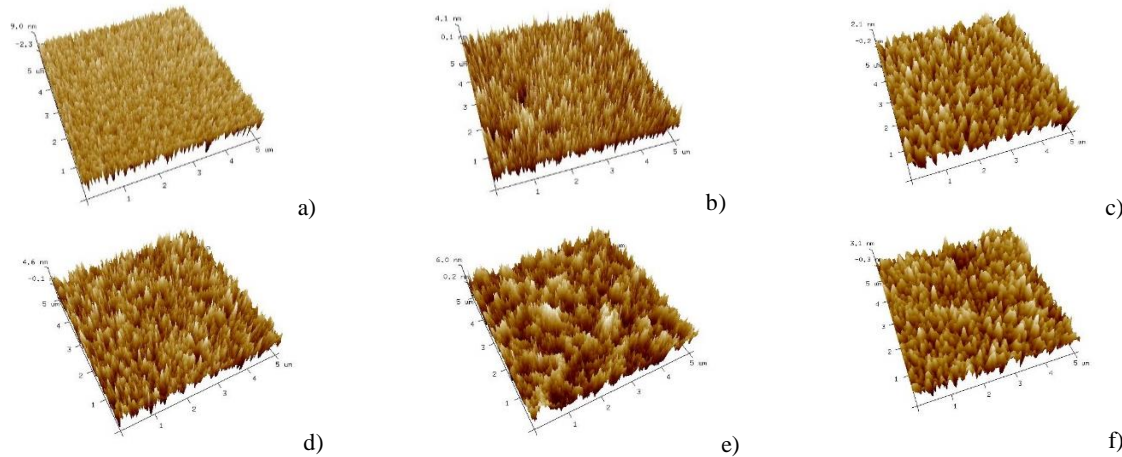


Fig. 2 Surface morphology obtained after high temperature annealing at 1700, 1600 and 1500°C (from left to right) on 4° off-axis ((a) to (c)) and on-axis ((d) to (f)) 4H-SiC substrates with top epilayers.

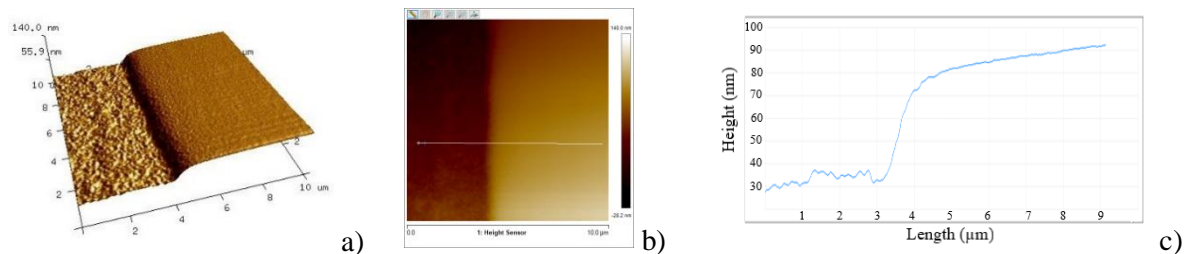


Fig. 3. AFM images of a 4° off-axis substrate with top epilayers. The limit between the nanostructured and the resin-covered zones after annealing at 1600°C is represented in a) 3D and b) 2D. c) Profile of the surface. The images were realized by Peak-Force mode.

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