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# High quality single crystal recrystallization of thin 4H-SiC films deposited by PVD techniques, a way for new emerging fields

E. Usureau<sup>1)</sup>, E. Vuillermet<sup>1)</sup>, M. Lazar<sup>1)</sup>, A. Andrieux<sup>2)</sup>, A. Jacquemot<sup>3)</sup>

<sup>1)</sup>Laboratory Light, Nanomaterials & Nanotechnologies, CNRS EMR 7004, University of Technology of Troyes, 12 rue Marie Curie, 10004 Troyes, France

<sup>2)</sup>Laboratoire Interdisciplinaire Carnot de Bourgogne (ICB), UMR 6303 CNRS, Université Bourgogne Franche-Comté, 21078 Dijon, France

<sup>3)</sup>MICROTEST, Z.A. La Garrigue du Rameyron, 84830 Serignan, France  
E-mail: mihai.lazar@utt.fr

Silicon carbide is a compound semiconductor material with particular physical and chemical properties, making it very attractive for power electronics applications and harsh environment systems and sensors. Bulk and homoepitaxial growth of SiC crystals requires specific reactors. 150-mm-diameter wafers are currently produced by seeded sublimation method at  $\sim 2300^\circ\text{C}$ , on which homoepitaxial growth of SiC is performed typically at  $1500\text{-}1650^\circ\text{C}$  by chemical vapor deposition [1]. The layers obtained with these sophisticated and specific techniques are difficult to be directly localized at the substrate surface and thus device fabrication with limited architectures needs post-growth plasma etching. In this paper we present high quality 4H-SiC layers obtained by more classic physical vapor deposition (PVD) techniques opening a way to design new SiC devices exploiting these PVD thin films for power applications and also other emerging fields, such as bio sensors, high temperature sensors, and optoelectronics or quantum nanophotonics.

Starting from a commercial 4°-off-axis 4H-SiC, we deposited amorphous SiC layers at room temperature (RT) and at  $750^\circ\text{C}$  by sputtering amorphous SiC target and by electron-beam evaporation techniques using an Elettrorava machine. The surface of the sample was cleaned by in-situ etching before deposition. In order to recrystallize the thin amorphous films (0.15 to  $1.5\mu\text{m}$  thicknesses), samples have been cut in pieces of  $25\times 25$  mm and annealing steps under Ar have been performed in a dedicated 150-mm AET RTP graphite resistive furnace (Fig.1) with a plateau at  $1400^\circ\text{C}$  and  $1700^\circ\text{C}$  during 30 min. Before the annealing at the highest temperature, the sample was encapsulated with an AZ photoresist, spin-coated on the both sides and pyrolyzed at  $750^\circ\text{C}$  under Ar in a second chamber (in quartz) of the AET furnace. The obtained graphite cap has been removed by plasma oxygen after RTP annealing. Before and after the RTP annealing the samples have been analyzed by Scanning Electronic Microscope (SEM) FEG SU8030 Hitachi and UV  $\mu$ Raman Spectroscopy ( $\lambda_{\text{ex}}=325$  nm) in back-scattering geometry with LabRAM HR Evolution from Jobin Yvon Technology. Finally, current-voltage measurements have been performed with a probe-station in order to test the electric conductivity in lateral and vertical configurations.

SEM images presented in Figure 2 correspond to the SiC surface obtained after  $1400^\circ\text{C}$  or  $1700^\circ\text{C}$  annealing (C-cap retired). The surface-state is homogenous with a slightly undulating grainy morphology typically found on recrystallized SiC amorphous layers created by high doses RT ion implantation [2]. The  $\mu$ Raman spectra (Fig. 3) prove that the post-annealed PVD layers get 4H-SiC crystallinity with polytype substrate replication, the LO and TO peaks corresponding to the 4H-SiC polytype. This denotes a solid phase epitaxy from the PVD layer/substrate interface. We used UV laser excitation (our lowest set-up wavelength) in order to limit the penetration depth of the laser within the PVD layer in surface. For the crystallized PVD layers deposited at high temperature ( $750^\circ\text{C}$ ) we obtained an epitaxial quality (Fig. 3a) with an annealing temperature as low as  $1400^\circ\text{C}$ . The decrease of the LO peak after the annealing at  $1700^\circ\text{C}$  is probably due to the dopant activation.

High n-type conductivity is obtained on the PVD layers deposited by sputtering, as Figure 4 shows with electrical measurements, both in lateral and vertical configurations. As the tungsten tips are put directly on the SiC surface without metal electrodes, the linearity of the I-V curves gives evidence for the high doped layers we obtained. This high conductivity is not found on the e-beam layers, which is explained by the higher vacuum level with lower impurity incorporation during this process.

In the final paper and at the time of the conference we will provide more details about our results, complemented with tests on ohmic contacted metallized structures.



Fig. 1. 150 mm AET furnace for this study: RTP chamber with graphite resistors (a), pyrolyzed quartz chamber (b) and typical temperature and Ar pressure profiles for the RTP 1700°C 30 min plateau.

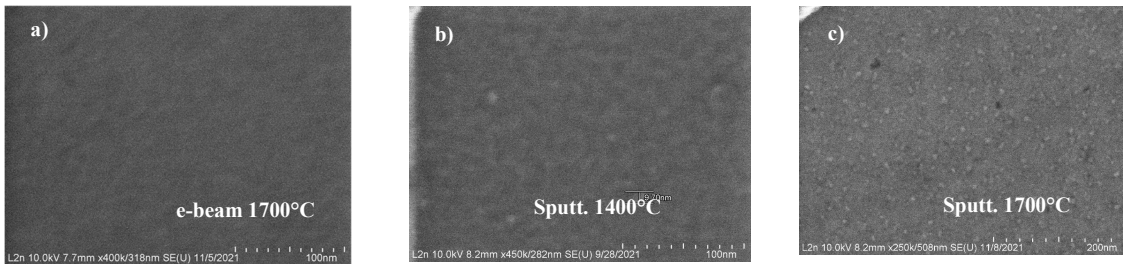


Fig. 2. SEM images from the PVD layers after recrystallisation (C-cap removed by O<sub>2</sub> plasma) : SiC e-beam deposited at 750°C and annealed at 1700°C/30 min (a), SiC sputtered at RT and annealed at 1400°C/30 min (b) and 1700°C/30 min (c).

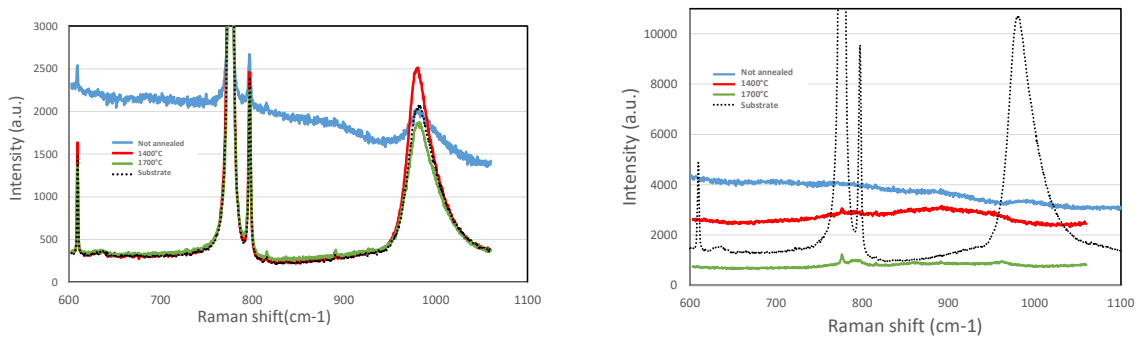


Fig. 3. UV Raman spectroscopy at 325 nm from PVD layers before and after annealing compared to initial 4H-SiC substrate: SiC e-beam deposited at 750°C (a) and SiC RT sputtered layers (b)

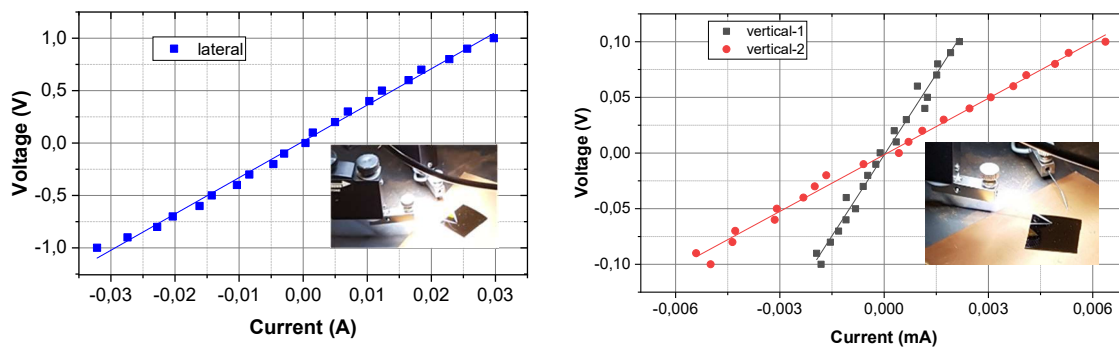


Fig. 4. Current-voltage measurements performed on the SiC RT sputtered layers and crystallized with 1700°C/30min annealing: in lateral configuration with both tips on the sample surface (a) and in vertical configuration (b). Optical images from measurement set-up are inserted.

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