Fault blocking capability in the DC-MMC with reduced number of submodules

Juan David Paez, Florent Morel, Seddik M Bacha, Piotr Dworakowski

Fault blocking capability in the DC-MMC with reduced number of sub-modules

J. D. Páez[1], F. Morel[1], S. Bacha[1,2], P. Dworakowski[1]

[1]SuperGrid Institute
23 Rue de Cyprian
69100 Villeurbanne, France
juan.paez@supergrid-institute.com
https://www.supergrid-institute.com/

[2]G2ELab
Univ. Grenoble Alpes, CNRS, Grenoble INP*
21 Avenue des Martyrs
38000 Grenoble, France
http://www.g2elab.grenoble-inp.fr/
*Institute of Engineering Univ. Grenoble Alpes

Acknowledgements

This work was supported by a grant overseen by the French National Research Agency (ANR) as part of the "Investissements d'Avenir" Program ANE-ITE-002-01.

Keywords

«HVDC», «Modular Multilevel Converter», «DC-DC converter», «Multi-terminal HVDC».

Abstract

The capability of DC-DC converters to block DC faults is an important issue for the development of HVDC grids. To include such feature, converters are generally oversized in terms of components by adding more semiconductors than needed in normal operation. This paper proposes to use a main switch instead of adding sub-modules in the topology to provide fault blocking capability. A converter control method is proposed to open the switch at zero current; thus, no breaking capability is required. An analysis on the impact on the converter design and a comparison with the classical solution are done. The operation of the proposed solution is verified through transient simulations. In the analysis, the requirements in terms of opening time for the switch were determined to be around 1 ms to 6 ms, which is feasible with a fast disconnector. However, the required control to keep the current on the switch at zero amps adds constraints to the lower arms of the topology in terms of installed capacitance and current withstanding.

Introduction

DC-DC converters are needed to enable the development of future HVDC grids. These structures allow the interconnection of DC systems with different characteristics like voltage rating or line configuration [1]. While enabling the interconnection of DC systems, DC-DC converters can also provide several functionalities to the system, like power flow control, DC voltage regulation and fault blocking capability (FBC) [2]. This last characteristic makes that DC-DC converters can play a role in the protection strategy of DC networks [3].

The FBC can be understood as the capability of the converter to prevent the apparition of anormal voltages or currents in one of the DC systems being interconnected by the converter when a fault appears in the second DC system. Anormal voltages and currents are defined as values that could lead to stop the operation of the network or to damage some of its components. This feature is achieved by liming the contribution of the healthy system to the fault current. The FBC can be achieved by a DC-DC converter integrated with an external protection device like a DC circuit breaker (DCCB), or by a DC-DC converter designed to provide the functionality by controlling the contribution of the heathy system to the fault current or being capable of interrupting this current.

Several DC-DC topologies adapted to HVDC applications have been proposed in literature. The common trend are modular multilevel converters that use chains of sub-modules (SMs) [2]. The SMs can be of different types, the half-bridge (HB) and the full-bridge (FB) being the most common. Two main categories of DC-DC converters are identified: isolated and non-isolated circuits. Non-isolated topologies seem to be more competitive in term of losses and component count [4], but they do not provide inherent FBC as the isolated circuits do. The non-isolated converters generally need some modifications in the structure to provide the FBC, like the use of FB-SMs instead of HB-SMs.

Among the non-isolated topologies, the DC-MMC has been identified as an interesting solution [4]–[8]. In this circuit, the FBC is provided by adding more SMs compared to those needed for normal operation [9]. This leads to an increase on the losses and costs, which can reduce the interest of the topology. This paper proposes an alternative solution to include the FBC.

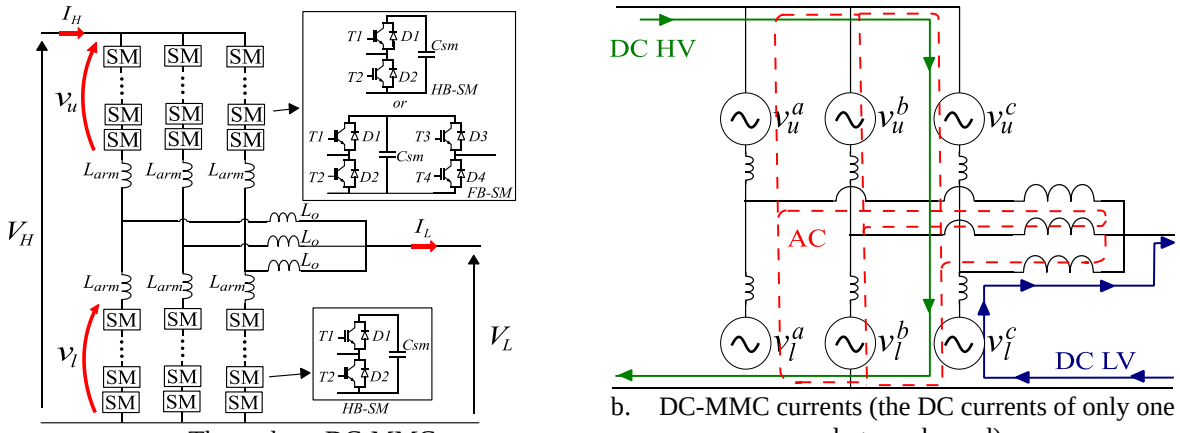
The solution proposed in this paper relies in the use of a main high voltage switch (HV-Sw) instead of SMs to include the FBC against faults on the low-voltage side. A converter control method is proposed during faults to operate the HV-Sw at zero current. The aim is to reduce the constraints of the switch in terms of breaking capability.

The paper is organized in three sections. In the first section the DC-MMC topology is introduced and the constraints in terms of number of SMs to provide FBC are presented. The second section presents the proposed solution and the proposed control during faults. Finally, the third section presents the validation of the solution in simulation as well as a sensitivity analysis on the converter sizing and the constraints to the proposed HV-Sw. A comparison of the converter losses in the proposed solution and the classical DC-MMC is also done.

The DC Modular Multilevel Converter

The DC-MMC (also known as M2DC) (Fig. 1) is a non-isolated converter formed by several legs connected in parallel to the HV DC system. Each leg is formed by two arms made by a stack of SMs and an inductor. The legs have a middle point which interconnects both arms. On this middle point a filter interconnects the LV side DC system. The simplest filter is an inductance. In this paper a three-phase DC-MMC is studied.

The operation principle of the circuit is to use the SM stacks as controllable voltage sources by acting on the insertion and bypass of the SM capacitors. AC and DC voltages are produced on the SM stacks, and thanks to the voltage drop that is generated on the converter inductors, AC and DC currents are controlled. The DC currents control the power flow between DC systems while the AC currents are used to balance the energy in the converter, i.e. to control the voltage on the SM capacitors, by exchanging energy between upper arms and lower arms for instance. The balanced operation between the legs makes that the AC currents circulate between arms and legs but not into the DC ports.



a. Three phase DC-MMC

b. DC-MMC currents (the DC currents of only one leg are showed)

Fig. 1: The DC-MMC and its operation principle with DC and AC circulating currents

In normal operation, each arm generates a maximum voltage described by Eq. (1) and Eq. (2) [9] which leads to the number of SMs per arm that would be required for normal operation which is shown on Eq. (3) and Eq. (4), where V_{SM} is the nominal voltage of one SM.

$$v_{u_{max}} = V_H - V_L + \min(V_L, V_H - V_L) \quad (1)$$

$$v_{l_{max}} = V_L + \min(V_L, V_H - V_L) \quad (2)$$

$$N_{SM\,u_{normal}} = \text{ceil}\left(\frac{v_{u_{max}}}{V_{SM}}\right) \quad (3)$$

$$N_{SM\,l_{normal}} = \text{ceil}\left(\frac{v_{l_{max}}}{V_{SM}}\right) \quad (4)$$

For HV side faults, to provide the FBC, the upper arms should generate a voltage equal to -V_L. For LV side faults, they should withstand V_H. Thus, the number of SMs required in upper arms to provide FBC are defined by Eq. (5) and Eq. (6) [9].

$$N_{SM\,FB_u} \geq \text{ceil}\left(\frac{V_L}{V_{SM}}\right) \quad (5)$$

$$N_{SM\,HB_u} \geq \text{ceil}\left(\frac{V_H}{V_{SM}}\right) - N_{SM\,FB_u} \quad (6)$$

Comparing Eq. (3) and Eq. (4) with Eq. (5) and Eq. (6) it is seen how FBC leads to oversize the upper arms for transformation ratios less than 2 (defining the transformation ratio as the ratio between the HV and LV DC voltages, i.e . $n_{dc} = V_H/V_L$). This means that, that the upper arms require FB-SMs and more HB-SMs compared to the normal operation requirements. For the lower arm the number and kind of SMs to provide FBC is the same that for normal operation. Therefore, The DC-MMC has to be oversized on the upper arms to provide FBC [9]. This oversizing is presented in Fig. 2.

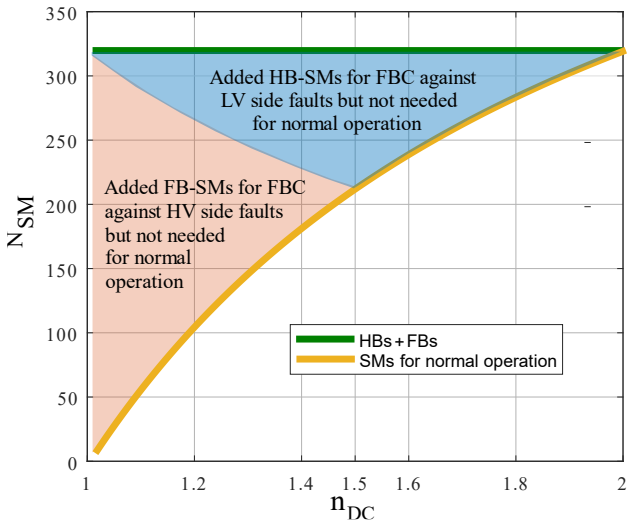


Fig. 2: Number of SMs required on each upper arm for normal operation and to provide FBC. A DC system voltage of $V_H = 640\ kV$ and SM voltage of $V_{SM} = 2\ kV$ were assumed as an example.

As an example, from Fig. 2, for $n_{dc} = 1.2$ ($V_L = 533$ kV) the required number of SMs for an operation in normal conditions is 107 per upper arm, all of them are HB-SMs. To include the FBC against HV side faults, the number of SMs per upper arm increases to 267 and must be of FB-SM type (Eq. (5)). To include the FBC against LV side faults, in addition to these SMs, 53 HB-SMs must be added (Eq. (6)). Thus, in total to include FBC for both types of faults the number of SMs per upper arm increased from 107 HB-SMs to 320 SMs (267 FBs+53 HBs). Considering that there are three upper arms, the oversizing is considerable. From Fig. 2, it is also observed that for $n_{dc} > 2$ there is no oversizing to include FBC.

The oversizing for the cases of $n_{dc} < 2$ degrades the performance indicators of the topology such as losses, number of switches and semiconductor utilization factor [9].

The use of a HV-Sw to avoid adding HB-SMs

To provide FBC without adding HB-SMs that are not necessary in normal operation on the upper arms, it is proposed to use an external switch HV-Sw between the HV side and the upper arms as shown in Fig. 3 [10]. This switch replaces the added HB-SMs on the upper arms to provide FBC against LV side faults. For HV side faults, the use of FB-SMs is still required as the proposed solution does not rely on a DCCB. During normal operation the switch is closed, and it is open only when there is a fault on the LV side.

Since breaking a DC current requires a circuit breaker, which is a costly solution, it is proposed to open the HV-Sw at zero current. To achieve this, a control method of the converter during the fault is proposed. With this approach it is expected that the requirements of breaking capability for the HV-Sw would be decreased and then a cost-effective solution like a disconnector could be used.

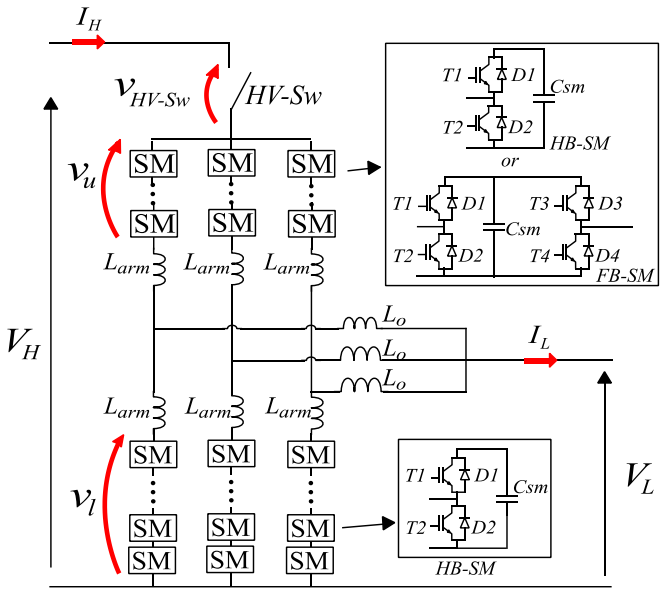


Fig. 3: DC-MMC with external HV-Sw to provide FBC against LV faults.

Reduction of number of SMs and losses

Fig. 4 shows the number of SMs (FBs and HBs) required on each upper arm in function of the transformation ratio for the classical DC-MMC as well as those needed with the proposed solution. It is observed how with the proposed solution, the number of HB-SMs needed in the topology to provide FBC is reduced. In the figure, the savings in SMs per upper arm are presented. For $n_{dc} = 1.5$ the solution gives the maximum reduction on SMs.

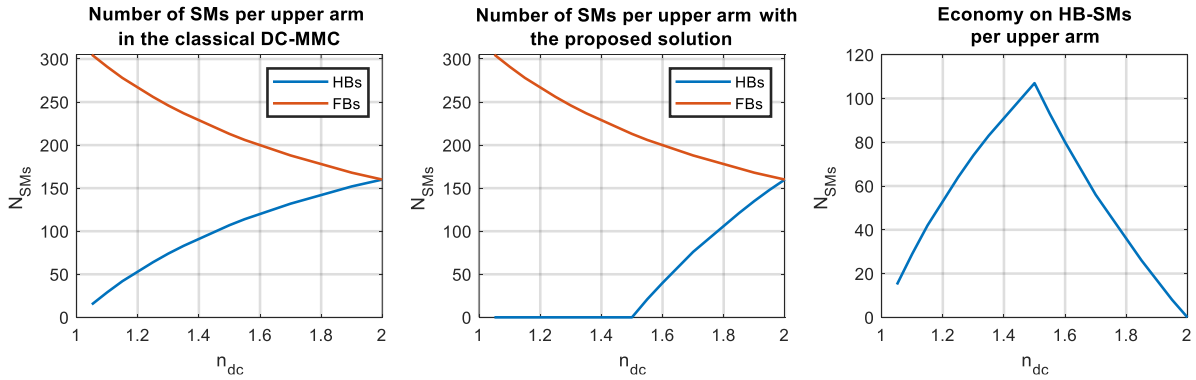


Fig. 4: Number of SMs per upper arm on the classical DC-MMC, in the proposed solution and the economy of HB-SMs for the proposed solution. A DC system voltage of $V_H = 640\ kV$ and SM voltage of $V_{SM} = 2\ kV$ were assumed as an example.

Since the conduction losses in a mechanical disconnector are lower than in the semiconductors of the removed SMs and because the current seen by the HV-Sw is only the DC current, contrary to the

classical solution where the added SMs in the arms see the DC current and the circulating AC currents, it is expected that the proposed solution leads to an overall reduction on the conduction losses.

In addition, because the HV-Sw is kept closed during normal operation contrary to the classical solution where the added HB SMs are switching permanently to keep balanced the energy in the SM capacitors, it is expected that the proposed solution leads as well to a reduction on switching losses

In the section of validation of the proposed solution, the losses are quantified.

Proposed control

In order to open the HV-Sw at zero current it is proposed to use the lower arms to control the DC current on HV side after a LV side fault. The proposed control scheme is based on the following steps:

1. LV side fault detection by a measurement of the voltage drop, the rise of the DC current (di/dt) or by overcurrent.
2. Blocking of all SMs in the upper arms by turning OFF all IGBTs in the SMs.
3. Control of the lower arm SMs to generate the highest possible DC voltage by inserting all the SM capacitors.
4. When the current on each of the upper arms is zero, the corresponding lower arm in the same leg is controlled to maintain the current at zero amps.
5. When the current in all upper arms is zero (the DC current on the HV side is also zero), the HV-Sw is opened at zero current. The opening time depends on the HV-Sw technology.
6. When the HV-Sw is totally opened, (which can be verified by the voltage at its terminals), all the SMs in the lower arms are blocked.

The proposed control relies in the energy stored on the lower arms SMs to control the current. Since the lower arms still operate during the fault, the output inductances play an important role to decrease the fault current circulating by the arms.

In the following section the proposed control approach is validated, and a sensitivity analysis on the output inductor and SM capacitors is done.

Validation of the proposed solution in simulation

Control validation

To validate the proposed solution, simulations are done in Matlab/Simulink using the SimPowerSystems Toolbox. A case study based on the values of Table I is proposed. To model the circuit, an average model including the blocked state is used per arm as shown in Fig. 5. These models were proposed in [11], [12]. In these models, the SM stack is replaced by equivalent voltage and current sources, and all SM capacitors by an equivalent capacitor Ceq. IGBTs and diodes are added into the model to simulate the blocked state according to the blocking signal of the arm Blk.

The value of the equivalent capacitor depends on the number of SMs on the arm and the SM capacitance:

$$Ceq = \frac{C_{SM}}{N_{SM}} \tag{7}$$

The voltage at the terminals on this capacitor represents the sum of the voltages of all the SMs in the arm.

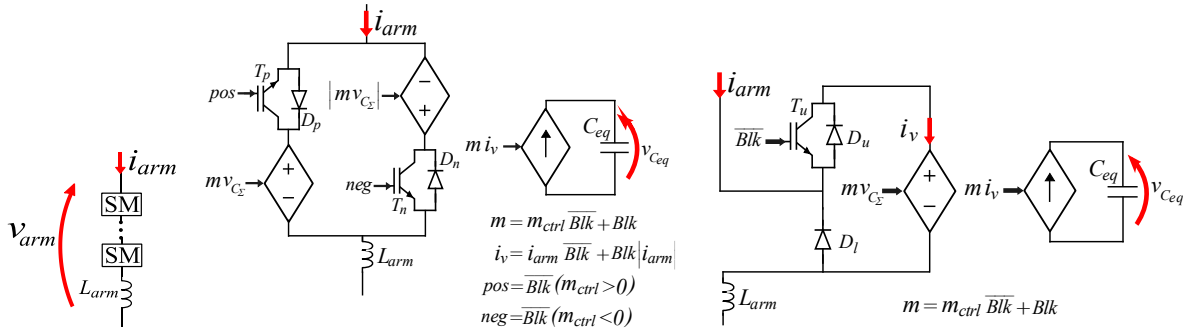
The blocking signal is a boolean and is calculated by the controller of the converter. The modulation index m is also used on the models. This variable represents the percentage of SMs being inserted at a given moment. It is calculated by the controller of the converter. The details of converter control during normal operation are omitted here for simplicity, but the reader can find more details about the control the converter in [5]. The focus of the paper is the proposed algorithm after the fault.

Table I: Circuit parameters for DC fault simulations

Parameter	Value
DC voltage	640 kV (HV side) and 500 kV (LV side)
Nominal Power	700 MW
Operating frequency	150 Hz

SM capacitance (sized to have an acceptable SM voltage ripple during normal operation at nominal power)	2.8 mF (Upper arms) and 10 mF (Lower arms)
Number of SMs per arm	313 FBs (Upper arms) and 400 HBs (Lower arms)
SM nominal voltage	2 kV
Arm inductance	25 mH
Filter inductance	250 mH

In the simulation, a LV side fault is done at the converter terminals at t=0.8 s, at nominal power, then the different stages of the proposed control are executed. It is assumed that there is no delay between the detection of the fault and the start of the control algorithm. The fault detection is done by undervoltage and overcurrent measurements at the converter terminals. The controller time step is 40 µs. Fig. 6 presents the simulation results. Only the variables related to one of the converter legs are presented for clarity (except for the voltage on the equivalent arm capacitance and the lower arms currents that are presented for the three legs). The figure highlights the different control steps described in the previous section. A delay of 1.5 ms is assumed on the opening of the HV-Sw, between the trigger signal and the effective switch opening.



a. A generic Arm

b. Average model of an arm made of FB-SMs used for the upper arms

c. Average model of an arm made of HB-SMs used for the lower arms

Fig. 5: Simulation models of an arm used to model the DC-MMC.

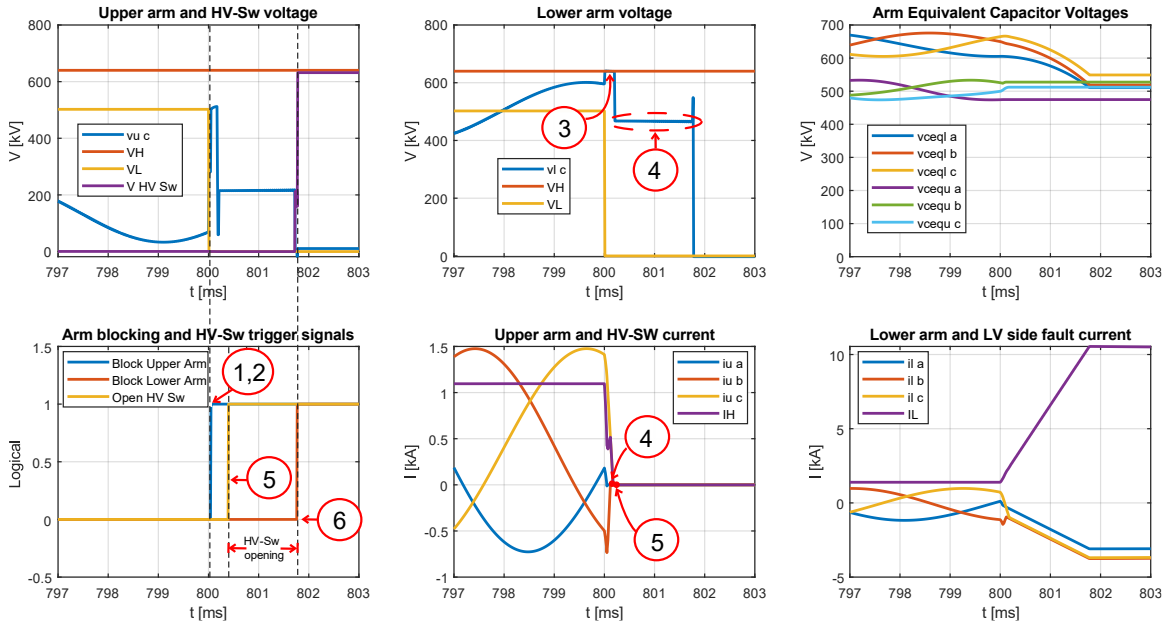


Fig. 6: Simulation results highlighting the control steps (1 to 6). The LV side fault is done at t=800ms

From the simulation results it is seen that effectively the opening of the HV-Sw (t=801.76 ms) is done at zero current. The control scheme achieves to maintain the I_H current on the switch at zero amps during all the opening. Once the switch is totally open, it is seen that the HV voltage is withstood by the HV-Sw and not by the FB-SMs on the upper arm.

According to the simulation results, during the transient, the high-side current I_H did not reached unacceptable values. Thus, the FBC is demonstrated.

In the figure it is also observed that, to keep controlled the HV current at zero during the opening of the HV-Sw, the lower arm should generate a voltage which feeds the LV fault. Thus, the SM capacitors are discharged into the LV side fault and the fault current increases. This is evidenced by the decrease of the capacitor voltage and the increase on the lower arm currents. This phenomenon poses two constraints to the proposed solution. From one side, if the capacitor voltages are discharged below the required voltage to control the upper arm currents, the control is lost and it is not anymore possible to regulate the HV current. From the other side, the current increase on the lower arms poses a constraint in the sizing of the semiconductor current rating. If the HV-Sw opening is too long, any of both situations will appear: the lower arm SM capacitors will be discharged below the control limit or the currents on the lower arms will reach unacceptable values.

Sensitivity analysis

An analysis of the maximum time to open the HV-Sw at zero current was done in function of the sizing of the converter. Two parameters were varied: the lower arm SM capacitance and the filter inductances *Lo*. The results are presented on Fig. 7. The maximum time before losing the control is presented as well as the current on the lower arms at that moment. For example, for a design with *Lo*= 250 mH and *Csml*= 10 mF the maximal time is around 3.5 ms and the lower arms must withstand a current of 6 kA.

The times presented on Fig. 7 are calculated as the time between the fault and when the current I_H cannot be longer controlled. Thus, this time represents the maximum time to open the switch including the fault detection, processing, triggering, and switch opening.

Fig. 7 shows that the technology of the HV-Sw must be capable of opening in some milliseconds, which can be done with a fast disconnector [13]. The increase on the SM capacitors can increase the available time to open the switch, but as a consequence the lower arms should withstand more current. Increasing the filter inductance can help to decrease the current rating and provide more time to open the HV-Sw.

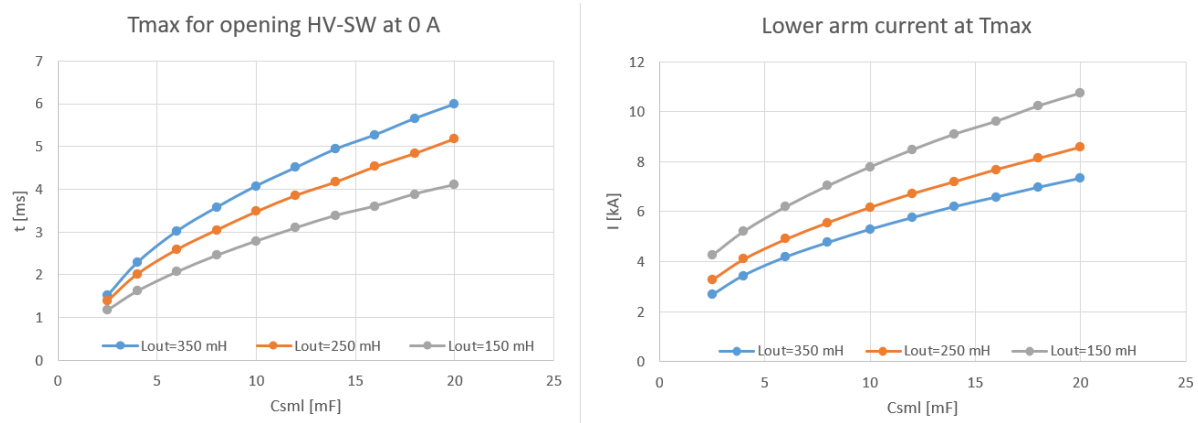


Fig. 7: Maximal time before losing the control at zero amps on the HV-Sw and current on the lower arms at that time in function of the lower arm SM capacitance and output filter inductance.

Power losses analysis

In this section, the losses of the proposed solution are compared with the losses of the classical DC-MMC. Only the semiconductor losses are considered. To calculate the conduction and switching losses, a semi-analytic detailed model of the converter is built. In this model the equivalent current source and equivalent capacitor used in the average models (Fig. 5) are replaced by a set of equations that represent the behavior of the individual SMs. The details of this modelling technique can be found in [14]. In these simulations, it assumed that the ac voltages are the same for a converter with or without FBC (even if a converter with FBC has additional SMs and then can generate different ac voltages).

From the simulation, the arm currents are extracted as well as the control signals of each SM. With this data, it is possible to establish which semiconductor is conducting at each time and to detect the switching actions (bypass or insertion of a SM). Then it is possible to establish the RMS and average currents per device as well as the switched current.

The conduction losses are estimated by Eq. (8) where V_o represents the saturation voltage if the switch is an IGBT or the threshold voltage if it is a diode, R_{ON} represents the device equivalent resistance in the ON state, I_{RMS} the device RMS current, I_{AVG} the device average current.

$$P_{conduction} = I_{RMS}^2 R_{ON} + I_{AVG} * V_o \tag{8}$$

The switching losses are calculated with Eq. (9), where $a_{on,off,rec}$, $b_{on,off,rec}$ and $c_{on,off,rec}$ are coefficients that approximate the energy loss at each switching of the device by a polynomial regression in function of the switched current I_{sw}. The power losses are calculated by adding all the energy losses and dividing by the elapsed time.

$$P_{switching} = \frac{1}{T_{total}} \sum \left(a_{on,off,rec} + b_{on,off,rec} * i_{switched} + c_{on,off,rec} * i_{switched}^2 \right) \tag{9}$$

The parameters R_{ON}, V_o, $a_{on,off,rec}$, $b_{on,off,rec}$ and $c_{on,off,rec}$ are obtained from the device datasheet. In this paper a 3.3 kV / 1500 A power module is assumed (FZ1500R33HL3).

For the simulation, a low-level controller was added to control the switching of each SM. The choice was a Nearest Level control modulation with a Balancing Control Algorithm (BCA) based in a tolerance band as described in [15]. The tolerance band was set to 180 V. The control of the FB-SMs in the structure does not consider a negative insertion.

The simulation is done during a long period of time (9 seconds) to average the "random" switching phenomena caused by the BCA. The data of one SM on the upper arms and one SM on the lower arms was recorded to do the post-processing. The losses are calculated for different scenarios. As base values, the parameters of Table I are used, Table II presents those parameters which are changed in comparison with the previous case.

Table II: Parameters for simulations for the calculation of power losses

Parameter	**Value**				
LV side DC voltages	533 kV	457 kV	427 kV	400 kV	356 kV
Ndc	1.2	1.4	1.5	1.6	1.8
Number of SMs (FBs) per upper arm	334	286	267	250	223
IGBT Losses parameters	$R_{ON} = 0.94\ \text{m}\Omega$, $V_o = 1.5\ V$, $a_{on} = 0.5435$, $b_{on} = 0.9946x10^{-3}$ and $c_{on} = 5.7705x10^{-7}$ $a_{off} = 0.2929$, $b_{off} = 1.7079x10^{-3}$ and $c_{off} = 0.4486x10^{-7}$				
Diode Losses parameters	$R_{ON} = 0.43\ \text{m}\Omega$, $V_o = 1.2\ V$, $a_{rec} = 0.5706$, $b_{rec} = 2.8654x10^{-3}$ and $c_{rec} = -7.2667x10^{-7}$				

Fig. 8 shows the power losses of the proposed solution compared with the classical DC-MMC. It is verified that the proposed scheme reduces the converter power losses. The reduction is mainly on the switching losses. The reduction on conduction losses is lower and increases with the transformation ratio n_{DC}. The conduction losses are still penalized by the high amount of FB SMs required on the upper arms to provide FBC against HV side faults.

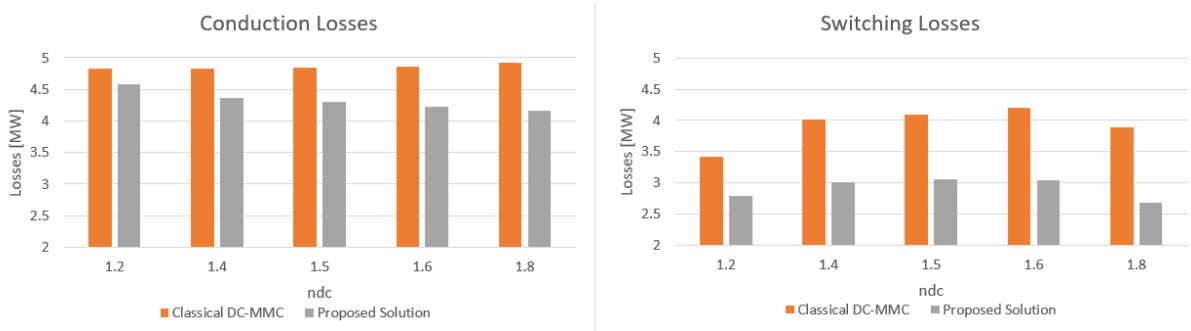


Fig. 8: Semiconductor losses comparison between the proposed solution and the classical DC-MMC.

Conclusions

An alternative method for providing FBC on the DC-MMC is proposed in this paper. The method is based on the use of an external switch. With the proposed solution, a decrease in the number of installed SMs is achieved and as well as a decrease in power losses. A control method was proposed to operate the switch at zero current. This avoids the need of breaking capability on the switch. Thus, it can be implemented with a fast disconnector. The operation of the switch and the control method was verified in simulation. A sensitive analysis on the circuit parameters was done to analyse the maximum opening time of the switch. It is seen that the HV-Sw must operate in some milliseconds and that the lower arms must withstand the fault current. The opening time of the HV-Sw is related to the maximal current that the semiconductors in the lower arms must be able to switch and to the minimal SM capacitance in lower arms. Thus, the proposed solution reduces the number of SM in the upper arms but, according to the HW-Sw performance, can lead to oversize the lower arm SMs. Finally, the proposed method can provide FBC against LV side faults but for HV side faults the DC-MMC is still oversized by the need of FB-SMs.

References

[1] D. Gómez, J. D. Páez, M. Cheah-Mane, J. Maneiro, P. Dworakowski, O. Gomis-Bellmunt, and F. Morel, "Requirements for interconnection of HVDC links with DC-DC converters," in *IEEE 45th Annual Conference of the Industrial Electronics Society (IECON 2019)*, 2019.

[2] J. D. Páez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of DC–DC converters dedicated to HVdc grids," *IEEE Transactions on Power Delivery*, vol. 34, no. 1, pp. 119–128, 2019.

[3] J. D. Páez, J. Maneiro, D. Frey, S. Bacha, A. Bertinato, and P. Dworakowski, "Study of the impact of DC-DC converters on the protection strategy of HVDC grids," in *15th IET International Conference on AC and DC Power Transmission (ACDC 2019)*, 2019, pp. 1–6.

[4] J. D. Páez, J. Maneiro, S. Bacha, D. Frey, and P. Dworakowski, "Influence of the operating frequency on DC-DC converters for HVDC grids," in *2019 21th European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019.

[5] F. Gruson, Y. Li, P. Le Moigne, P. Delarue, F. Colas, and X. Guillaud, "Full State Regulation of the Modular Multilevel DC converter (M2DC) achieving minimization of circulating currents," *IEEE Transactions on Power Delivery*, 2019.

[6] D. Jovcic, P. Dworakowski, G. Kish, A. Jamshidi Far, A. Nami Abb, A. Darbandi, and X. Guillaud, "Case Study of Non-Isolated MMC DC-DC Converter in HVDC Grids," in *CIGRE Symposium 2019 - Aalborg, Denmark*, 2019.

[7] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel DC/DC converter with fault blocking capability for HVDC interconnects," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 148–162, 2015.

[8] S. Norrga, L. Ängquist, and A. Antonopoulos, "The polyphase cascaded-cell DC/DC converter," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 4082–4088.

[9] J. D. Paez, F. Morel, S. Bacha, P. Dworakowski, and D. Frey, "Impact of DC fault blocking capability on the sizing of the DC-DC Modular Multilevel Converter," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. 1–10.

[10] J. D. Paez Alvarez, J. Maneiro, P. Dworakowski, S. Bacha, D. Frey, and F. Morel, "DC-DC VOLTAGE CONVERTER PROVIDED WITH A CIRCUIT BREAKER DEVICE," WO2021/1221872021.

[11] F. Xinkai, Z. Baohui, and W. Yanting, "Fast electromagnetic transient simulation models of full-bridge modular multilevel converter," in *2016 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, 2016, pp. 998–1002.

[12] H. Zhang, D. Jovcic, W. Lin, and A. J. Far, "Average value MMC model with accurate blocked state and cell charging/discharging dynamics," in *Environment Friendly Energies and Applications (EFEA), 2016 4th International Symposium on*, 2016, pp. 1–6.

[13] R. Derakhshanfar, T. Jonsson, U. Steiger, and M. Habert, "Hybrid HVDC breaker–Technology and applications in point-to-point connections and DC grids," in *CIGRE session*, 2014, pp. 1–11.

[14] A. Zama, S. Bacha, A. Benchaib, D. Frey, and S. Silvant, “A novel modular multilevel converter modelling technique based on semi-analytical models for HVDC application,” *J. Elect. Syst.*, vol. 12, no. 4, pp. 649–659, 2016.
[15] A. Hassanpoor, L. Ängquist, S. Norrga, K. Ilves, and H.-P. Nee, “Tolerance band modulation methods for modular multilevel converters,” *IEEE Transactions on power electronics*, vol. 30, no. 1, pp. 311–326, Jan. 2015.