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Controlled SOI nanopatterning for GaN pendeo-epitaxy

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ABSTRACT

Nanopatterning of GaN/AlN layers on Silicon-On-Insulator (SOI) substrates is discussed with the aim of fabricating nanopillar arrays that can be used for subsequent GaN pendeo-epitaxy. The principle of the developed epitaxy process is that GaN crystallites are grown on deformable nano-pedestals able to rotate at GaN growth temperature. The objective is to control the complete pattern profile of GaN/AlN/Si/SiO₂ pillars, both in lateral and vertical directions. Since a smaller pillar diameter should enhance the pillar rotation at growth temperature, special emphasis will be given to nanometer-scale pillars. In this context, the control of GaN/AlN vertical sidewalls is still an issue for high-resolution nanopillars. In this paper, we report on the optimization of the plasma etching processes of GaN/AlN/Si/SiO₂ stacks to reduce the slope that widens the pillar base. Overall, we achieve near perfect arrays of 100 nm diameter nanopillars obtained by combining Nanoimprint Lithography (NIL) and plasma etching, with bases of 150 nm in diameter.

1. Introduction

Due to its outstanding properties, Gallium Nitride (GaN) is currently exploited in power electronics and optoelectronic applications such as light emitting diodes (LEDs) and laser diodes. Yet the lifespan of such optoelectronic devices, in particular lasers, strongly depends on the material dislocation density, and since threading dislocations act as non-radiative centers they can also limit the device performance for optoelectronics [1,2]. GaN substrates are still expensive compared to other well performing semiconductor materials, not to mention the fact that the size of GaN wafers is limited. A good solution to this problem is the epitaxial growth of GaN on large and low-cost foreign substrates, such as silicon. This heteroepitaxy process is an attractive economic solution for the mass production of GaN. However, this is at the expense of material quality, which drops due to the generation of higher dislocation densities coming from the epi-layer/substrate lattice mismatch, the thermal expansion coefficient mismatch and the independent nucleation of initial AlN grains on the substrate. This behavior was demonstrated for the growth of aluminum nitride (AlN) on silicon [3], where AlN grains were found to be twisted with respect to each other with an in plane misorientation of up to $\pm 3^\circ$. More specifically, misfit dislocations lead to

mis-orientation of grains, resulting in grain boundary dislocations, which occur upon coalescence of nuclei in order to adjust their mis-orientation with respect to each other. These dislocations thread vertically through the AlN nucleation layer into the GaN epi-layer up to the device active region, acting as non-radiative centers and affecting the efficiency and lifespan of GaN devices.

In order to limit the dislocation density, GaN can be grown on patterned substrates where nucleation areas are minimized, to have fewer nucleation grains, and so reduce the dislocations originating from the substrate/nuclei interface. Several methods have been implemented to achieve this idea, such as epitaxial lateral overgrowth (ELO) [4,5] and pendeo-epitaxy (PE) [6,7]. Nevertheless, these techniques solve the problem only partially, since boundary defects can still occur upon coalescence of crystallites originating from different nucleation sites. In fact, neighboring crystallites approaching each other from independent nucleation sites inherit necessarily the crystallographic misalignment associated with the heteroepitaxial growth. This misalignment results in the generation of coalescence boundary dislocations required to accommodate the misorientation. The dislocations will thread within the epilayer up to the active region, leading to an inhomogeneous spatial distribution of stress and dislocation density dictated by the geometry of

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the initial pattern, as has been demonstrated in various studies [7,8].

In our unique approach, we aim to tackle both the mis-orientation problem and the high threading dislocation density, at the same time. In order to do so, we introduce a bottom-up approach based on the pendeo-epitaxy of GaN on nano-patterned silicon on insulator (SOI) templates. Thanks to this geometry, GaN crystallites are grown on deformable nano-pedestals that are able to rotate at GaN growth temperature (~1050 °C) [9].

In this paper we will discuss the development process that we adopted for the fabrication of these nano-pedestals which are composed of GaN /AlN /Si /SiO₂ /Si stack, cf. Fig. 1. We will discuss in detail our capability to control and optimize nanopillar dimensions and profiles as these parameters are crucial for nanopillar rotation and hence for the proper coalescence of GaN crystallites, which will lead later to the higher epitaxial layer quality.

2. Experimental details

The technology development and the process principle that we mentioned in the previous section are detailed in Fig. 1. A 270 nm thick GaN layer was grown by metal organic vapor phase epitaxy (MOVPE) on SOI substrates in an AIXTRON showerhead reactor. A 150 nm thick AlN layer was introduced between the GaN epi layer and the top silicon layer

of the SOI substrate. The AlN on Si growth is essential to avoid melt-back etching [10].

The next step was nanopatterning, where nanoimprint lithography (NIL) technique was used as it is compatible with high resolution patterning and high throughput, which are necessary for future micro-LEDs fabrication. After NIL and Lift-off, we managed to create metal dots patterns on samples. Next, using inductively coupled plasma (ICP) etching we generated nanopillars using the metal dots as a hard mask. Similar work was also performed by Le Boulbar et al, but their pattern resolution was limited to 230 nm [11]. For each set of macro patterns, we created one silicon master using E-beam lithography and ICP etching. The master mold served to duplicate patterns on hard-PDMS/PDMS stamps in order to be compatible with soft UV-NIL. The nano-pattern arrays exhibit an area varying from 40 × 40 μm² to 3 × 3 μm² with hexagonal symmetry and compatible with microLEDs processing. The dimensions of the nano-pillars are 100 nm or 200 nm in diameter with a 1000 nm-pitch (center-to-center distance).

The first step of this technological work is the stamp imprinting in the TU resist film on the GaN on SOI substrates. More precisely, a TU /Ge /PMMA tri-layer classical system was used to improve the lift off, as described in ref. [12]. For this NIL step we used an EITRE6 Obducat tool. A scanning electron microscopy (SEM) image of the imprinted holes is shown in Fig. 2 a. Next, a Ti (5 nm)/Ni (75 nm) metal mask was deposited using a Plassys electron beam evaporator. The Ti serves as an adhesion layer and the Ni as the hard mask layer for the etching step. Some researchers used the imprinted resist as an etching mask, such as Yamono et al. who succeeded in fabricating 140 nm wide pillars on a thin 25 nm AlN film [13]. The residual TU in the imprinted holes, the Ge and the PMMA layers are plasma etched before the Ti /Ni deposition and the lift off. The resulting Ti /Ni metal mask pillars are shown in Fig. 2 b with a pillar diameter of 100 nm.

Pattern transfer in the GaN /SOI stack is performed using an ICP DPS reactor from Applied Materials. The important parameter is the control of the SiO₂ etched depth, as it will impact the pillar deformation capability during further epitaxy steps. The etch process is controlled using an end-point system, EyeD from Verity Instrument allowing a real time monitoring. This system combines two techniques: interferometry and optical emission from the plasma. For the interferometry technique, a Xenon lamp providing wavelengths from 200 to 800 nm is used to create incident light on the wafer being etched. This is illustrated on Fig. 3a. The different curves correspond to different detection wavelengths (415 nm, 425 nm, 680 nm and 765 nm) whose intensity is sensitive to the etched material. The process parameters impact is analyzed in next section. The final result is a pillar array, where we see no missing pillar (Cf. Fig. 3b).

Pillar bases should give to GaN crystallites the freedom to rotate and align with each other, and so ensure a perfect coalescence rather than generating boundary dislocations. The SiO₂ is the material of choice for the base in our case. Due to its viscoelastic properties at GaN growth temperatures around 1050 °C, the SiO₂ allows us to achieve these goals.

Subsequently, GaN is selectively grown in a two step-process on top of the GaN/SOI pillars using trimethylgallium (TMGa) and ammonia (NH₃) as source precursors for Ga and N respectively, and H₂ as carrier gas. The growth process is carried out in two steps, as shown on Fig. 1: the nucleation step (step 1, Fig. 1 c) and the coalescence step (step 2, Fig. 1 d) as previously described in [9].

During the first growth step, GaN pyramids are selectively grown on top of the pillars. Step 1 is continued until adjacent pyramids come into contact. This step is then followed by step 2, where lateral growth is favored in order to promote the coalescence of the GaN pyramids and form a two-dimensional GaN layer (Cf. Fig. 1 d).

3. Results and discussions

GaN and AlN materials are typically etched using chlorine-based plasma etch [14]. For many years, a key objective was to increase the

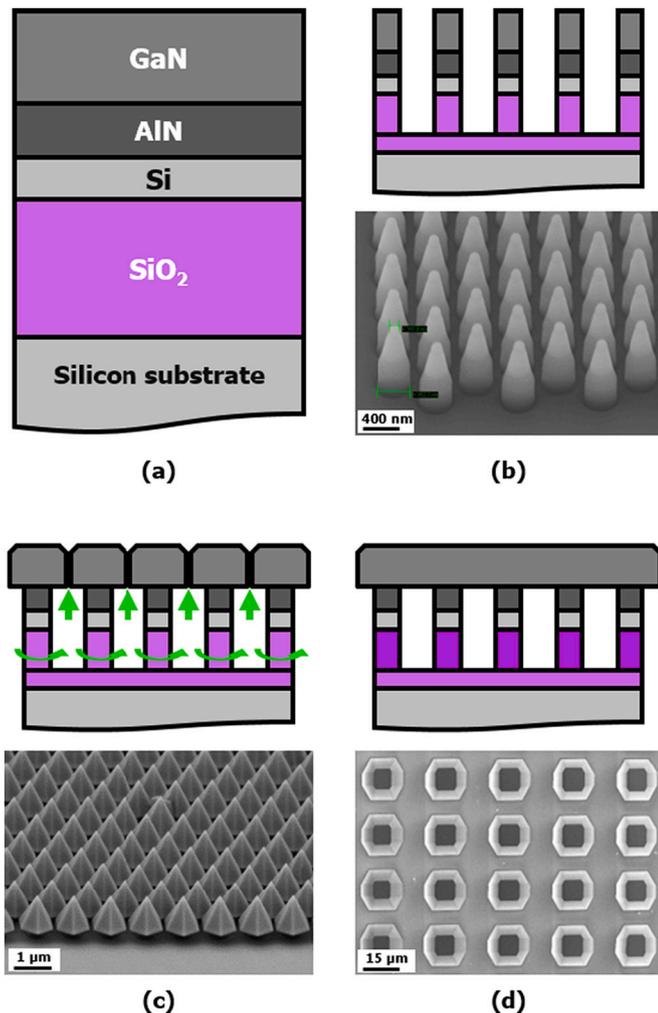


Fig. 1. Technology developments: (a) GaN on SOI stack, (b) nano-pedestals generated post lithography and etch, (c) GaN step 1 growth: selective nucleation and the principle of SiO₂ pillar twist during GaN epitaxy, (d) GaN step 2 growth: lateral growth. Each GaN mesa is grown on arrays of pillars/pyramids as those in (b) and (c).

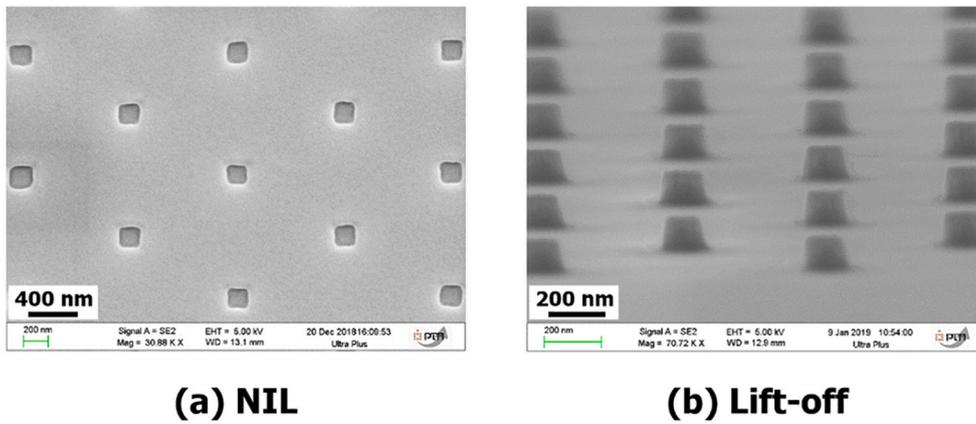


Fig. 2. (a) 100 nm patterns obtained in TU resist post NIL (b) post Ni deposition and lift off to create a hard mask.

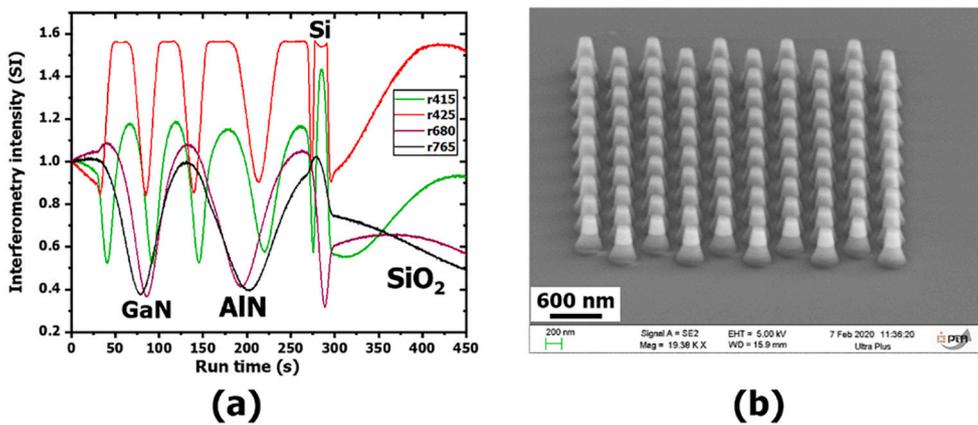


Fig. 3. (a) Real-time etch control is monitored using optical interferometry and (b) a 100 nm pillar array without any defect.

etching rate and control the etched profile of thick micrometric layers [15–17], and common processes use Cl_2 / Ar or Cl_2 / BCl_3 chemistries. Our initial etching process is determined from our previous experiments [9]. It is based on $Cl_2 / CH_4 / Ar$ and the plasma parameters are 3 mTorr /500 Ws /55 Wb. The gas ratio is 39 /12 /9 sccm for $Cl_2 / CH_4 / Ar$ respectively. The same process is used to etch all the materials including Si and SiO_2 within the heterostructure stack.

However, as discussed in the previous sections, the key idea of this project is the capability of SiO_2 pillar deformation and rotation during GaN pendeo epitaxy. The SiO_2 base diameter is therefore a crucial parameter, which must be optimized. The initial etching process resulted in an increased diameter of the nanopillars upon etching down within the stack. This increase in nanopillars base diameter is associated with the slope highlighted in Fig. 4a. As a result, a 100 nm top nanopillar diameter creates an SiO_2 base with very large diameter. It is worth mentioning that since the slope is constant under certain given etching

conditions, the deeper we etch the larger the SiO_2 base will be.

The objective is therefore to increase the verticality of the etched sidewalls. For this, ICP etch recipes were further optimized, where we now adopt a new chemistry plasma to etch the SiO_2 and Si layers. By using CF_4 gas, we were able to obtain vertical sidewalls in the Si and SiO_2 base pillar as shown in Fig. 4 b.

The next objective was then to control the slope in the etched sidewalls of GaN and AlN layers in order to reduce further the SiO_2 base diameter. Such adjustment has been already demonstrated but on high aspect ratio pillars, with top diameters of a few hundreds of nanometers [11,18]. The results are usually a good control of the verticality along the large height of the patterns, but a poor control of the slope that occurs as the etching starts. For our structures, we have to limit this slope since our etching depth is only 350 nm for the GaN /AlN stack. The influence of all the parameters of the chlorine-based plasma were therefore analyzed in order to improve the verticality of the GaN /AlN sidewalls. The influence of the pressure and the bias power was first studied, and the results are summarized in Fig. 5. An increase of the pressure results in an increase of the etching slope and therefore in an increase of the D_{bottom} pillar diameter. A pressure of 3 mTorr is therefore the optimized value, that cannot be decreased due to tool limitations. The same behavior was reported in ref. [18]. The influence of the bias power (Wb) was analyzed while the source power (Ws) was constant with a fixed value of 500 W. An increase of Wb shows a reduction of the SiO_2 base diameter down to 290 nm. This progression saturates for Wb values above 75 W. We note that the etching rate increases as we increase Wb for values to above 150 W. This makes it difficult to control the etched depth, hence hard to stop at the AlN/Si interface where we switch to the CF_4 Si/ SiO_2 etch recipe. A 100 W value for bias power was

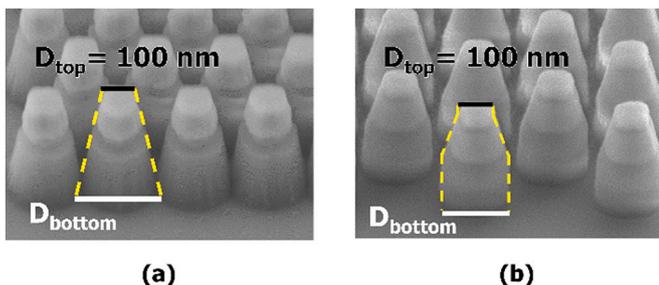


Fig. 4. Optimization of SiO_2 sidewalls.

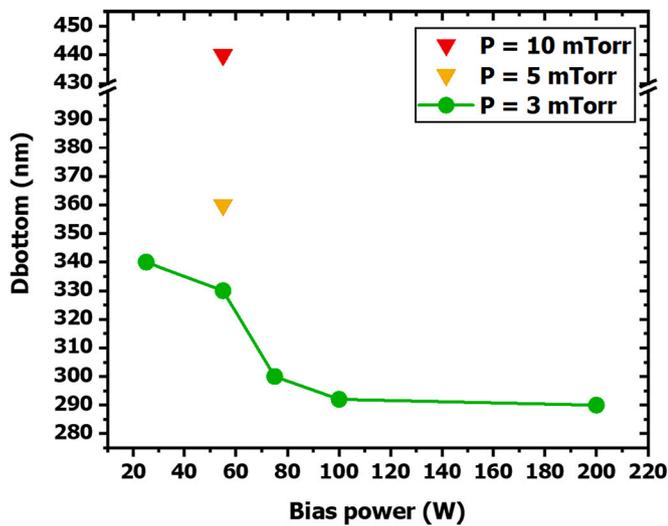


Fig. 5. Plasma parameter modification: three different etching pressures and bias power VS D_{bottom} for the same D_{top} of 100 nm.

then fixed. RF bias power is proportional to DC bias voltage. With increasing DC bias voltage, the ions impacting onto the substrate have more energy, which results in a higher anisotropy, a reduced slope and therefore a smaller pillar base diameter. However, the excessive increase of DC bias voltage may bring about the redepositing because of strong sputtering effect.

Next, we investigated the effect of plasma chemistry in order to make the etching slope in the GaN /AlN stack even more vertical. Etching gases flows and compositions were modified, and the most significant results are summarized in Fig. 6.

First the Ar flow value was increased from 9 sccm up to 90 sccm (Fig. 6 a). The hypothesis was here to enhance physical etching and get more vertical sidewalls, but this was not successful.

Next, the CH₄ /Cl₂ ratio was modified and when decreased from 12 sccm /39 sccm to 8 sccm /43 sccm, the impact on the base diameter was promising, as values dropped from 280 nm down to 235 nm. Following this positive behavior, we decided to decrease the presence of CH₄ in the

etching gas mixture even more. Interestingly, we have found that removing the CH₄ and the Ar completely from the etching gas mixture further straightens the nanopillars. In this case, the GaN /AlN stack was etched with chlorine only with a gas flow of 80 sccm (Cf. Fig. 6 c). The resulting bottom diameter is 200 nm and the impact of other parameters such as pressure, source and bias power have been analyzed once again using pure chlorine-based plasma with no significant change on the 200 nm diameter value.

Finally, as we were not able to reduce the base diameter any further with all the etch parameters that we can modify on our tool, we decided to perform a pure chlorine-based plasma etch on another ICP etching tool, Oxford Plasmalab 133, where we have access to the wafer etching temperature. In this tool, and during the etch process, the chuck is cooled to 5 °C, while on the Applied Materials tool the chuck had a fixed temperature of 55 °C. The source power, bias power and pressure values are 200 W/300 W/8mTorr respectively; it is difficult to compare the impact of these values to the ones used in the previous equipment since the reactor is different. The Cl₂ concentration is 80 sccm, which is similar to previous one.

Using this cooled chuck, a final SiO₂ base diameter of 150 nm was achieved with a 100 nm top, demonstrating a significant optimization of the process. Indeed, testing the temperature impact on the Applied Materials tool was impossible at this stage, however, the same effect has been previously observed in reference [18].

FIB-STEM and EDX analysis were additionally performed on some samples whose Si/SiO₂ layers were etched using CF₄ based plasma, as pillars illustrated on Fig. 4b. The goal is to analyze the etched sidewalls of the nanopillars and observe any possible passivation layers which could be responsible for the etching slope. These analyses are presented in Fig. 7. In this particular sample, a 30 nm protective SiO₂ top layer has been deposited on the GaN surface by physical vapor deposition prior to NIL and etching process.

The verticality of the Si and SiO₂ sidewalls is clearly observed from this view. We also notice that the etching slope is similar in GaN and AlN layers. Lastly, we see a very thin oxidized film on GaN and AlN sidewalls. However, this very thin layer is unlikely to be the reason for slope formation during etch.

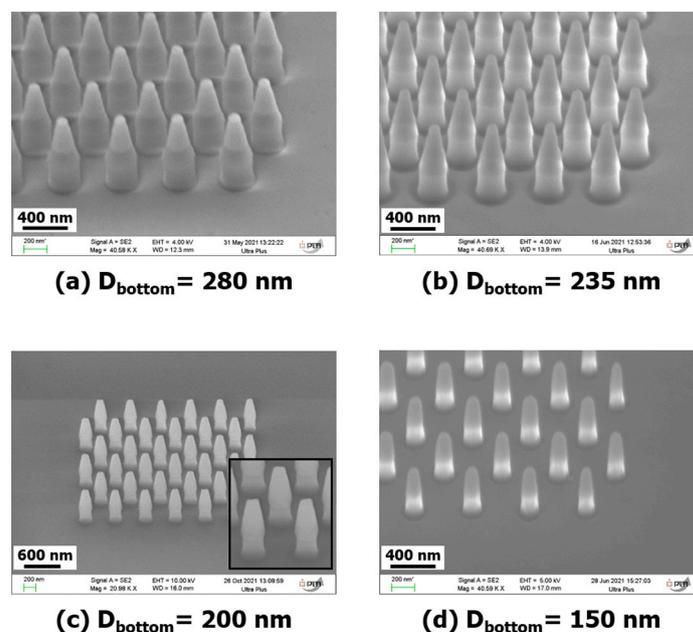


Fig. 6. Plasma chemistry effect on nanopillars profiles; (a) increase of Ar concentration (Cl₂/CH₄/Ar = 39/12/90); (b) increase of Cl₂ concentration (Cl₂/CH₄ = 43/8), (c) pure Cl₂ (80 sccm); (d) pure Cl₂ (80 sccm) on an Oxford Plasmalab 133 reactor with a chuck cooled down to 5 °C.

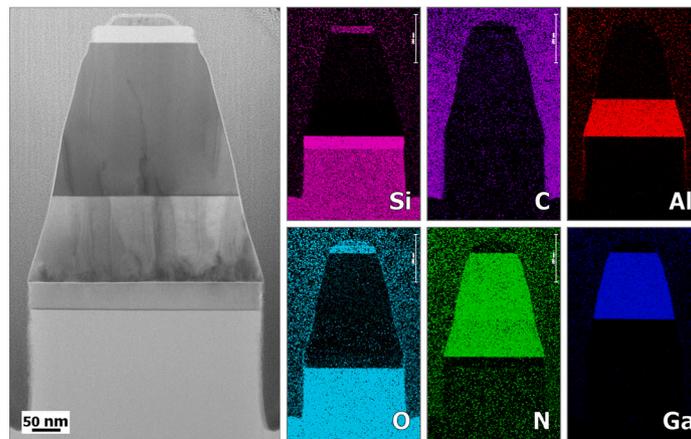


Fig. 7. STEM and EDX analysis.

4. Conclusion

NIL and plasma etching processes have been optimized to fabricate arrays of 100 nm diameter nanopillars. The objective was to reduce as much as possible the bottom width of the pillars in order to improve the pendeo-epitaxy quality. The impact of all the etching parameters was studied to optimize the verticality of each layer of the complex GaN/AlN/Si/SiO₂ stack. Near perfect arrays were imprinted and etched with a 150 nm base diameter that should help the pedestal rotation during GaN pyramids coalescence, reduce the dislocation density and therefore improve the quality of future microLEDs.

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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