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Guideline for test-structures placement for on-Wafer calibration in sub-THz Si device characterization

Chandan Yadav, Marco Cabbia, Sebastien Fregonese, Marina Deng, Magali de Matos, Thomas Zimmer
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Abstract—In this paper, we present a guideline to optimize the layout floorplan by minimizing the impact of on-wafer neighbouring structures in very high frequency (1 GHz to 220 GHz) on-wafer measurements of Si electronic devices. To present the guideline, a 3D electromagnetic (EM) simulation is carried out extensively using a realistic EM model of a commercial RF probe. First layout design dependent factors influencing the DUT characteristics are identified which are 1) way of positioning of the on-wafer structures w.r.t. DUT (e.g. in line or checkerboard pattern) and 2) the spacing between on-wafer structures and the DUT. Afterwards, a guideline to reduce the influence of on-wafer neighbours on the DUT characteristics is presented. The optimization of the layout floorplan with minimal on-wafer neighbours prior to their fabrication also permits to reduce the costs with respect to occupied Si area.

Index Terms—On-wafer TRL calibration, test-structures, EM simulation, RF probes, Spatial placement, sub-THz.

I. INTRODUCTION

OF late, millimeter wave (mmWave) and sub-millimeter wave (sub-mmWave) have received attention for many applications e.g. high speed 5G communication, automotive radar, biomedical applications etc. [1], [2]. For these high frequency (HF) applications, silicon (Si) and III-V technologies based devices and circuits are being explored and the on-wafer measurement is widely adopted in their characterization [3].

A compact model of an electronic device has become integral part in the integrated circuit and system designs. Accurate measurement data is an essential requirement for reliable compact model parameter extraction of electronic devices but at high frequencies accurate measurements with band-to-band continuity is a challenging task [4], [5]. For accurate HF-measurement of the electronic devices, layout design of test-structures plays a very important role [6], [7]. In addition, different factors e.g. probe design, pad design, substrate material, calibration techniques etc. can influence the measured S-parameters [8], [9]. On a high packing density silicon wafer, calibration kit structures as well as the active and passive devices are fabricated in very close vicinity to each other. Due to high packing density, influence of the on-wafer neighbouring environment on the on-wafer S-parameter measurement of a DUT cannot be ignored. Since, Si wafer area occupied by a device or circuit is directly related to cost. Therefore, optimizing a layout floorplan of calibration kit structures for accurate on-wafer S-parameter measurements of a DUT by optimal placement of on-wafer neighbours can potentially reduce the occupied wafer area.

II. DESCRIPTION OF SPATIAL POSITION OF STRUCTURES

The transistor-open shown in Fig. 1 is used as a DUT and its characteristics are studied under different on-wafer

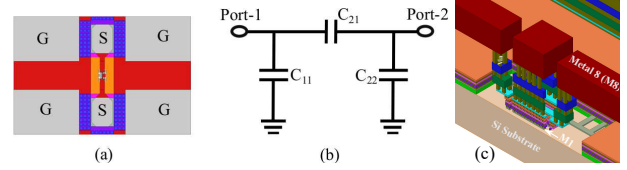


Fig. 1. (a) 2D schematic of transistor-open used as a DUT in this study where G and S refers to the ground and signal, respectively. Panel (b) shows capacitances associated with port-1, port-2 and between port-1 and port-2 of transistor-open. In panel (c), 8 metal lines in back-end-of-lines are shown using a cross sectional view of the transistor-open.

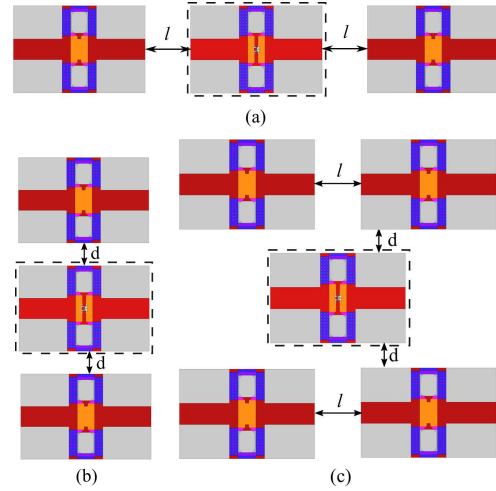


Fig. 2. Spatial placement of test-structures around a DUT (transistor-open) in three different ways. To clearly show position of the DUT, a dashed black box is used to highlight it in all the configurations.

neighbouring environments shown in Fig. 2. The on-wafer neighbouring structures placement around a DUT (inside a dashed box) in Fig. 2 are divided into two categories: 1) neighbours placement either parallel to the DUT (Fig. 2a) or behind the RF probes (Fig. 2b and Fig. 2c, here in a diagonal checkerboard pattern). Note that due to page limit, only few combinations of spatial placement of structures placements (but the most relevant) around a DUT are discussed in this work while many more other combinations are possible. All the structures in this study have 8-metal layers in the back-end-of-line (see Fig. 1c) and are designed for fabrication on Si similar to described by authors in [10]. Picoprobe probes with 100 μm and 50 μm pitch are used in the measurement between 1 - 110 GHz and 140 - 220 GHz but only the port-2 Picoprobe used in measurement is modelled in HFSS (see Fig. 3). Which is used to perform the EM simulation of the on-wafer TRL calibration test-structures as well as DUT including the probe. Since the work presented in [11] shows that simulation results using RF probe model corresponding to 1 -110 GHz showing satisfactory results upto 220 GHz, therefore, in this work only one model of the RF probe is used upto 220 GHz to reduce simulation time.

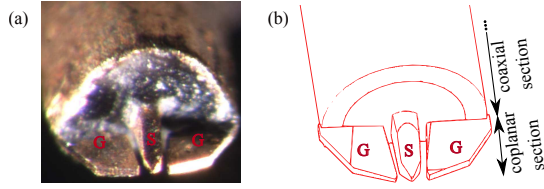


Fig. 3. (a) Image of the Picoprobe probe used at port-2 during measurement in 140GHz - 220 GHz frequency band and (b) 3-D sketch of the probe modeled in HFSS analogous to probe shown in panel (a).

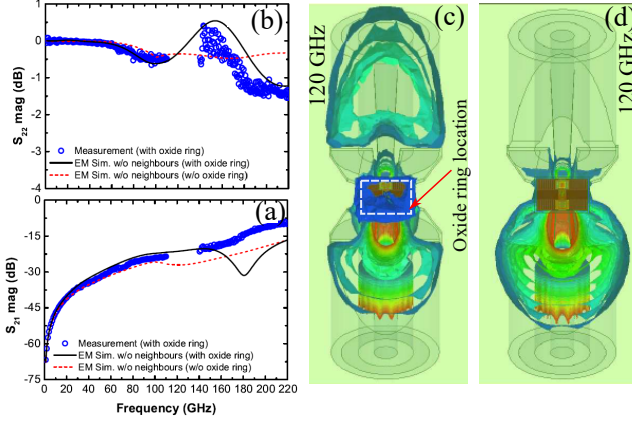


Fig. 4. S-parameters (S_{22} and S_{21}) of transistor-open with and without oxide ring around the DUT and calibration kit structures. The measurement data is corresponding to the fabricated structures having oxide ring around them. Due to the oxide ring (indicated in panel c by white color), the reflection S-parameter goes above 0 dB due to increased coupling with the substrate as shown in panel (c) at 120 GHz while replacing the oxide ring with a metal leads to expected value of S_{22} below 0 dB due to reduced parasitic coupling as shown in panel (d).

III. RESULTS AND DISCUSSION

A. Improving on-wafer Measurement of a Discrete DUT

First, the on-wafer TRL calibration is performed using the measured raw S-parameters of the thru, reflect and lines fabricated on the Si-BiCMOS55 technology of STMicroelectronics [12] and applied on the transistor-open (DUT), see Fig. 1c. The TRL calibrated on-wafer S-parameter of transistor-open are shown in Fig. 4 with the symbols. In the on Si wafer fabricated structures, each structure is surrounded by a $10\ \mu\text{m}$ wide oxide ring to electrically isolate each structure. Using the procedure adopted in [11] and RF probe model shown in Fig. 3, the EM simulations of on-wafer TRL calibration kit structures (thru, reflect and lines) as well as of the transistor-open (DUT) are performed one by one excluding all the on-wafer neighbours. For the impedance correction, $50\ \Omega$ on-wafer load is also designed and used. The EM simulation based on-wafer TRL calibrated S-parameters of transistor-open surrounded by a $10\ \mu\text{m}$ wide oxide ring are shown in Fig. 4 with solid black lines. The EM simulation prediction is qualitatively the same as the measured data including the S-parameter (S_{22}) value above 0 dB at around 150 GHz. To improve the S_{22} behaviour with frequency, the oxide ring in each structure is replaced by a copper layer connecting the two ground pads at each port, thus creating a ground shield all around the test-structures which should prevent any coupling with the neighbours. The EM simulations of the on-wafer TRL calibration kit structures and the transistor-open are again performed with this modification. The obtained on-wafer

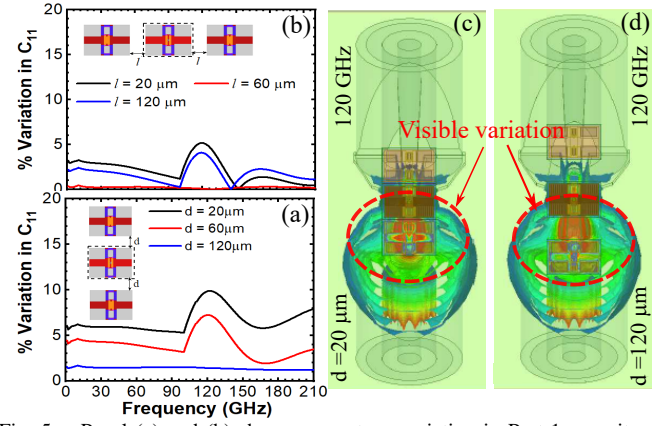


Fig. 5. Panel (a) and (b) shows percentage variation in Port-1 capacitance C_{11} of the transistor-open (DUT) with neighbours (shown in inset and Fig. 2) in reference to DUT without neighbour shown in Fig. 1a. A non-zero % variation shows influence of the on-wafer structures on DUT. Panel (c) and (d) shows electric field distribution in transistor-open in presence of on-wafer structures of design Fig. 2a at 120 GHz for two values of "d".

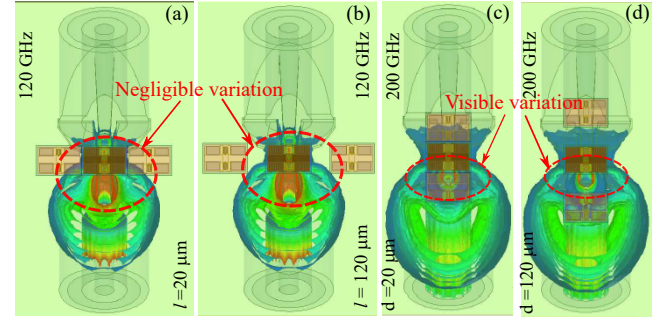


Fig. 6. Electric field distribution in transistor-open with on-wafer design shown in Fig. 2b and Fig. 2a at 120 GHz and 200 GHz, respectively. The variations in electric field distribution are visible in panel (c) and (d) with change in value of "d".

TRL calibrated S-parameters of transistor-open are shown in Fig. 4 with red dashed line where S_{22} is always below the 0 dB. To understand the differences in the S-parameters due to the presence and absence of the oxide ring, the electric field distributions on the same scale are shown for the transistor-open at 120 GHz by including and excluding oxide ring in Fig. 4c and Fig. 4d, respectively. The backside views in Fig. 4 show that the presence of an oxide ring around structures increases the coupling with the substrate and between port-1 and port-2. This phenomenon has already been observed and investigated on III-V technologies [13]. The reduced coupling in Fig. 4d compared to Fig. 4c explain this improvement in S-parameter behavior in Fig. 4a and b.

B. Impact of Spatial Placement of on-Wafer Neighbours

Further, to analyse the impact of the spatial placement of the on-wafer neighbours around a DUT, structures with ground shield i.e. without oxide ring are used. If on-wafer neighbours do not have any impact on the S-parameter of a DUT, then the measured S-parameter or the from S-parameter derived characteristics of a DUT by including or excluding the on-wafer neighbours should be the exactly same. Here we focus on the transistor-open capacitances, which are more relevant for device modeling purposes. The percentage variations in port-1 capacitance of the transistor-open (C_{11}) are calculated as $100 \times (C_{11,N} - C_{11,\text{ref}}) / C_{11,\text{ref}}$ in presence of the on-wafer

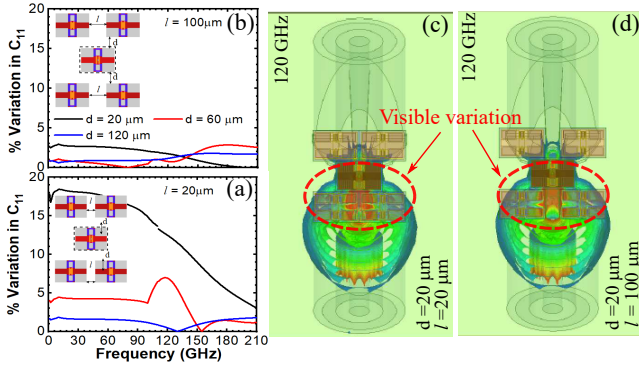


Fig. 7. The percentage variation in C_{11} of transistor-open (DUT) with neighbours of design in Fig. 2c in respect to DUT without neighbours, (a) $l = 20 \mu\text{m}$ and (b) $l = 120 \mu\text{m}$. In the panel (a), the legend entry for 'd' is the same as shown in (b). Panel (c) and (d) shows electric field coupling at 120 GHz.

neighbours where $C_{11,\text{ref}}$ and $C_{11,N}$ are capacitance excluding (i.e. reference data) and including the on-wafer neighbours, respectively. A zero and non-zero percentage variation in C_{11} of the DUT would indicate no impact (i.e. ideal placement) and impact of the spatial placement of structures around a DUT, respectively. Further analysis is presented for different types of spatial placement of the on-wafer structures around a DUT (transistor-open) shown in Fig. 2.

For the on-wafer placement of structures in Fig. 2a and Fig. 2b, the % variations in C_{11} of the DUT are shown in Fig. 5a and Fig. 5b, respectively. Both the placement designs show non-zero variations hence highlights that presence of an on-wafer structure around the DUT can have some influence on the DUT characteristics. A non-zero percentage variation in C_{11} can be attributed to variations in electric field distribution of a DUT due to parasitic couplings after including the on-wafer structures around it (compare Fig. 4d with Fig. 5c and Fig. 5d). Since, variations in C_{11} of DUTs with on-wafer structures in Fig. 2a and Fig. 2b are different for the same value of the "d" or "l", this indicates that with change in spatial placement of the on-wafer structures, their influences on DUT characteristics varies. These variations are associated with change in parasitic couplings due to the spatial placement of structures (compare Fig. 5c and Fig. 5d with 6a and Fig. 6). With stronger variations in C_{11} corresponding to placements in Fig. 2b indicates that an on-wafer structure just below the RF probe signal trace and very close to the DUT (e.g. see variation with "d") should be avoided.

In Fig. 5, the % variation in C_{11} w.r.t. frequency is not constant for a given value of 'd' or 'l'. This frequency dependent variation in DUT characteristics is probably due to the change in the signal wavelength which can alter the interaction / coupling of a DUT with the same neighbours. The frequency dependent variation in parasitic coupling of the DUT with neighbours can be observed by comparing the electric field distribution for the same "d" in Fig. 5c and Fig. 6c or Fig. 5d and Fig. 6d at 120 GHz and 200 GHz, respectively.

From the aforementioned observation we deduce that the structure placement below the RF probe requires a careful strategy. Thus neighbours' placement shown in Fig. 2c is analyzed further. In this diagonal checkerboard pattern design, the structures are placed at a distance $l/2$ from the center of

the signal trace of the RF probes. In Fig. 7a and Fig. 7b, the variation in the C_{11} behaviour of the transistor-open is shown for two values of 'l' i.e. $20 \mu\text{m}$ and $100 \mu\text{m}$. It can be easily noticed that in Fig. 7, for $l = 20 \mu\text{m}$ the variation in the C_{11} is more pronounced because some part of the neighbouring structures are either lying very close to or below the signal trace. The same conclusions can be drawn qualitatively from the electric field distribution of the DUT with on-wafer structures for $l = 20 \mu\text{m}$ and $100 \mu\text{m}$ shown in Fig. 7c and Fig. 7d. Note that these observed variations may vary quantitatively with change in test-structures design or RF probe design.

IV. CONCLUSION

It is observed that the influence of the spatial placement of an on-wafer structure around a DUT varies with change in their location and placement distance w.r.t. the DUT. A greater attention is required while placing a structure just below the signal trace of a RF probe. It has been shown that when using a diagonal checkerboard pattern, the influence of an on-wafer structures on the DUT characteristics becomes negligible and further increase of the distance would increase the wafer area and thus the costs.

REFERENCES

- [1] K. Sengupta *et al.*, "Terahertz Integrated Electronic and hybrid Electronic-Photonic Systems," *Nat. Electron.*, vol. 1, pp. 622–635, 2018.
- [2] P. Hillger *et al.*, "Terahertz Imaging and Sensing Applications With Silicon-Based Technologies," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 1–19, Jan 2019.
- [3] P. Chevalier *et al.*, "Si/SiGe:C and InP/GaAsSb Heterojunction Bipolar Transistors for THz Applications," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 1035–1050, June 2017.
- [4] C. B. Sia, "Minimizing discontinuities in wafer-level sub-THz measurements up to 750 GHz for device modelling applications," in *89th ARFTG Microwave Measurement Conference*, June 2017, pp. 1–4.
- [5] S. Fregonese *et al.*, "On-Wafer Characterization of Silicon Transistors Up To 500 GHz and Analysis of Measurement Discontinuities Between the Frequency Bands," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 7, pp. 3332–3341, July 2018.
- [6] T. E. Kolding, "Shield-based microwave on-wafer device measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1039–1044, June 2001. doi: 10.1109/22.925488
- [7] M. S. Eggebert *et al.*, "On the Accurate Measurement and Calibration of S-parameters for Millimeter Wavelengths and Beyond," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2335 – 2342, July 2015.
- [8] C. Andrei *et al.*, "Coupling On-wafer Measurement Errors and their Impact on Calibration and De-embedding up to 110 GHz for CMOS millimeter wave Characterizations," in *IEEE Int. Conf. Microelectronic Test Structures (ICMTS)*, March 2007, pp. 253–256, doi=10.1109/ICMTS.2007.374494.
- [9] S. Fregonese *et al.*, "Comparison of On-Wafer TRL Calibration to ISS SOLT Calibration with Open-Short De-embedding up to 500 GHz," *IEEE Trans. THz Sci. Technol.*, vol. 9, no. 1, pp. 89–97, Jan. 2019.
- [10] M. Deng *et al.*, "Design of Silicon On-Wafer sub-THz Calibration Kit," in *IEEE Mediterranean Microwave Symp.*, Nov. 2017, pp. 1–4.
- [11] C. Yadav *et al.*, "Importance and Requirement of Frequency Band Specific RF Probes EM Models in Sub-THz and THz Measurements up to 500 GHz," *IEEE Transactions on Terahertz Science and Technology*, vol. 10, no. 5, pp. 558–563, 2020.
- [12] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, Dec. 2014, pp. 3.9.1–3.9.3.
- [13] G. N. Phung *et al.*, "Impact of Parasitic Coupling on multiline TRL Calibration," in *2017 47th European Microwave Conference (EuMC)*, 2017, pp. 835–838.