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Optimizing Finger Spacing in Multi-Finger Bipolar Transistors for Minimal Electrothermal Coupling

Aakashdeep Gupta, K Nidhin, Suresh Balanethiram, *Member, IEEE* Shon Yadav, Sebastien Fregonese, Thomas Zimmer, *Senior Member, IEEE*, Anjan Chakravorty, *Member, IEEE*

Abstract—We present a compact modeling framework to optimize finger spacing for improving the thermal stability in multi-finger bipolar transistors with shallow-trench isolation. First, we present an accurate physics-based model for total junction temperature in all the fingers of a transistor. Other than validating the model with 3D TCAD simulations and measured data, we demonstrate its efficacy to achieve finger spacing optimization with the aid of an iterative algorithm. Since the proposed technique is scalable from the viewpoint of the number of fingers within a transistor and their geometries, the proposed framework is found to work seamlessly for various emitter finger numbers.

Index Terms—SiGe HBT, multi-finger transistor, finger placement, self-heating, thermal coupling, shallow trench isolation, Kirchhoff’s transformation.

I. INTRODUCTION

Multi-finger silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) are preferred in power amplifier applications [1]–[3]. A conventional layout of a multi-finger transistor always consists of uniformly spaced emitter fingers with a fixed emitter width (W_E) and emitter length (L_E) [1] (see Fig. 1(a)). High current operations of power amplifiers cause electro-thermal heating inside the device leading to a high junction temperatures [4]. Since all the fingers dissipate heat simultaneously, the total junction temperature of a given finger is resulted from the self-heating (due to power dissipation within the finger) and thermal coupling (from power dissipation at adjacent fingers) effects [5], [6]. Note that all the fingers are electrically isolated but thermally coupled via substrate. The unequal amount of thermal coupling at each finger of the conventional layout (Fig. 1(a)) leads to an uneven total temperature distribution across the fingers and one observes a comparatively higher temperature in the central (or inner) fingers [7]. This can lead to degraded electrical performances and various issues due to electro-thermal instability such as snapback and thermal runaway [8] eventually affecting the safe-operating-area and reliability

of the device [9]. One can overcome these issues with non-uniform finger spacing in a multi-finger transistor structure as shown in Fig. 1(b). A careful optimization of finger spacing can help obtaining nearly uniform temperature at all the fingers. Such an optimization can be carried out either using computationally expensive numerical simulations [10], [11] or by the use of complex analytical formulation [12]. A simple, fast and accurate analytical model to solve this optimization problem is not reported so far in the literature.

Existing electrothermal compact models of multi-finger transistors use superposition to compute the rise in the junction temperature of i^{th} finger (ΔT_i) above an ambient temperature (T_a) as [5] [6] [13] [14]

$$\begin{aligned} \Delta T_i &= \Delta T_{ii} + \sum_{j=1, j \neq i}^n \Delta T_{ij} \\ &= P_{d,i} R_{th,ii} + \sum_{j=1, j \neq i}^n c_{ij} P_{d,j} R_{th,jj} \end{aligned} \quad (1)$$

where the first term indicates the self-heating at i^{th} finger and the second term accounts for the thermal coupling on i^{th} finger from all other fingers. $P_{d,i}$ ($P_{d,j}$) and $R_{th,ii}$ ($R_{th,jj}$) are, respectively, the electrical power dissipation and thermal resistance corresponding to the i^{th} (j^{th}) finger. Static thermal coupling coefficient (c_{ij}) quantifies the amount of mutual thermal coupling over finger- i due to the heat source at finger- j and is defined as

$$c_{ij} = \frac{\Delta T_{ij}}{\Delta T_{jj}}. \quad (2)$$

However, direct use of (1) on the measured data to extract thermal coupling related model parameters yields erroneous results as reported in [15]. The study clearly states that the validity of (1) is limited only to a linear case where the thermal conductivity (κ) of a given substrate material is constant. However, the thermal conductivity of substrate Si is temperature-dependent [16]; hence the governing heat diffusion equation becomes non-linear. Therefore, one cannot use (1) as a basis formulation in order to optimize the finger spacing for obtaining a nearly uniform temperature distribution in a multi-finger transistor.

In this paper, we present a simple analytical compact model framework along with an iterative algorithm to obtain a fast and logical solution of this optimization problem. Section II describes modeling framework, followed by model validation with 3D TCAD simulation and measurement data in section III. In section IV we present the results and discussions on

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spacing optimization using the proposed model and finally conclude in section V.

II. MODELING FRAMEWORK

Figs. 1(a) and (b) show the top view of a shallow trench (ST) isolated five-finger structure with uniform (s) and non-uniform spacing (s_i with $i=1, 2, 3, 4$), respectively. In Fig. 1(b), the spacing between the inner fingers (s_2 and s_3) are increased to reduce the total thermal coupling and the total temperature rise at the central finger maintaining a constant the foot print as in Fig. 1(a). Essentially, we kept $(n-1)s = \sum_{k=1}^{n-1} s_k = d$, with n as the number of fingers. The problem is to quickly find out the optimized values of $[s_1, s_2, s_3, s_4]$ in order to ensure a nearly equal and possibly minimal junction temperature at all the fingers. Note that for every unique spacing combination there exists a unique set of temperature values of all the fingers. We start with an accurate estimation of total temperature rise of a given finger due to self-heating and thermal coupling for any given set of spacing values.

A. Linear self-heating

Fig. 2 shows a cross-sectional view of the first three fingers in an n -finger shallow trench (ST) isolated structure with a substrate thickness of H and spacing between the immediate neighbours as s_1 and s_2 . The heat-flow volume of the heating finger (i.e., $j=1$ in Fig. 2) is defined with the thermal spreading angles (θ' and θ). The z -dependent temperature profile $T(z)$ under the heating finger can be expressed as [17]

$$T(z) = T_a + P_d R_{th}(z) \quad (3)$$

where $R_{th}(z)$ is z -dependent thermal resistance at an ambient temperature T_a and is expressed as $R_{th}(z) = [1/\kappa(T_a)] [\int_0^z dz/A(x, y, z)] = f_G(z)/\kappa(T_a)$. The geometry factor $f_G(z)$ is defined in terms of position-dependent heat-flow cross-sectional area, $A(x, y, z) = (L_E + 2z \tan(\theta_z))(W_E + 2z \tan(\theta_z))$, as [18]

$$f_G(z) = \int_0^z \frac{dz}{A(x, y, z)} = \frac{\ln \left[\frac{L_E(W_E + 2z \tan(\theta_z))}{W_E(L_E + 2z \tan(\theta_z))} \right]}{2(L_E - W_E) \tan(\theta_z)} \quad (4)$$

where W_E and L_E are, respectively, the width and length of the heat source. Note that the heat spreading angle $\theta(z) = \theta'$ within ST and $\theta(z) = \theta$ outside ST. We evaluate (3) to estimate the substrate temperature at any z by considering a constant thermal conductivity of the substrate material ($\kappa(T_a)$) measured at T_a . This yields a linear junction temperature rise at the heat-source ($\Delta T_{jj,lin} = T(z=0) - T_a$) due to the self-heating effect.

B. Linear thermal coupling

It is evident that the junction temperature of the neighboring fingers ($i=2, 3, \dots, n$) tends to rise above T_a (by an amount $\Delta T_{ij,lin}$) due to thermal coupling from the heating finger ($j=1$). In [13] we reported a strategy to model the coupling coefficients (c_{ij}) in device structures without any trench isolations and also for the ST-isolated devices. Although the formulations derived in [13] considered $\kappa(T)$, the approximations

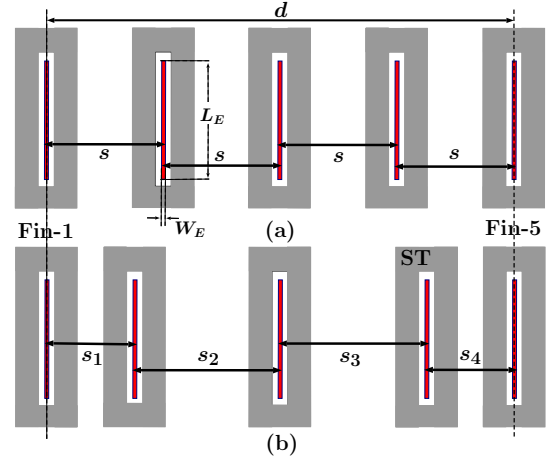


Fig. 1. Top views of the shallow trench isolated five-finger structures with (a) uniform spacing (s) and (b) non-uniform spacing. A fixed value of d ensures the same total footprint area for both the structures. Areas shaded in grey and red, respectively, indicates ST isolation and emitter fingers (of area $A_E = W_E \times L_E$).

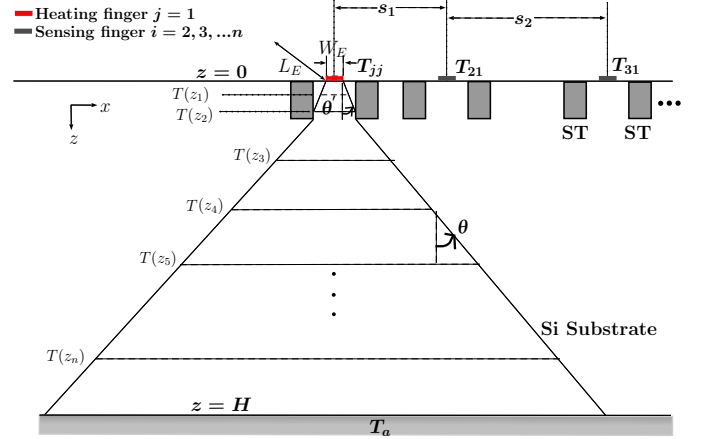


Fig. 2. Schematic cross-section of a five-finger multifinger transistor structure with ST isolation. The heat source is located at $z=0$.

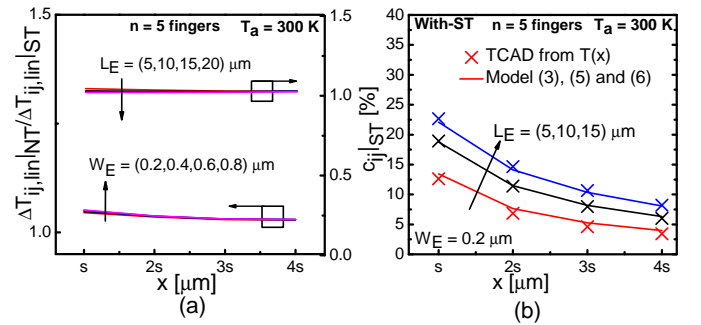


Fig. 3. (a) Linear temperature ratio at the sensing fingers of transistors with no-trench to with-ST ($\Delta T_{ij,lin}|_{NT} / \Delta T_{ij,lin}|_{ST}$) obtained from TCAD for different W_E at a fixed $L_E = 5 \mu\text{m}$ and for different L_E at a fixed $W_E = 0.2 \mu\text{m}$. (b) A comparison of c_{ij} between TCAD (symbols) and values resulting from the model (solid-lines) of $c_{ij}|_{ST}$ for the case when 1st finger is heating and rest fingers are sensing. A constant finger spacing of $s = 2.5 \mu\text{m}$ is used in the structures.

used in the derivation hold true even for the linear case with constant $\kappa(T_a)$. The resulting c_{ij} in a no-trench (NT) structure is expressed as [19]

$$c_{ij}|_{NT} = \frac{\Delta T_{ij,lin}|_{NT}}{\Delta T_{jj,lin}|_{NT}} \equiv \frac{T_{NT}(z = x = s') - T_a}{T_{NT}(z = 0) - T_a} \quad (5)$$

where s' is the spacing between the heating and sensing finger. Note that the $c_{ij}|_{NT}$ in (5) comes out to be P_d -independent due to linear $T_{NT}(z)$. Subsequently, following [13] one can express the coupling factor for the structure with-ST as

$$c_{ij}|_{ST} = c_{ij}|_{NT} \left(\frac{\Delta T_{ij,lin}|_{ST}}{\Delta T_{ij,lin}|_{NT}} \right) \left\{ \frac{\Delta T_{jj,lin}|_{NT}}{\Delta T_{jj,lin}|_{ST}} \right\} \approx c_{ij}|_{NT} \left\{ \frac{\Delta T_{jj,lin}|_{NT}}{\Delta T_{jj,lin}|_{ST}} \right\}. \quad (6)$$

Note that all the terms in (5) and (6) can be directly obtained using (3) along with (4). Fig. 3(a) demonstrates the validity of the approximation $\Delta T_{ij,lin}|_{NT} / \Delta T_{ij,lin}|_{ST} \approx 1$ (as used in (6)) for various emitter geometries and at a fixed $\kappa(T_a)$. Since the shallow trench (ST) depth ($< 0.4 \mu\text{m}$) is usually much less than the finger spacing (around $2.5 \mu\text{m}$), the overall coupling temperature in ST-isolated device hardly differs from that of the no-trench (NT) device. One obtains P_d -independent $c_{ij}|_{ST}$ from (6) and subsequently $\Delta T_{ij,lin}|_{ST}$ using (2). In Fig. 3(b) we compare the results from (6) (solid lines) against the TCAD values (with fixed $\kappa(T_a)$) for five-finger uniformly spaced structures with spacing of $2.5 \mu\text{m}$ and different emitter geometries. Note that we employ heat spreading angle of 35° (for volume confined by ST) and 48° (for volume below ST) in (4) to obtain the solid lines. From the results of Fig. 3, one can confirm the efficacy of (5) and (6) in predicting the thermal coupling between a given pair of heating and sensing fingers with any finger spacing.

C. True junction temperature and spacing optimization

The formulations presented in II-A and II-B are linear due to temperature independent thermal conductivity and provide us with the information of temperature rise caused by self-heating and thermal coupling at a given i^{th} finger. The linearity allows one to employ the superposition relation of (1) to obtain $\Delta T_{i,lin}$ from the sum of $\Delta T_{ii,lin}$ and $\Delta T_{ij,lin}$ (for all j). However, the substrate thermal conductivity is temperature-dependent in the practical range of operation and follows a relation $\kappa(T) = \beta/T^\alpha$ [16]. Following the work in [15], we apply Kirchhoff transformation over the already estimated $\Delta T_{i,lin}$ to obtain the true total junction temperature as

$$T_{i,true} = T_a \left[1 + (1 - \alpha) \frac{\Delta T_{i,lin}}{T_a} \right]^{1/(1-\alpha)}. \quad (7)$$

Note that α and β are substrate material parameters to model the temperature dependent thermal conductivity. In order to obtain a minimum peak temperature with maximum possible uniformity in the temperature distribution of the multi-finger transistor structure, we embed the above developed model (7) into an optimization algorithm shown in the form of a flow chart in Fig. 4. In the main program we first start by defining the minimum (s_{min}) and maximum sweeping (s_{max}) limits

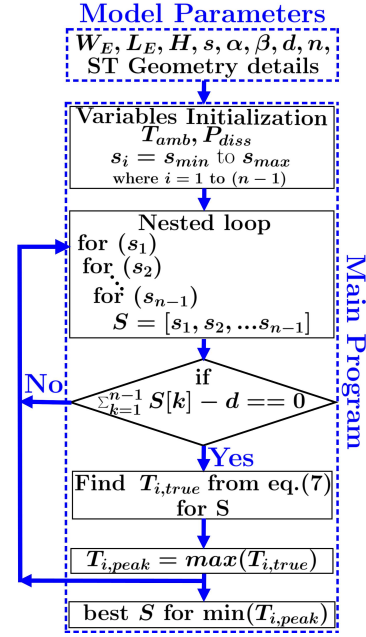


Fig. 4. The complete flow chart of the algorithm to obtain the optimized non-uniform finger spacing. The algorithm is valid for any number of fingers and employs true total temperature model as a function. All the geometry details and thermal conductivity parameters are inputs.

for all the spacing variables (s_i). Note that for a practical purpose, s_{min} and s_{max} can be, respectively, set to $s_{uni}/2$ and $3s_{uni}/2$ where $s_{uni} = d/n$ with d as the total spacing between the corner fingers and n as the total number of fingers. Following this, we employ nested loops to generate all the possible combinations of finger spacing variables. In a given iteration, we store a set of spacing variables into an array S . At the if-decision block, we check and select a given S if all its elements add to the fixed value of the parameter d . The main program then calls the $T_{i,true}$ model (7) to compute the total junction temperatures at all fingers and stores them in the array $T_{i,true}$ for a selected S . We further store the maximum value of the array $T_{i,true}$ as $T_{i,peak}$. The algorithm yields optimized set of finger spacing that is associated with the minimum value of $T_{i,peak}$. All the geometry details and material properties are fed into the program as model parameters.

III. MODEL CALIBRATION USING STRUCTURES WITH UNIFORM FINGER SPACING

A. Calibration with TCAD simulation

We created two types of five-finger transistor structures with silicon substrate in TCAD environment of Synopsys Sentaurus [20], one with no-trench and the other with-ST isolation. Uniform finger spacing was kept at $d/5 = 2.5 \mu\text{m}$. The dimensions of the structures correspond to those of the state-of-the-art SiGe HBTs from STMicroelectronics B55 technology [21]. An emitter area of $0.2 \times 5 \mu\text{m}^2$ is maintained for both the structures. We performed 3D thermal simulations of these TCAD structures where all the fingers were heated simultaneously in order to emulate a real operating condition. Note that the substrate material thermal parameters with

$\alpha = 1.261$ and $\beta = 2.076 \times 10^5 \text{ WK}^{\alpha-1}/\text{m}$ were used in the simulation.

Figs. 5 (a) and (b) compare the P_d -dependent $T_{i,true}$ obtained from (7) (solid lines) and the TCAD (symbols) for a five-finger transistor with no-trench and with-ST isolation, respectively. For $f_G(z)$ calculation in (4) we used heat spreading angles of 35° and 48° , respectively, for within and outside the ST region. The results of our modeling framework show excellent agreement with the TCAD simulation results. Two sets of TCAD data with red circles and black cross (and the respective modeling results) correspond to the 5-finger structures with uniform spacing ($s=2.5 \mu\text{m}$) and optimized spacing, respectively. Results show that our model predicts the TCAD simulation with high level of accuracy; hence it can be used to optimize the finger spacing for minimizing the overall electrothermal heating instead of rigorous TCAD simulation. In order to compare the maximum achievable accuracy of state-of-the-art existing model, we have also added the total temperature values resulting from (1) (green symbols) after substituting the non-linear TCAD simulated values of ΔT_{jj} and ΔT_{ij} in the case of $P_d=30 \text{ mW}$. It is observed that the existing model noticeably underestimates the true finger temperature. Optimized spacing related results are discussed in section IV.

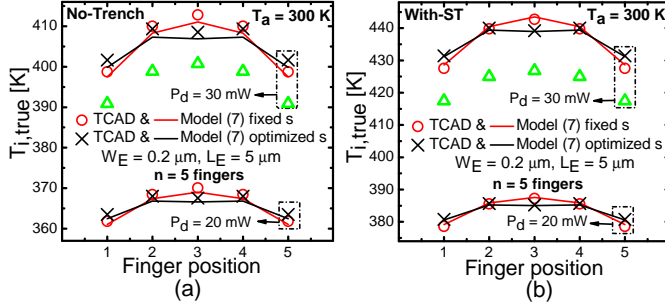


Fig. 5. Comparison of total temperature distribution obtained from model (solid lines) and TCAD (symbols) in (a) no-trench and (b) with-ST structures for all the fingers. Data points in red and black result from structures with uniform and optimized spacing, respectively. Green symbols represent existing state-of-the-art model obtained from (1) after substituting non-linear TCAD simulated values of ΔT_{jj} and ΔT_{ij} for uniformly spaced structure.

B. Calibration with Experimental data

To validate the proposed framework for a fabricated device, we chose the on-wafer measurement data presented in the work of [22]. Thermal characterizations were carried out for shallow trench-isolated five-finger HBTs from state-of-the-art technology of IHP microelectronics. Devices with emitter dimensions of $W_E \times L_E = 0.44 \times [7.64, 12.68, 27.8] \mu\text{m}^2$ and uniform finger spacing of $s = 3.23 \mu\text{m}$ were considered in the study. Following [15] we extracted the true junction temperature ($T_{i,true}$) values for all the on-wafer devices and used them to validate our model. Note that in a practical device one should account for the upward heat flow through the back-end-of-line (BEOL) metallization layers, and also consider the variation in thermal conductivity due to doping and the

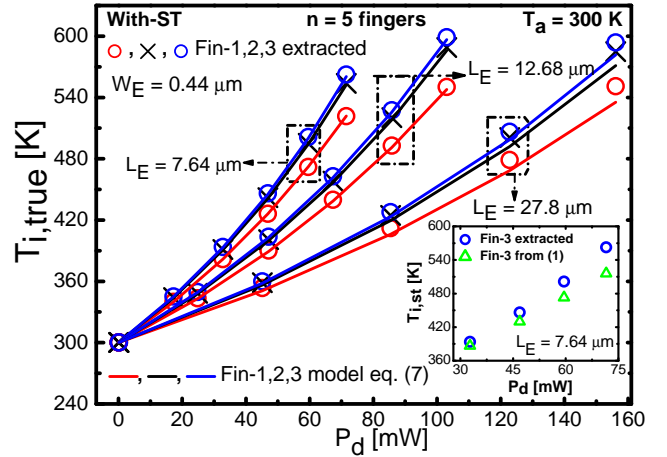


Fig. 6. True finger temperature of fingers-1, 2 and 3 for a fabricated shallow trench isolated structures with $W_E = 0.44 \mu\text{m}$ and $L_E = [7.64, 12.68, 27.8] \mu\text{m}$: comparison of the proposed model against the extracted data from measurements. Inset shows the underestimation in predicting the $T_{i,true}$ values obtained by a direct use of superposition of measured self-heating and coupling temperature data for the central finger.

materials in the heat flow path. The upward heat flow is modeled by a finite BEOL thermal resistance ($R_{th,m}$) that appears in parallel with the net substrate thermal resistance $R_{th,s}$ to produce the overall self-heating thermal resistance (R_{th}) seen from the heating finger. Before the model validation step we used the the extraction strategy detailed in [23] that employs the concept of average thermal conductivity of the substrate material to simultaneously extract the substrate $\kappa(T)$ related parameters α and β , and the BEOL related $R_{th,m}$ parameter by utilizing multiple measured data points of self-heating junction temperature (T_{jj}) and thermal resistance ($R_{th,jj}$). Since the extracted thermal conductivity parameters are obtained directly from experimental data, they automatically include the effects of substrate material and doping on to the overall thermal behavior.

Fig. 6 compares the results of $T_{i,true}$ obtained from our model (solid lines) with those extracted from on-wafer measurements (symbols) for all the three emitter geometries. Excellent model agreement is observed across different emitter geometries. Increased thermal coupling for the inner fingers than the corner fingers results in higher temperature for fingers-3 and 2 than finger-1. $R_{th,m}$ values of 20, 15, 12 (in kK/W) were extracted for the devices with L_E of 7.64, 12.68, 27.8 (in μm) respectively. Similarly, the extracted values of $\alpha = 1.285$ and $\beta = 2.136 \times 10^5 \text{ WK}^{\alpha-1}/\text{m}$ and they were used for model validation. The inset in the figure demonstrates the highest achievable accuracy in predicting the total junction temperature at finger-3 for the device with $L_E=7.64 \mu\text{m}$ by a direct use of superposition of the measured self-heating and coupling temperature data (state-of-the-art model). The prediction becomes significantly erroneous with increasing dissipated power.

IV. FINGER SPACING OPTIMIZATION RESULTS

Excellent model capability and its calibration with TCAD simulation and measured data are demonstrated in section III.

Therefore, we can now apply our model for the purpose of finger spacing optimization in order to ensure minimal over device temperature due to electrothermal heating. We implemented the finger spacing optimization algorithm detailed in section II (see Fig. 4). The algorithm was executed for TCAD multi-finger structures based on STMicroelectronics, as mentioned in section III-A. Appropriate values of model parameters are inserted and optimized spacing values are obtained via iterative calculations. Fig. 5 presents the $T_{i,true}$ values (in black) obtained from TCAD (cross symbols) and model (7) (solid lines) for optimized five-finger structures. The data in black are obtained for optimized set of spacing with values $S = [2, 3, 3, 2] \mu\text{m}$. Note that the corner finger temperatures in optimized structures are more even with lower peak temperature than in uniformly spaced structures (data in red). The optimization routine attempts to obtain a relatively uniform temperature across the fingers. However, for a given footprint where thermal coupling is inevitable, non-uniformity in spatial temperature cannot be completely eliminated. Our algorithm that utilizes analytical formulations, essentially attempts to minimize this non-uniformity. In Fig. 7, for a given emitter geometry and P_d we present $T_{i,true}$ values corresponding to the optimized finger spacing obtained from the optimization algorithm for six and seven-finger structures with-ST. Finger temperatures of uniformly spaced structure are also plotted for a direct comparison. Since the thermal coupling at the corner fingers Fin-1 and Fin-6 (or Fin-7) is one sided (either from right or left), their optimized $T_{i,true}$ values are the lowest among all the fingers. The optimized trend of total temperature demonstrated in Fig. 7 is similar to the previously reported ones in [11], [12]. The optimized spacing values obtained here are independent of the power dissipation at the fingers. Fig. 8 presents the P_d -dependent $T_{i,true}$ of all four fingers in an optimized seven finger ST-isolated structure with a particular emitter geometry. The data points obtained from the model (solid line) and TCAD simulation (symbols) corresponding to the same finger spacing are also plotted for validation purpose. We have also plotted $T_{i,true}$ values of the central (4th) finger from the uniformly spaced structure to highlight the temperature reduction due to optimization.

V. CONCLUSIONS

This work provides a simple finger spacing optimization framework for thermally aware design of multi-finger transistors with shallow trench isolation. The framework comprises of an iterative optimization algorithm and a new physics-based model for accurate prediction of the total junction temperature. The model includes the linear finger temperature rises due to self-heating and thermal coupling effects and employs Kirchhoff's transformation based expression to predict the true total temperature for all the fingers of a transistor. Model is first validated and calibrated against 3D TCAD simulations and subsequently against experimental data after incorporating the effect of back-end-of-line. Excellent model agreement is observed with the values of true finger temperatures from TCAD and the ones extracted from the measurement data of fabricated devices. The model is implemented in an optimization algorithm to achieve the optimized non-uniform

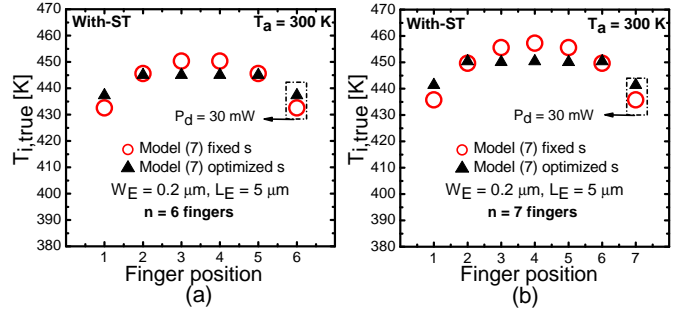


Fig. 7. Comparison of total temperature distribution obtained from the proposed algorithm in Fig. 4 when applied to ST isolated structures with uniform finger spacing (red circles) and that with optimized finger spacing (black triangles): (a) for a six-finger device with optimized spacing $S = [1.73, 3.16, 2.73, 3.16, 1.73] \mu\text{m}$ and (b) a seven-finger device with optimized spacing $S = [1.72, 2.81, 2.97, 2.97, 2.81, 1.72] \mu\text{m}$.

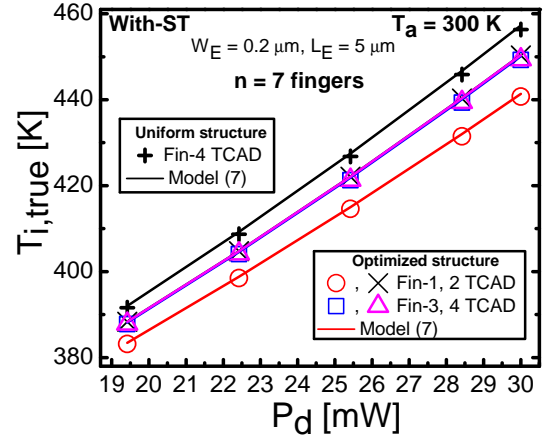


Fig. 8. Dissipated power dependent true temperatures of all four fingers obtained for structures with optimized spacing and emitter area of $A_E = 0.2 \times 5 \mu\text{m}^2$. Results from the model (solid lines) are compared against TCAD (symbols).

finger spacing values in order to minimize the overall non-uniformity in the spatial temperature distribution across the fingers. Obtained values of optimized finger spacing are found to be independent of power dissipation and give rise to an almost uniform temperature distribution across all the fingers of a multi-finger device. The proposed framework is scalable for transistors with different emitter dimensions and any number of fingers.

REFERENCES

- [1] U. Erben, M. Wahl, A. Schuppen, and H. Schumacher, "Class-a sige hbt power amplifiers at c-band frequencies," *IEEE Microwave and Guided Wave Letters*, vol. 5, no. 12, pp. 435–436, 1995. doi: <https://doi.org/10.1109/75.481852>.
- [2] W. Liu, "Thermal coupling in 2-finger heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, no. 6, pp. 1033–1038, 1995. doi: [10.1109/16.387234](https://doi.org/10.1109/16.387234).
- [3] J. M. Andrews, C. M. Grens, and J. D. Cressler, "Compact modeling of mutual thermal coupling for the optimal design of SiGe HBT power amplifiers," *IEEE Trans. Electron Devices*, vol. 56, no. 7, pp. 1529–1532, 2009. doi: [10.1109/TED.2009.2021365](https://doi.org/10.1109/TED.2009.2021365).

- [4] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: part II—Two-finger devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2022–2033, 2005. doi: 10.1109/TED.2005.854275.
- [5] D. J. Walkey, T. J. Smy, R. G. Dickson, J. S. Brodsky, D. T. Zweidinger, and R. M. Fox, "Equivalent circuit modeling of static substrate thermal coupling using VCVS representation," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1198–1206, 2002. doi: 10.1109/JSSC.2002.801200.
- [6] Y. Zimmermann, "Modeling of spatially distributed and sizing effects in high-performance bipolar transistors," *Dipl.-Ing.(MSEE) thesis, Chair Electron Devices Integr. Circuits, Technische Univ. Dresden, Dresden, Germany*, 2004.
- [7] G.-B. Gao, M.-Z. Wang, X. Gui, and H. Morkoc, "Thermal design studies of high-power heterojunction bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 36, no. 5, pp. 854–863, 1989. doi: <https://doi.org/10.1109/16.299666>.
- [8] L. La Spina, N. Nenadović, V. d'Alessandro, F. Tamigi, N. Rinaldi, L. Nanver, and J. Slotboom, "Thermally induced current bifurcation in bipolar transistors," *Solid-State Electronics*, vol. 50, no. 5, pp. 877–888, 2006. doi: <https://doi.org/10.1016/j.sse.2006.04.006>.
- [9] N. Rinaldi and V. d'Alessandro, "Theory of electrothermal behavior of bipolar transistors: Part III—Impact ionization," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1683–1697, 2006. doi: 10.1109/TED.2006.876285.
- [10] A. Metzger, V. d'Alessandro, N. Rinaldi, and P. Zampardi, "Evaluation of thermal balancing techniques in InGaP/GaAs HBT power arrays for wireless handset power amplifiers," *Microelectronics Reliability*, vol. 53, no. 9, pp. 1471–1475, 2013. doi: <https://doi.org/10.1016/j.microrel.2013.06.013>.
- [11] G. Wang, C. Qin, N. Jiang, and Z. Ma, "Boosting up performance of power sige hbt's using advanced layout concept," in *Digest of Papers. 2004 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2004.*, 2004, pp. 135–138. doi: 10.1109/SMIC.2004.1398186.
- [12] Z. Wan-rong, J. Dong-yue, Y. Jing-wei, H. Li-jian, S. Yong-ping, W. Yang, and Z. Wei, "Improvement of thermal stability of multi-finger power SiGe HBTs using emitter-ballasting-resistor-free designs," in *2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, 2006, pp. 221–223. doi: 10.1109/IC-SICT.2006.306167.
- [13] A. Gupta, K. Nidhin, S. Balanethiram, S. Yadav, A. Chakravorty, S. Fregonese, and T. Zimmer, "Static Thermal Coupling Factors in Multi-Finger Bipolar Transistors: Part I—Model Development," *Electronics*, vol. 9, no. 9, 2020. doi: <https://doi.org/10.3390/electronics9091333>.
- [14] —, "Static Thermal Coupling Factors in Multi-Finger Bipolar Transistors: Part II—Experimental Validation," *Electronics*, vol. 9, no. 9, 2020. doi: <https://doi.org/10.3390/electronics9091365>.
- [15] A. Gupta, K. Nidhin, S. Balanethiram, R. D'Esposito, S. Fregonese, T. Zimmer, and A. Chakravorty, "Extraction of true finger temperature from measured data in multifinger bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 68, no. 3, pp. 1385–1388. doi: 10.1109/TED.2021.3054602, 2021.
- [16] T. T. Nghiêm, J. Saint-Martin, and P. Dollfus, "Electro-thermal simulation based on coupled Boltzmann transport equations for electrons and phonons," *Journal of Computational Electronics*, vol. 15, no. 1, pp. 3–15, 2016. doi: <https://doi.org/10.1007/s10825-015-0773-2>.
- [17] J.-S. Rieh, D. Greenberg, B. Jagannathan, G. Freeman, and S. Subbanna, "Measurement and modeling of thermal resistance of high speed SiGe heterojunction bipolar transistors," in *Proc. Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2001, pp. 110–113. doi: 10.1109/SMIC.2001.942350.
- [18] S. Balanethiram, A. Chakravorty, R. D'Esposito, S. Fregonese, D. Céli, and T. Zimmer, "Accurate modeling of thermal resistance for on-wafer SiGe HBTs using average thermal conductivity," *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3955–3960. doi: 10.1109/TED.2017.2724939, 2017.
- [19] G. Goh, U. Kim, M.-S. Jeon, and J. Kim, "A simple extraction method of thermal resistance in multifinger GaAs HBT," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2620–2624. doi: 10.1109/TED.2016.2556086, 2016.
- [20] T. Synopsys, "Sentaurus: Sentaurus device user guide, release H-2013.03," 2013.
- [21] P. Chevalier et al., "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T /370 GHz f_{max} HBT and high-Q millimeter-wave passives," 2014, pp. 3.9.1–3. doi: 10.1109/IEDM.2014.7046978.
- [22] S. Lehmann, Y. Zimmermann, A. Pawlak, and M. Schroter, "Characterization of the static thermal coupling between emitter fingers of bipolar transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3676–3683, 2014. doi: 10.1109/TED.2014.2359994.
- [23] S. Balanethiram, R. D'Esposito, A. Chakravorty, S. Fregonese, and T. Zimmer, "Extraction of BEOL contributions for thermal resistance in SiGe HBTs," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 1380–1384, 2017. doi: 10.1109/TED.2016.2645615.