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Study of water-soluble Polyethylene oxide (PEO) polymer based CBRAM devices

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In this research work, Conductive bridge Random Access memory devices (CBRAMs) featuring a water-solution processed Polyethylene Oxide (PEO) layer used as solid polymer electrolyte were fabricated. The devices showed promising results with forming-free capabilities, switching voltages within the range from -1.5 V to 2.0 V, high OFF/ON resistance ratio ~10^5 and >300 cycles each at 10 & 100 µA compliance current (CC). Cycling at various CC also confirmed that the conductive filament was more stable at higher compliance current with a higher probability to achieve non-volatile switching. This article also reports the conduction mechanism in the high and low resistance states for PEO based devices. Finally, due to their high OFF/ON current ratio, it is suggested that these devices could also serve as BEOL (Back-End-Of-Line) selector devices while operating in their volatile mode.

Keywords: CBRAMs, PEO, resistive switching, selectors, water solvent

1. Introduction

Resistive RAMs have gained great interest in the field of emerging non-volatile memories due to their low energy consumption < 0.1 pJ, downscaling abilities < 10 nm, sub-ns operating speed and high endurance cycles (>10^{12}) [1]–[6]. Among them, Conductive Bridge Random Access Memories (CBRAMs) rely on the formation or dissolution of conductive paths of Ag or Cu on application of voltage within a solid electrolyte, resulting into switching between two states, which is in general, stochastic in nature [4][5]. Their simple Metal Insulator Metal (MIM) architecture enabling solution processed solid polymer electrolyte layer and compatibility with flexible substrates makes them appealing

for further research in the field of flexible and sustainable electronics [6], [7]. CBRAMs consist of three layers - an active electrode (Ag or Cu), a solid electrolyte layer and an inert counter-electrode. Generally, the solid electrolyte layer consists of metallic oxides, chalcogenides alloys or porous materials [8]–[9]. However, it has been recently shown that this layer can be replaced by polymers to ease the process ability and promote compatibility with flexible substrates [10]–[15].

Polyethylene Oxide (PEO) with its attractive features of good binding, film forming properties, high chemical stability, flexibility, low cost and water solubility is used as the solid polymer electrolyte layer [16], [17]. Further, PEO brings additional advantages with respect to other demonstrated solid polymer electrolytes such as polymer blends like PVP with 2-Amino-5-Methyl-1,3,4-thiadiazole or Polyimide with PCBM (6-phenyl-C61 butyric acid methyl ester) used as SPE layer [18][19]. Firstly, for the processing of the PEO polymer, no polymer blends are required. Secondly, PEO can be dissolved in non-toxic, readily available green solvent such as water, reducing the overall ecological footprint of the fabrication process, whereas for other SPEs precursors and chemical solvents are required for their deposition. Previous research works on Poly-Ethylene Oxide (PEO) based CBRAMs have shown results on silicon, glass and flexible substrates workable with low operating voltages and >100 endurance cycles [20]–[23]. However, their studies have mainly used acetonitrile (ACN) as solvent for PEO deposition which is toxic in nature with limitations in electrical performance. Carrying forward, this work, for the first time reports optimization on the fabrication step- by presenting the critical thickness of PEO layer, study on the conduction mechanism in detail and relates it's electrical performance with applications, as selectors. Upon giving the fabrication details, the devices were fabricated with three different PEO thicknesses 30, 50 & 150 nm. Further, devices were subjected to cycling at two different compliance currents 10 and 100 µA. Programming voltages together with Low and High Resistance State (namely LRS, HRS) were extracted and analysed. A study on the conduction mechanism of the devices is presented, in the HRS and LRS respectively. The final part of the paper discusses the possibility of exploiting volatile switching to achieve BEOL selector devices.

2.Experimental

2.1. Device fabrication

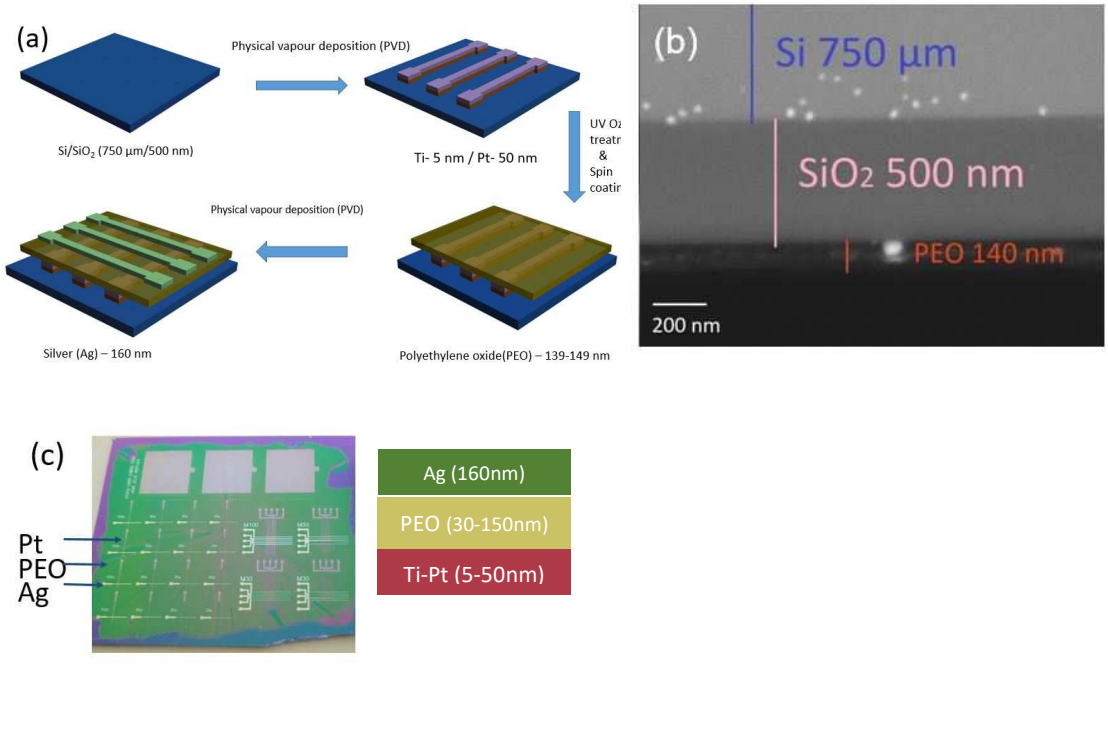

Fig. 1 (a) The sketch shows stepwise procedure of fabrication of the CBRAM devices. (b) SEM image of the cross section of the devices. (c) Fully fabricated CBRAM devices with the different layers and cross section scheme of the deposited layers.

Samples featuring a PEO layer of 30, 50 and 150 nm were fabricated following the schematic fabrication procedure illustrated in Fig. 1(a). Firstly, the substrate was dried with N_2 and thereafter, an adhesive Titanium layer (5 nm) and bottom Platinum (50 nm) electrodes were patterned by using electron beam evaporation through a solid shadow mask. Samples were then cleaned with Iso-propyl-alcohol (IPA), Ethanol and Acetone and dried again with N_2. UV-Ozone treatment of the surface was then performed for 20 minutes with UVO cleaner (Model number 42A-220) in order to increase the hydrophilicity of the substrate and promote adhesion of the polymer layer. A polymer solution was prepared from pure PEO (Sigma Aldrich Chemistry) Mw 600 000 g/mol, mixed with deionized water to obtain a solution concentration of 20 g/L for spin coating.

More details concerning the solution preparation and spin coating parameters can be found in reference [13]. Finally, a 150 nm-thick top electrode silver (Ag) was deposited by electron beam evaporation. Scanning Electron Microscopy (SEM) images were acquired on the cross section of PEO layer, by cleaving Si/SiO_2 layer with a diamond tip pen with Mira Tescan on devices subjected to 5 kV voltage and SEM magnification of 151 kX. Fig. 1(b) showing cross section image of the PEO layer obtained on Si/SiO_2. The corresponding set of fully fabricated devices is shown in Fig. 1(c).

2.2. Electrical Characterization

The electrical characterization of the devices was carried out with a Keithley SCS 4200A parameter analyser using quasi-static voltage ramps ranging from -1.5 V to 2.0 V and at set compliance current of 10 & 100 µA respectively. This range was obtained by progressively subjecting the device from 0 to 1 V for set and 0 to -1 V for reset.

3. Results and discussion

3.1. Workability of devices with various PEO thicknesses

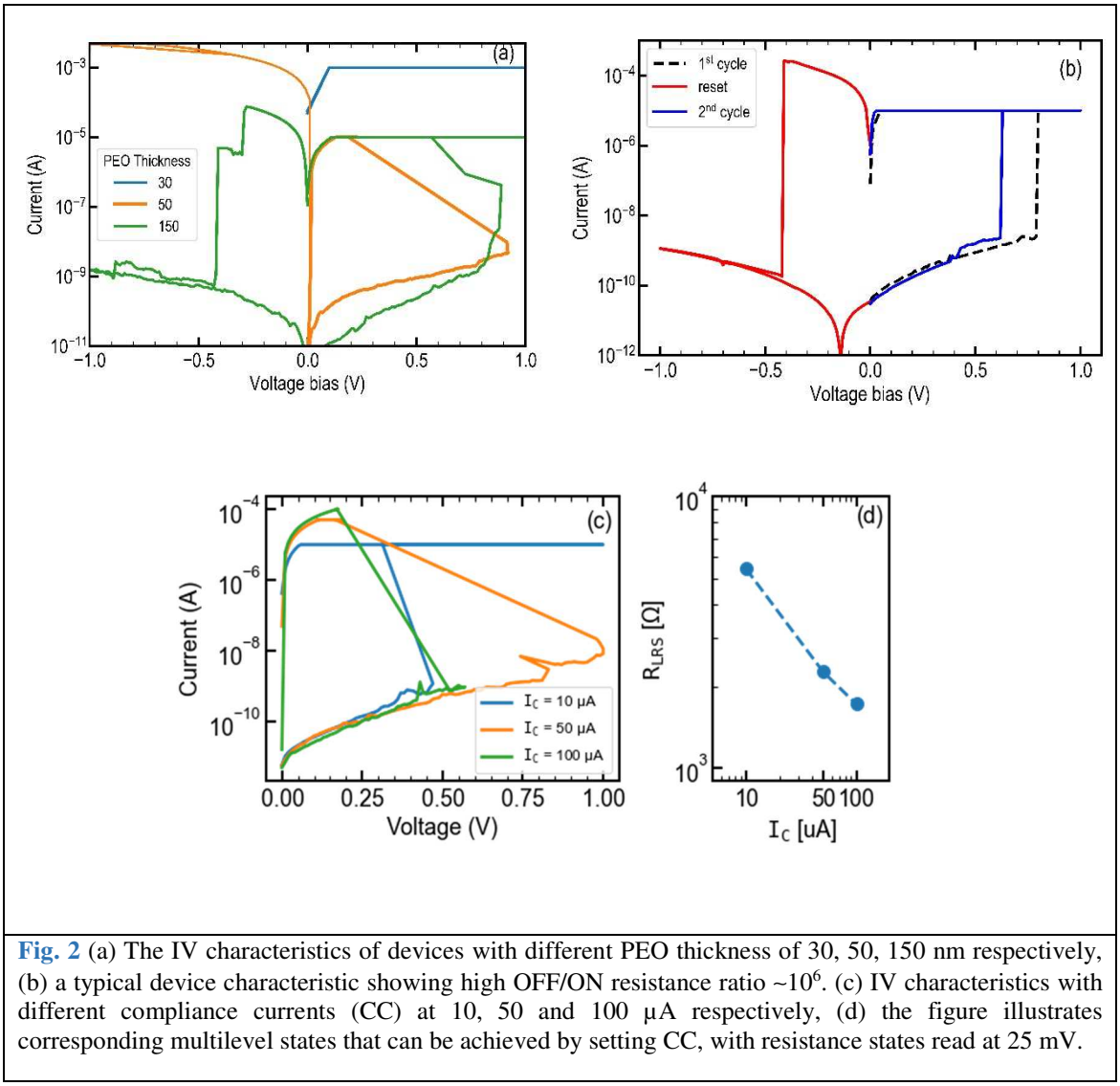

Fig. 2 (a) The IV characteristics of devices with different PEO thickness of 30, 50, 150 nm respectively, (b) a typical device characteristic showing high OFF/ON resistance ratio ~10^6. (c) IV characteristics with different compliance currents (CC) at 10, 50 and 100 µA respectively, (d) the figure illustrates corresponding multilevel states that can be achieved by setting CC, with resistance states read at 25 mV.

Fig. 2(a) shows typical IV curves of devices with three different PEO thicknesses: 30, 50 and 150 nm. Devices with a 30 nm thick PEO films were systematically short circuited, while those with a 50 nm thick PEO exhibited set switching but were then stuck in a Low Resistance State (LRS). Such a behaviour can be related to diffusion of Ag through the thin PEO layer during e-beam evaporation leading to fully non-functional devices. Finally, the 150 nm thick PEO CBRAM devices showed complete set and reset phenomena. Following this, our study further focuses exclusively on the investigation of 150 nm PEO layer devices. Fig. 2(b) depicts the switching of one of the devices, showing high OFF/ON

resistance ratio~10^6 and forming free programming voltages ~ 0.75 V. Taking the advantage of such characteristics, Fig. 2(c)-(d) shows the possibility of storing multilevel states by setting up compliance current (CC) as 10, 50 & 100 µA respectively.

3.2. Cycling at various compliance currents

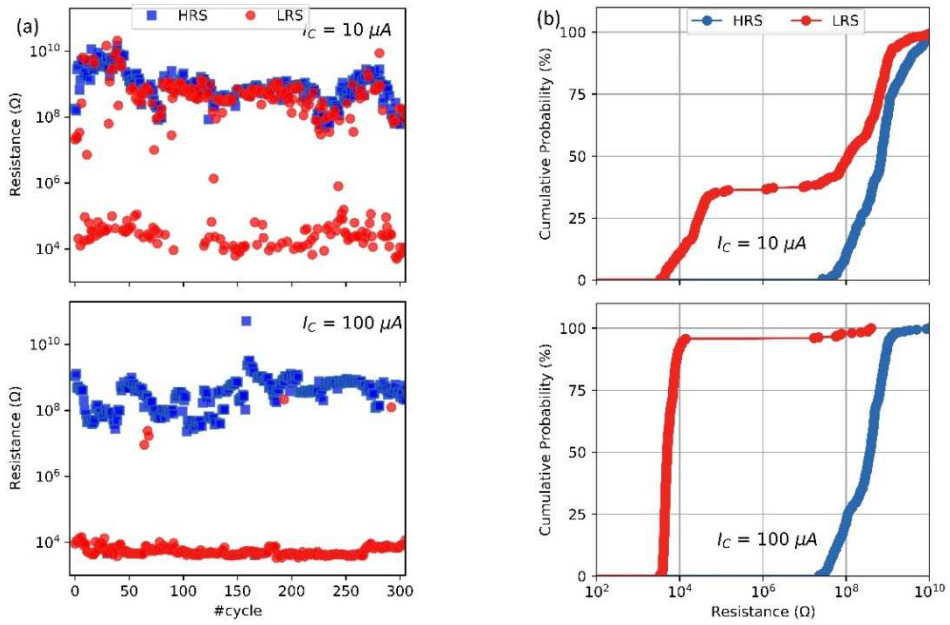

Fig. 3 (a) LRS and HRS along cycling at a CC of 10 and 100 µA. (b) Cumulative resistance distribution at current compliance levels of 10 and 100 µA read at 50 mV.

Low and High Resistance State (LRS/HRS) were evaluated during cycling at various current compliances. Devices were subjected to back and forth voltage sweeps with current compliance used exclusively for positive voltage sweeps. After applying a negative voltage sweep, the HRS was evaluated by reading the current at 50 mV on the subsequent forward positive sweep while the LRS was taken at the same voltage on the backward sweep. Fig. 3(a) shows endurance cycles performed on a device at 10 & 100 µA CC, while Fig. 3(b) shows the corresponding cumulative resistance distributions. Large LRS values (solid red points) greater than 10^6 Ω can be observed in Fig. 3(a) mostly when the current compliance was decreased from 100 to 10µA. These failed set states correspond to volatile switchings where devices spontaneously come back to their HRS

during the backward sweeps and are discussed more in details below. It is observed that our devices in 1R configuration withstood more than 300 cycles each without breakdown. Limited endurance cycles ($<10^3$) can be explained by the parasitic current overshoots commonly observed when using voltage sweeps combined with current compliances as exposed by Tirano *et al.* [24]. Hence 1T1R configurations or using short-pulse measurements would probably be more suitable to observe optimal performances. As illustrated in Fig. 3(b), besides, the large electrical variability observed at lower current compliance, the most striking feature concerns the overlap of the LRS/HRS distribution, mostly occurring at a compliance current of 10 µA. As discussed later, this feature can be attributed to volatile switching occurring at low CC, where a spontaneous breakdown of the conductive filament is observed during the backward voltage sweep.

Focusing on non-volatile switching, Fig. 4 shows the resistance distributions, presented as boxplots, obtained at both compliance currents in LRS and HRS. Fig. 4 was obtained from Fig. 3 by excluding LRS values greater than 1 MΩ; this criterion efficiently allows to distinguish volatile and non-volatile switching as exposed in the next section. As can be seen, the decrease of electrical variability together with LRS resistance was confirmed through the decrease of the ratio between the standard deviation (σ) and mean value (µ) at increasing current compliance[25], [26].

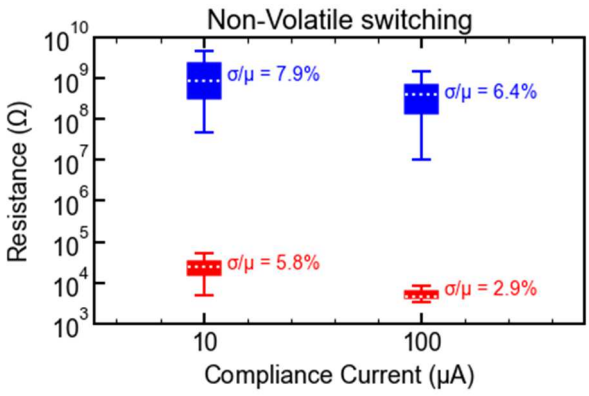

Fig. 4 Box plots of LRS/HRS at 10 µA and 100 µA current compliance restricted to the Non-volatile switching ($R_{LRS}>10^6$ Ω). Values in inset indicate the ratio between the standard deviation and mean value of the resistance distribution.

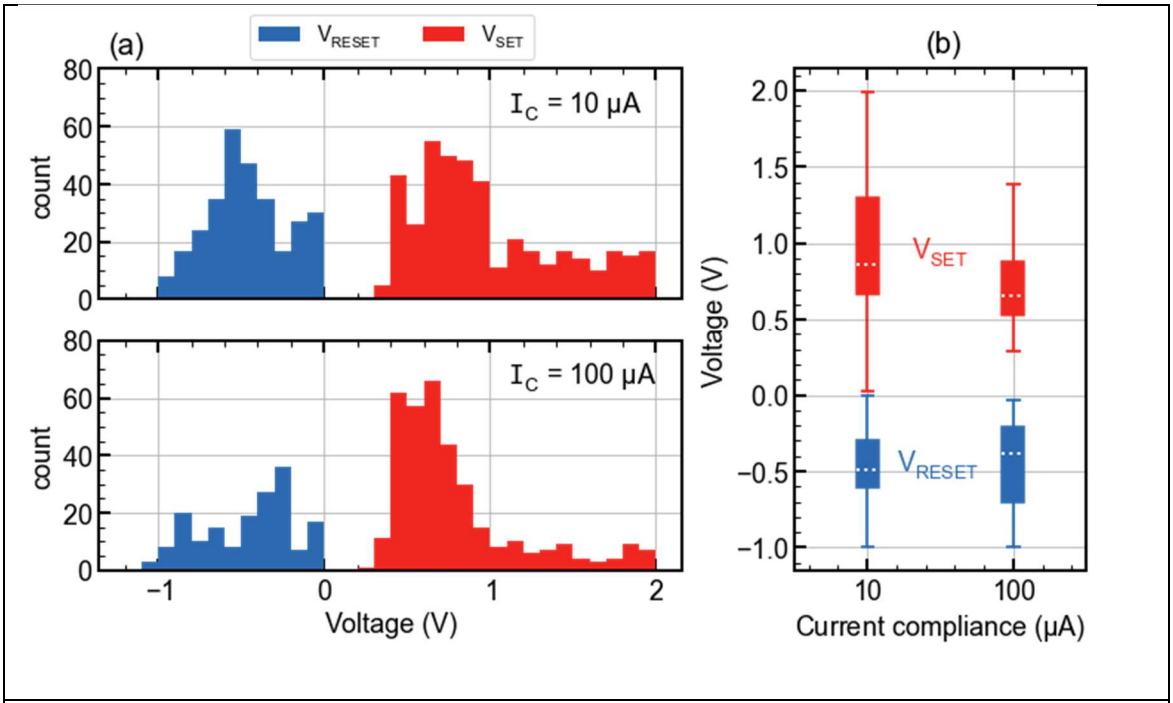

Fig. 5 (a) Programming voltage distribution and (b) corresponding boxplots for 10 µA 100 µA compliance currents.

Set/reset voltages histograms and box plots are respectively shown in Fig. 5(a) & (b) at compliance currents (CC) of 10 & 100 µA. A lower variability in set voltages are observed for 100 µA CC. A possible cause for such behaviour can be that the residual filament after reset is larger or features more ramifications, due to more incorporation of Ag within the solid electrolyte; therefore, a lower voltage/electric field would be then required to reform the complete filament during the subsequent set operation. The characterization of these PEO based CBRAM devices has been carried out for several months showing insignificant change in performance of switching, hence proving their fair stability.

3.3. Study of the conduction mechanism in LRS and HRS

Conduction mechanism was studied on Ag/PEO/Pt devices along 300 set cycles measured at ambient temperature with a set compliance current of 100 µA. A careful inspection of

the data was undertaken in order to exclude any volatile switching from this study. Fig. 6(a) shows the current density (J) as a function of the electric field (E) computed as the ratio between the applied voltage and the PEO nominal thickness of 150 nm measured with a profilometer; current density and electric field in logarithmic scales, along the 300 cycles. The linear behaviour suggests ohmic conduction which can be captured through the following equation:

$$J = \sigma E^{\gamma} \quad (1)$$

Where σ is the electrical conductivity, E the electric field and γ a field factor which is assumed to be equal to 1 for ohmic conduction. σ and γ values were extracted for each IV curve and their distribution plotted in Fig. 6(b)&(c) respectively. With an average γ value of 1.0, ohmic conduction is undoubtedly confirmed in the LRS with an average conductivity of 2.9×10^{-2} *S/m*.

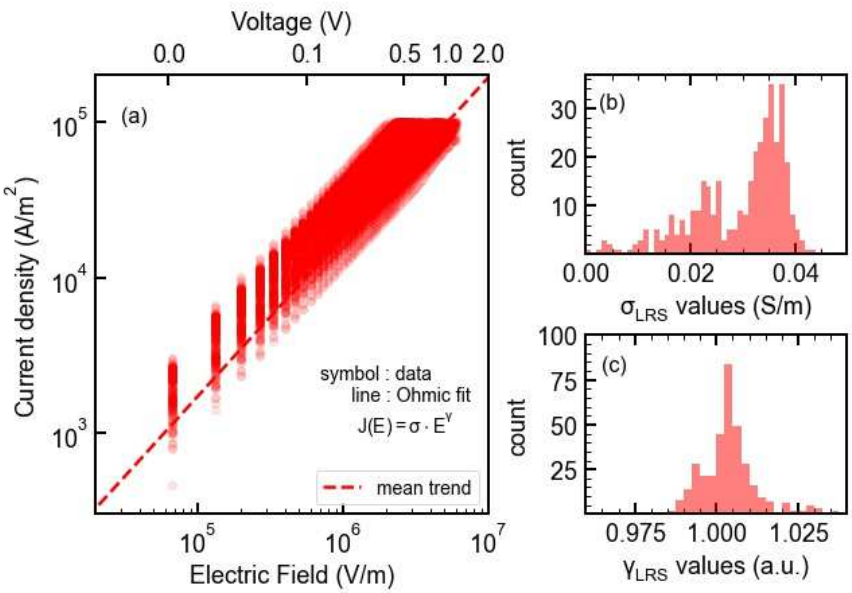

Fig. 6 Study of LRS at CC of 100 µA. (a) J-E plots corresponding to 300 cycles and Ohmic fit using eq. 1 together with mean values of σ and γ extracted from histograms presented in (b) and (c) respectively.

Similar studies were conducted on the high resistance state (HRS) of our Ag/PEO/Pt devices, as illustrated in Fig. 7. From Fig. 7(a) it can be seen that J-E curves still exhibit a linear behaviour before approaching Set voltage (i.e. 0V≤V≤0.5V). However, as shown in Fig. 7(b)&(c) the average conductivity fell to $0.68\ nS/m$ while the extracted field factors were ranging between 0.8 and 2.0.

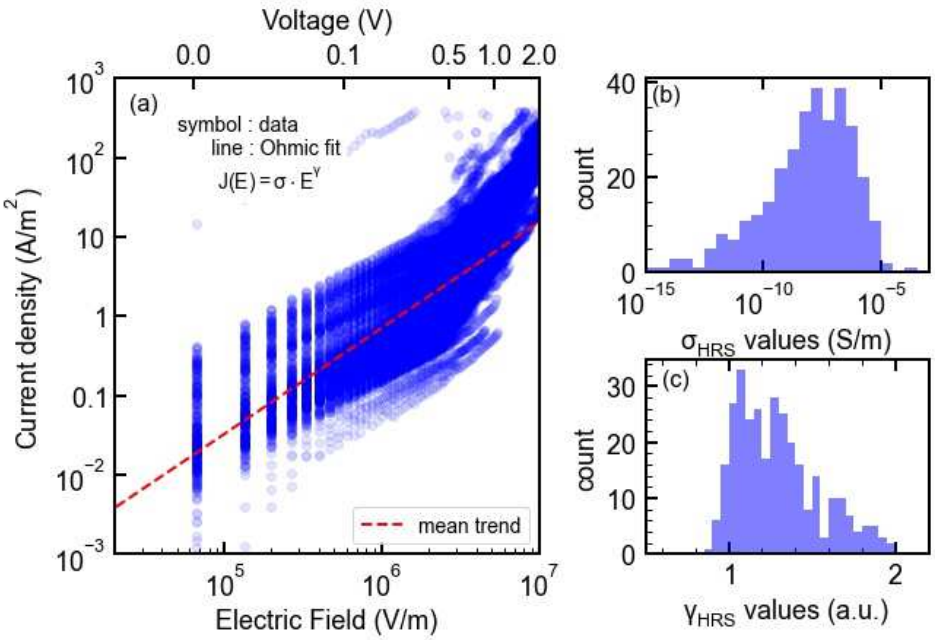

Fig. 7 Study of HRS for Ic =100 µA. (a) J-E plots and Ohmic fit using eq. 1 together with mean values of σ and γ extracted from histograms (b) and (c).

The drastic decrease of the electrical conductivity can be attributed to the filament breakdown leaving the PEO layer as the main contributor for HRS current and is consistent with the large ON/OFF resistance ratio observed on our devices. In order to evaluate the intrinsic conductivity of PEO, a reference Pt/PEO/Pt device was investigated through temperature measurements ranging from 230 to 330K. As shown in Fig. 8(a) J-E curves exhibited a linear behaviour together with temperature-activated electrical conductivity. In order to catch the temperature-dependency, an Arrhenius law was introduced in Eq. (1) as follows:

$$J = \sigma_0 \, e^{-\frac{E_a}{k_b T}} E^{\gamma} \quad (2)$$

where σ_0 is the high-temperature conductivity, E_a the conduction activation energy and k_bT the thermal energy. The Arrhenius plots of Fig. 8(b)&(c) show that γ remained almost constant with temperature with a mean value of 1.36 while the high-temperature conductivity (σ_0) and conduction activation energy (E_a) were extracted with respective values of $46.4 \times 10^5 \, nS/m$ and 0.41 eV. From these values, the effective conductivity at ambient temperature (300 K) was evaluated to be $0.51 \, nS/m$. This conductivity value together with γ extracted on Pt/PEO/Pt device is consistent with values those obtained on Ag/PEO/Pt in the HRS state (Fig. 7) and suggest that HRS conduction is mostly controlled by the PEO solid-electrolyte. Finally, the HRS field factor ranging between 0.9 and 2.0 can be indicative of a mixed conduction regime involving both Ohmic conduction (γ=1) and Space Charge Limited Current (γ=2)[27], [28].

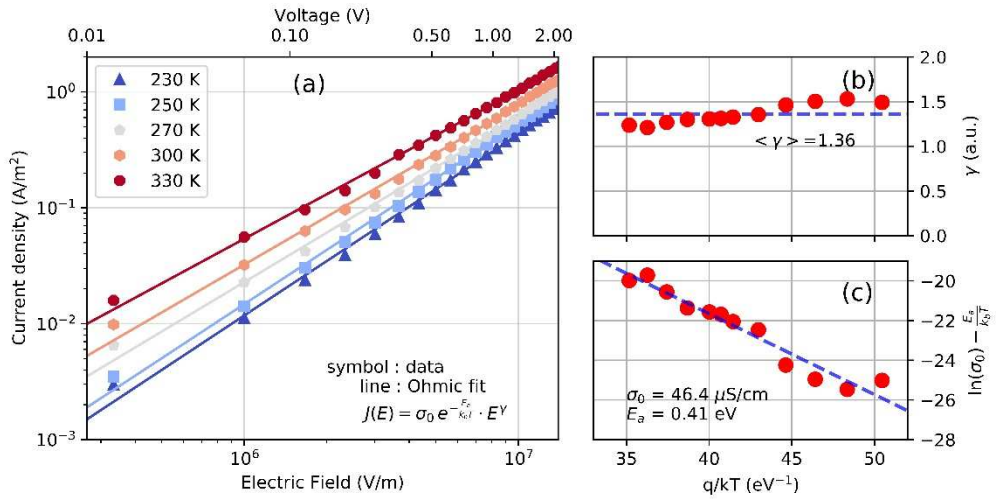

Fig. 8 Study of Pt/PEO/Pt reference device. (a) J-E plots at various temperatures from 230 to 330 K (b) and (c). The J-E curve of the reference Pt-PEO-Pt recorded at 300 K is shown in (a) for comparison.

3.4. Volatile CBRAMs as selectors

As stated in the previous section, devices programmed at a 10 µA CC mostly returned to the HRS during the backward sweep from the positive voltage bias leading to a volatile-switching. This behaviour is illustrated in Fig. 9(a) showing both a non-volatile and a volatile switching cycle. The spontaneous breakdown of the conductive filament (CF) at low voltages can be related to weakness of the CF at low CC due to the dependency of its size (area) on the compliance current as exposed in previous research works [29], [30]. It has been mentioned that the cross sectional area of the CF decreases with decrease in CC , with theoretical investigations showing that reducing the CF diameter by 5 times would decrease the lifetime of the CF by 150 times [26], [29], [30]. Such type of volatile switching was related to the surface diffusion of Ag clusters into the dielectric material [25].This leads to the computation of set failure rate of the devices. Based on the typical I-V curves presented in Fig. 9(a) and the LRS resistance distribution of Fig. 4, we evaluated the occurrence of volatile switching by considering LRS values (read at 50 mV) exceeding 1MΩ. This threshold resistance value being intermediate state between the HRS and non-volatile LRS states, allowed a systematic distinction between both types of switching events.

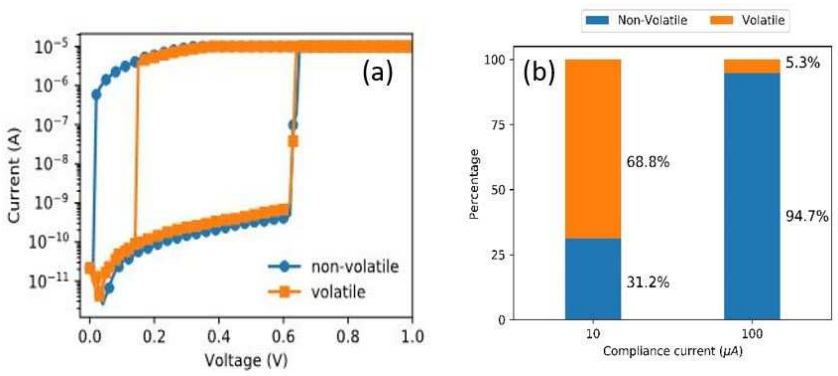

Fig. 9 (a) I-V curves illustrating a volatile and non-volatile switching. (b) Percentage of volatile and non-volatile switching obtained at CC of 10 and 100 µA respectively.

The percentage of the non-volatile and volatile switching was then calculated for each compliance current and presented in Fig. 9(b). While almost 95% of the obtained

switching were non-volatile at a compliance current of 100 µA, more than 68% were volatile as the current compliance was decreased to 10 µA.

Such volatile CBRAMs can be exploited as selectors to suppress sneak paths in large crossbar arrays [31]–[36]. These selectors devices can then suppress such leakage current in 1S-1R configuration at each cross point [37]. A selector is in ON state above a threshold value of voltage with an abrupt increase in resistance, hence supplying current only to the selected cell. In a similar way in the low voltage regime, the selector returns in its OFF state below a hold voltage (V_{hold}) as shown in Fig. 10(a), which hinders leakage current flow through the half-selected cells. Fig. 10(b) & (c) shows the extracted hold voltages and ON/OFF current ratio with median values 70 mV and $2x10^4$ respectively.

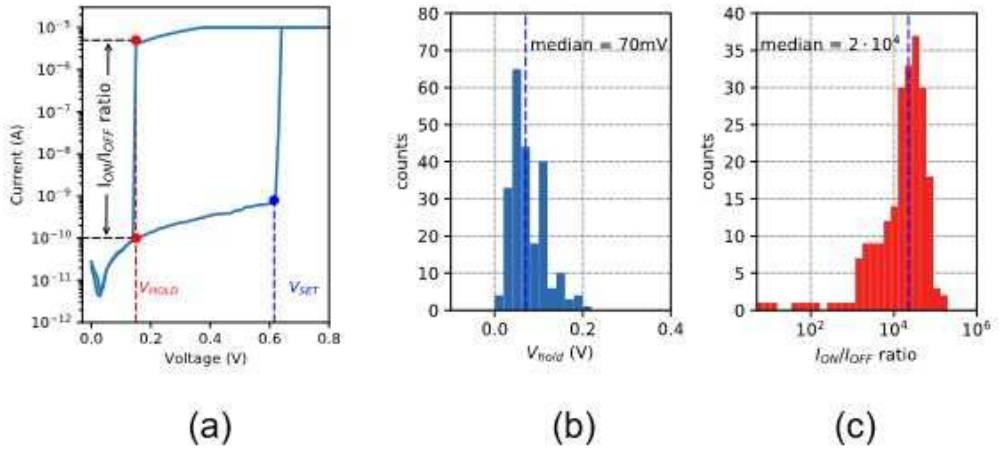

Fig. 10 (a) Definition of hold voltage (V_{Hold}) and (b) distribution of V_{Hold} and (c) $I_{ON/OFF}$ achieved at 10 µA compliance current.

Table 1 shows comparison of the figure of merits- non linearity and voltage margin for different RRAMs used as selectors making our CBRAM devices suitable candidates as selectors when operated at 10 µA CC. Non linearity ratio is the $I_{ON/OFF}$ ratio during the backward sweep as shown in Fig. 10(a), whereas the voltage margin is defined as the difference between the V_{set} and V_{hold} accounting for the variability of performance of a selector. With high non-linear ratio ~ 10^5 and voltage margin 0.7 V allowing good

selectivity, our polymer-based devices are competitive with other reported selector devices based on inorganic materials. Extending the scope of our previous studies [13], this work suggests that PEO-based devices can be an affordable and sustainable way to develop both resistive and selector devices for applications such as low-cost flexible electronics applications.

Table 1 Comparison of the figure of merits- non linearity and voltage margin for different RRAMs

Reference	**Materials**	**Non linearity ratio = $I_{ON/OFF}$ ratio**	**Voltage Margin = V_{set} - V_{hold}(V)**
[31]	Cu/Ti/HfO_2/TiO_2	3×10^3	~ 1
[32]	Ag/TiO_2/Pt	10^7	~ 0.10
[38]	Ag/SiTe/HfO_2/TiN	10^7	~ 0.70
[39]	TiN/Ta_2O_5/TiN	$3.3X10^3$	~ 0.75
[35]	Ni/TiO_2/Ni	10^3	~ 2.0
[36]	Ag /HfO_x/ Pd	10^{10}	~0.15
This work	*Ag/PEO/Pt*	*10^5*	*~0.70*

used as selectors

Moreover, in this work we achieved the advantage of low cost and low-temperature process so that it can be integrated in the back-end-of-line (BEOL) where thermal budget is strictly limited to 450°C. A comparison of OFF/ON resistance ratio enabling multilevel states between different CBRAMs based on polymers is made in Table 2.

Table 2 Summarizes the OFF/ON resistance ratio of CBRAMs based on different SPE layers

[40]	PI:PCBM	10^4
[41]	EMAR : CNTs	10^4
[19]	PCBM :MoS_2	10^3
[42]	PVP :PMF	10^5
This work	*Polyethylene oxide (PEO)*	*~10^5*

4. Conclusion

In this work, CBRAM devices based on a water casted Polyethylene oxide (PEO) solid polymer electrolyte layer were fabricated and investigated. With switching voltages ranging between -1.5 V and +2 V, high OFF/ON resistance ratio (~10^5) and fair cycling capabilities in 1R configuration, these devices exhibited promising performances in the field of low-cost and low-thermal budget non-volatile memory. Through a statistical study conducted at a current compliance of 100 µA over 300 measurements, ohmic transport was unambiguously confirmed in LRS while a super linear conduction regime was observed in HRS. The latter conduction regime was also confirmed on a reference device featuring inert electrodes. This behaviour was attributed to a mixed contribution of ohmic transport and Space-Charge-Limited-Conduction in the PEO layer. Decreasing the current compliance down to 10 µA lead to an increase of both the electrical variability (both in LRS and HRS) and of the occurrence of volatile switching. In this context, it was suggested that such volatile CBRAM, may be exploited as selector devices given the high non-linearity of their switching characteristics and high ON/OFF ratio. In conclusion, PEO based water casted CBRAMs are promising candidates for moving towards sustainable technology.

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References:

[1] A. C. Torrezan, J. P. Strachan, G. Medeiros-ribeiro, and R. S. Williams, "Sub-nanosecond switching of a tantalum oxide memristor," vol. 485203, doi: 10.1088/0957-4484/22/48/485203.

[2] B. J. Choi *et al.*, "Electrical performance and scalability of Pt dispersed SiO 2 nanometallic resistance switch," 2013, doi: 10.1021/nl401283q.

[3] M. Lee *et al.*, "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta2O5-x/TaO2-x bilayer structures," *Nat. Mater.*, vol. 10, no. 8, pp. 625–630, 2011, doi: 10.1038/nmat3070.

[4] M. N. Kozicki and H. J. Barnaby, "Conductive bridging random access memory - Materials, devices and applications," *Semicond. Sci. Technol.*, vol. 31, no. 11, pp. 0–54, 2016, doi: 10.1088/0268-1242/31/11/113001.

[5] S. Guitarra, P. Mahato, D. Deleruyelle, L. Raymond, and L. Trojman, "Stochastic based compact model to predict highly variable electrical characteristics of organic CBRAM devices," *Solid. State. Electron.*, vol. 185, p. 108055, Nov. 2021, doi: 10.1016/j.sse.2021.108055.

[6] E. Linn, R. Rosezin, C. Kügeler, and R. Waser, "Complementary resistive switches for passive nanocrossbar memories," *Nat. Mater.*, vol. 9, no. 5, pp. 403–406, 2010, doi: 10.1038/nmat2748.

[7] W. Lu, D. S. Jeong, M. Kozicki, and R. Waser, "Electrochemical metallization cells — blending nanoionics into nanoelectronics ?," vol. 37, no. February, pp. 124–130, 2012, doi: 10.1557/mrs.2012.5.

[8] F. Zhuge *et al.*, “Mechanism for resistive switching in chalcogenide-based electrochemical metallization memory cells,” *AIP Adv.*, vol. 5, no. 5, pp. 0–8, 2015, doi: 10.1063/1.4921089.

[9] D. Deleruyelle *et al.*, “Ge2Sb2Te5 layer used as solid electrolyte in conductive-bridge memory devices fabricated on flexible substrate,” *Solid. State. Electron.*, vol. 79, pp. 159–165, 2013, doi: 10.1016/j.sse.2012.06.010.

[10] X. Yan *et al.*, “Flexible memristors as electronic synapses for neuro-inspired computation based on scotch tape-exfoliated mica substrates,” *Nano Res.*, vol. 11, no. 3, pp. 1183–1192, 2018, doi: 10.1007/s12274-017-1781-2.

[11] J. H. Lee, S. P. Park, K. Park, and H. J. Kim, “Flexible and Waterproof Resistive Random-Access Memory Based on Nitrocellulose for Skin-Attachable Wearable Devices,” *Adv. Funct. Mater.*, vol. 30, no. 1, p. 1907437, Jan. 2020, doi: 10.1002/adfm.201907437.

[12] B. Huber, P. B. Popp, M. Kaiser, A. Ruediger, and C. Schindler, “Fully inkjet printed flexible resistive memory,” *Appl. Phys. Lett.*, vol. 110, no. 14, 2017, doi: 10.1063/1.4978664.

[13] P. Mahato, E. Puyoo, D. Deleruyelle, and S. Pruvost, “CBRAM devices with a water casted solid polymer electrolyte for flexible electronic applications,” pp. 1–5, 2020, doi: 10.1109/nmdc47361.2019.9083996.

[14] N. Raeis-Hosseini and J. S. Lee, “Controlling the Resistive Switching Behavior in Starch-Based Flexible Biomemristors,” *ACS Appl. Mater. Interfaces*, vol. 8, no. 11, pp. 7326–7332, 2016, doi: 10.1021/acsami.6b01559.

[15] H. Tian *et al.*, “Cost-effective, transfer-free, flexible resistive random access memory using laser-scribed reduced graphene oxide patterning technology,” *Nano Lett.*, vol. 14, no. 6, pp. 3214–3219, 2014, doi: 10.1021/nl5005916.

[16] B. K. Money and J. Swenson, “Dynamics of Poly(ethylene oxide) around Its

Melting Temperature," *Macromolecules*, vol. 46, no. 17, pp. 6949–6954, Sep. 2013, doi: 10.1021/ma4003598.

[17] M. L. Verma and H. D. Sahu, "Study on ionic conductivity and dielectric properties of PEO-based solid nanocomposite polymer electrolytes," *Ionics (Kiel).*, vol. 23, no. 9, pp. 2339–2350, 2017, doi: 10.1007/s11581-017-2063-4.

[18] Y. Sun and D. Wen, "Nonvolatile WORM and rewritable multifunctional resistive switching memory devices from poly(4-vinyl phenol) and 2-amino-5-methyl-1,3,4-thiadiazole composite," *J. Alloys Compd.*, vol. 806, pp. 215–226, Oct. 2019, doi: 10.1016/j.jallcom.2019.07.217.

[19] W. Lv *et al.*, "Tunable Nonvolatile Memory Behaviors of PCBM − MoS 2 2D Nanocomposites through Surface Deposition Ratio Control," 2018, doi: 10.1021/acsami.7b16878.

[20] K. Krishnan, M. Aono, and T. Tsuruoka, "Kinetic factors determining conducting filament formation in solid polymer electrolyte based planar devices," *Nanoscale*, vol. 8, no. 29, pp. 13976–13984, 2016, doi: 10.1039/C6NR00569A.

[21] S. R. Mohapatra, T. Tsuruoka, K. Krishnan, T. Hasegawa, and M. Aono, "Effects of temperature and ambient pressure on the resistive switching behaviour of polymer-based atomic switches," *J. Mater. Chem. C*, vol. 3, no. 22, pp. 5715–5720, 2015, doi: 10.1039/C5TC00842E.

[22] S. Wu *et al.*, "A polymer-electrolyte-based atomic switch," *Adv. Funct. Mater.*, vol. 21, no. 1, pp. 93–99, 2011, doi: 10.1002/adfm.201001520.

[23] K. Krishnan, T. Tsuruoka, C. Mannequin, and M. Aono, "Mechanism for Conducting Filament Growth in Self-Assembled Polymer Thin Films for Redox-Based Atomic Switches," *Adv. Mater.*, vol. 28, no. 4, pp. 640–648, 2016, doi: 10.1002/adma.201504202.

[24] S. Tirano *et al.*, "Accurate analysis of parasitic current overshoot during forming

operation in RRAMs," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1129–1132, 2011, doi: 10.1016/j.mee.2011.03.062.

[25] W. Wang *et al.*, "Surface diffusion-limited lifetime of silver and copper nanofilaments in resistive switching devices," *Nat. Commun.*, vol. 10, no. 1, pp. 1–9, 2019, doi: 10.1038/s41467-018-07979-0.

[26] D. Ielmini, "Resistive switching memories based on metal oxides : mechanisms , reliability and scaling," *Semicond. Sci. Technol.*, vol. 31, no. 6, pp. 1–25, doi: 10.1088/0268-1242/31/6/063002.

[27] X. Zhang *et al.*, "Effect of Joule Heating on Resistive Switching Characteristic in AlOx Cells Made by Thermal Oxidation Formation," *Nanoscale Res. Lett.*, vol. 15, no. 1, 2020, doi: 10.1186/s11671-019-3229-y.

[28] E. Lim and R. Ismail, "Conduction Mechanism of Valence Change Resistive Switching Memory: A Survey," *Electronics*, vol. 4, no. 3, pp. 586–613, Sep. 2015, doi: 10.3390/electronics4030586.

[29] D. Ielmini, "Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4309–4317, Dec. 2011, doi: 10.1109/TED.2011.2167513.

[30] F. Nardi, S. Larentis, S. Balatti, D. C. Gilmer, and D. Ielmini, "Resistive Switching by Voltage-Driven Ion Migration in Bipolar RRAM—Part I: Experimental Study," *IEEE Trans. Electron Devices*, vol. 59, no. 9, pp. 2461–2467, Sep. 2012, doi: 10.1109/TED.2012.2202319.

[31] W. Banerjee and H. Hwang, "Understanding of Selector-Less 1S1R Type Cu-Based CBRAM Devices by Controlling Sub-Quantum Filament," *Adv. Electron. Mater.*, vol. 2000488, pp. 1–9, 2020, doi: 10.1002/aelm.202000488.

[32] J. Song, J. Woo, S. Lim, S. A. Chekol, and H. Hwang, "Self-Limited CBRAM with Threshold Selector for 1S1R Crossbar Array Applications," *IEEE Electron Device*

Lett., vol. 38, no. 11, pp. 1532–1535, 2017, doi: 10.1109/LED.2017.2757493.

[33] J. Song, J. Woo, A. Prakash, D. Lee, and H. Hwang, "Threshold Selector with High Selectivity and Steep Slope for Cross-Point Memory Array," *IEEE Electron Device Lett.*, vol. 36, no. 7, pp. 681–683, 2015, doi: 10.1109/LED.2015.2430332.

[34] B. Govoreanu, C. Adelmann, A. Redolfi, L. Zhang, S. Clima, and M. Jurczak, "High-performance metal-insulator-metal tunnel diode selectors," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 63–65, 2014, doi: 10.1109/LED.2013.2291911.

[35] J. J. Huang, Y. M. Tseng, C. W. Hsu, and T. H. Hou, "Bipolar nonlinear Ni/TiO2/Ni selector for 1S1R crossbar array applications," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1427–1429, 2011, doi: 10.1109/LED.2011.2161601.

[36] R. Midya *et al.*, "Anatomy of Ag / Hafnia-Based Selectors with 10 10 Nonlinearity," pp. 1–8, 2017, doi: 10.1002/adma.201604457.

[37] S. A. Chekol, J. Song, J. Park, J. Yoo, S. Lim, and H. Hwang, "Selector devices for emerging memories," in *Memristive Devices for Brain-Inspired Computing*, Elsevier, 2020, pp. 135–164.

[38] B. Song, R. Cao, H. Xu, S. Liu, H. Liu, and Q. Li, "A HfO 2 /site based dual-layer selector device with minor threshold voltage variation," *Nanomaterials*, vol. 9, no. 3, 2019, doi: 10.3390/nano9030408.

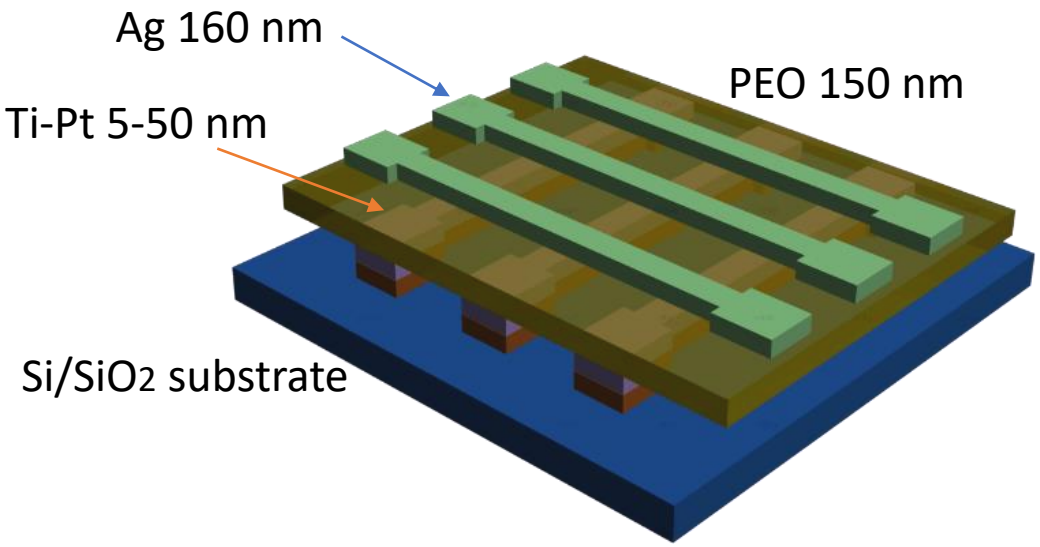
[39] B. Govoreanu *et al.*, "10x10nm 2 Hf / HfO x Crossbar Resistive RAM with Excellent Performance , Reliability and Low-Energy Operation," pp. 729–732, 2011.

[40] J. Jang *et al.*, "Energy Consumption Estimation of Organic Nonvolatile Memory Devices on a Flexible Plastic Substrate," *Adv. Electron. Mater.*, vol. 1, no. 11, p. 1500186, Nov. 2015, doi: 10.1002/aelm.201500186.

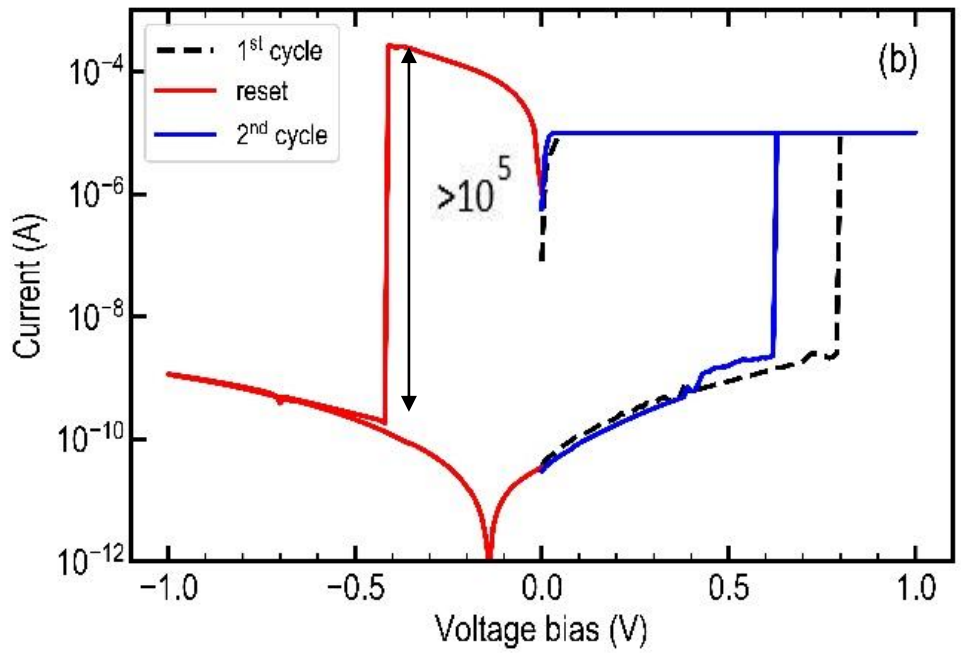
[41] Y. Sun, J. Lu, C. Ai, D. Wen, and X. Bai, "Multilevel resistive switching and nonvolatile memory effects in epoxy methacrylate resin and carbon nanotube

composite fi lms," *Org. Electron.*, vol. 32, pp. 7–14, 2016, doi: 10.1016/j.orgel.2016.02.002.

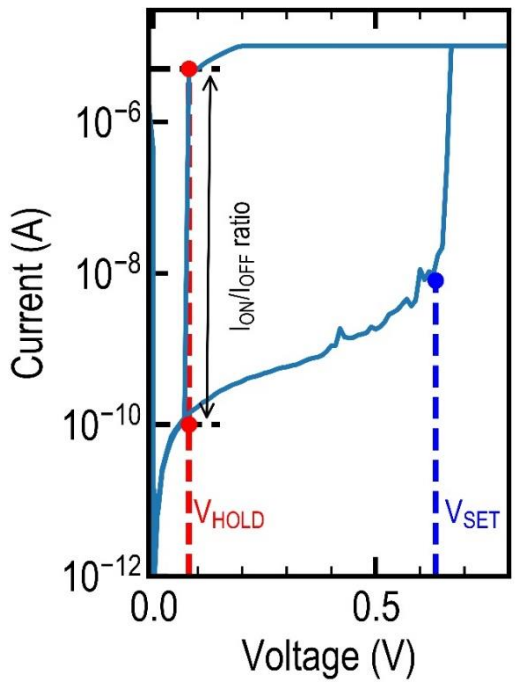
[42] W. S. Machado, M. A. Mamo, N. J. Coville, and I. A. Hümmelgen, "The OFF to ON switching time and ON state consolidation in write-once-read-many-times memory devices based on doped and undoped carbon-sphere / polymer composites Composite Substrate," *Thin Solid Films*, vol. 520, no. 13, pp. 4427–4431, 2012, doi: 10.1016/j.tsf.2012.02.075.



Fabrication



Non volatile switchings: as memories



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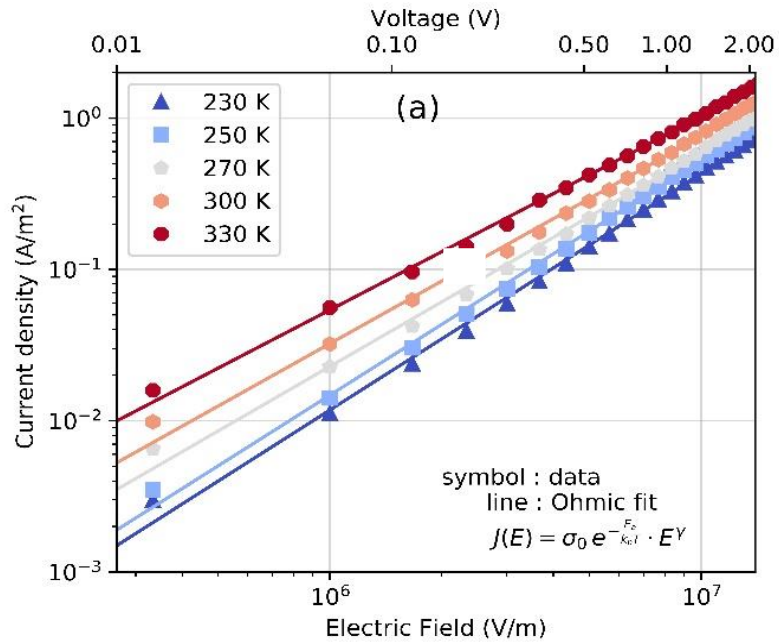

Study of Charge transport