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A 3D slow-wave transmission line approach for the design of Ka-band CMOS compact filters

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Abstract — This paper presents the implementation of a new topology of 3D slow-wave transmission lines in CMOS technology. The proposed structure makes it possible to consider the design of compact circuits based on these 3D transmission lines presenting performances superior to the lumped elements approach (inductors and capacitors) for the Ka band, and in particular for 5G applications. The equivalent electrical model of the 3D structure, based on a physical analysis, is established, with excellent agreement with the measurement results. Then a filter based on parallel stubs is proposed in order to show the potentialities of the proposed 3D structure. The performances obtained are acceptable, with a power balance showing insertion loss potentially equal to 3 dB if the structure is matched, for a relative bandwidth of 22%. Development prospects concern the design of more complex filters but also of matching networks for LNAs or PAs.

Keywords — 3D structure, Slow-wave, filter, CMOS technology

I. INTRODUCTION

The advent of 5G and soon 6G at the end of this decade propelled the development of front-end radios towards millimeter-wave (mm-wave) bands for consumer applications. The Ka band in particular, with frequencies around 28 GHz for 5G, has become a major field of study for the development of high-performance front-ends, whereas until now this band was mainly used for satellite communications. One of the challenges to be solved for Ka-band front-ends concerns the development of filters with low mass, low volume and flat shape. In this context, two solutions are currently available to designers, either using PCB technology, and in particular Substrate-Integrated Waveguides (SIW), which require connecting the integrated parts developed in CMOS technology (PA, LNA, mixer), at frequencies where the parasitics related to the interconnections are not negligible, or use filters integrated into the CMOS chip. The latter has the advantage of integrating the entire front-end, apart from the antenna. On the other hand, the designer must then face two challenges, (i) the cost of CMOS technology, which imposes the smallest possible surface for the filter so that its integration is acceptable, and (ii) the performance of the filters, which suffer the low-quality factor of CMOS passive components.

In this context, it is thus important to be able to study the possibility of producing compact and efficient filters in CMOS

technology. Few realizations exist in the literature in Ka band, unlike the bands around 60 GHz. This stems from the fact that the Ka band is not conducive to the development of integrated filters. In this band, lumped components (capacitors and inductors) have reduced quality factors (around 30), and above all require very fine modeling due to parasitic couplings, in particular for inductors. Conversely, the transmission lines are very simple to model, while presenting comparable quality factors, but suffer from prohibitive dimensions for the design of resonators. We could think to use the slow-wave CPW (S-CPW), invented in the early 2000s [1] and whose model is known [2], whose dimensions are reduced compared to conventional microstrip lines type, but their dimensions remain too important for the design of resonators in Ka band. In order to overcome this problem, we propose in this article to use 3D S-CPW, with a concept of superimposed CPW. This concept makes it possible to drastically reduce the dimension of the resonators, not only by using two levels of transmission lines, but also by creating many couplings that can be used efficiently for the resonators design. Hence, this approach permits to reach acceptable dimensions from the point of view of the cost of integration. The electrical performances are certainly modest compared to an SIW PCB technology, but are comparable to integrated slow-wave CPW [4]. This article must be considered as a first step to demonstrate the potential of 3D S-CPWs in CMOS technology for the realization of filters. The concept thus demonstrated can then be used also for the design of matching networks for LNA or PA amplifiers, for which we have to face the same problem concerning the integrated lumped components, but without the possibility of having recourse to PCB technology, the matching network necessarily having to be integrated as close as possible to the transistors.

The article is organized as follows. First, in section I, the 3D structure is presented, and a physical model of a 3D S-CPW is developed and validated on a resonator measured between a few GHz and 80 GHz. Then, in section II, the 3D concept is applied to the design of an elementary band pass filter. Finally, the experimental results of the designed filter are compared to the simulation results, then to the state of the art, in section III, and a conclusion allows to synthesize the main results presented in this article.

II. 3D STRUCTURE

A. Technology Description

This work was carried out on the 55-nm BiCMOS technology from STMicroelectronics [3].

This technology comes with a thick Back-End-Of-Line (BEOL), which permits to stack two CPW with broadside coupling, to reach the 3D concept. The BEOL is described in Fig. 1. It offers a total of eight metal layers, five thin metal layers at the bottom for digital purposes, and three thick metal layers at the top, which permit to develop RF passive circuits and components.

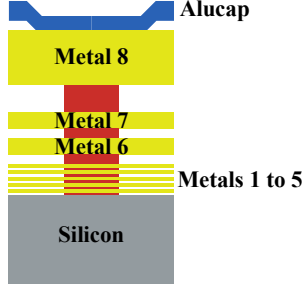


Fig. 1. Back-End-of-Line of the STM BiCMOS 55-nm technology

B. 3D S-CPW Principle

To take advantage of the full BEOL for the design of compact RF passive circuits (filters, matching networks...), a 3D structure is proposed, which is composed of two stacked S-CPWs, as depicted in Fig. 2.

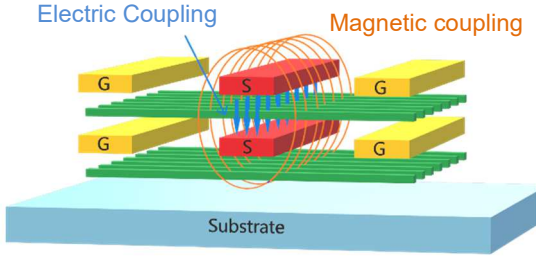


Fig. 2. Layout view of the proposed FS-CPW

Each S-CPW is composed by two ground strips on both sides of the signal strip, with underneath a series of perpendicular metallic ribbons limited in width by the ground strips. The distance between the two S-CPWs is about few microns. This proximity provides to this structure a strong capacitive and inductive coupling between the S-CPW, as shown in Fig. 2, which leads to (i) a reduction of the electrical length of the structure connected as a vertically folded S-CPW (FS-CPW), and (ii) additional degrees of freedom for complex circuits design, such as filters and matching networks.

C. Measurements of the Standalone 3D Structure

A first FS-CPW was designed and measured in order to validate the concept and develop a first electrical model (see next sub-section). The chip photo is given in Fig. 3.

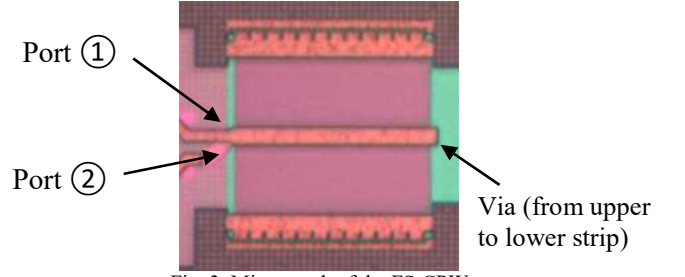


Fig. 3. Micrograph of the FS-CPW

The FS-CPW is folded with a via at the far end, and the I/O RF ports are located on the same side. The S-parameters of the structure are plotted in Fig. 4. The structure behaves as a stub, with a resonance frequency located near 45 GHz. In microstrip, a half wavelength stub operating at 45 GHz would have a physical length of 1.5 mm, whereas the FS-CPW length is only 160 μm . This proves the high compactness potential of the 3D structure.

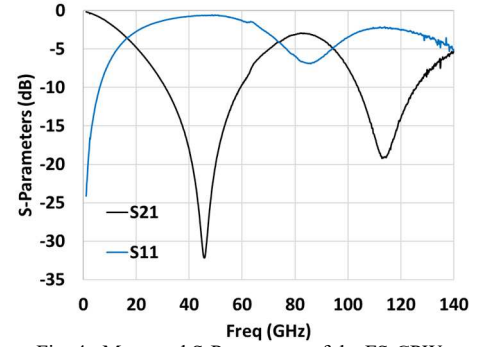


Fig. 4. Measured S-Parameters of the FS-CPW

D. Electrical equivalent Model of the 3D Structure

In order to get an efficient tool for future designs using the proposed 3D structure, a first electrical model was developed, based on a physical approach. The model developed herein is not general since it only concerns the particular FS-CPW measured above, but it paves the way for the future development of a full electrical model parameterized with all the dimensions of the FS-CPW. The proposed electrical model is based on the model of the S-CPW [2], where the S-CPW was divided in elementary cells corresponding to the floating ribbons period. The electrical of an elementary cell of the FS-CPW is shown in Fig. 5. This cell can then be cascaded multiple times to consider a transmission line of given length, as for the Telegraphist's model.

The electrical model in Fig. 5 considers the four layers used by the FS-CPW (Fig. 2). The upper (1 to 1') and lower (2 to 2') strips are modeled by an inductance in series with a resistance, L_{up} , R_{up} , and L_{low} , R_{low} , respectively. Similarly, the upper and lower ribbons are modeled by an inductance in series with a resistance, L_{f_up} , R_{f_up} , and L_{f_low} , R_{f_low} , respectively.

The electric coupling between strips and ribbons is represented by the capacitances $C_{f_up/up}$ (from the upper strip to the upper ribbons), $C_{f_up/low}$ (from the lower strip to the upper ribbons) and $C_{f_low/low}$ (from the lower strip to the lower

ribbons). In the same way, the electric coupling to the ground strips is represented by C_{f_up/g_up} , C_{f_up/g_low} and C_{f_low/g_low} .

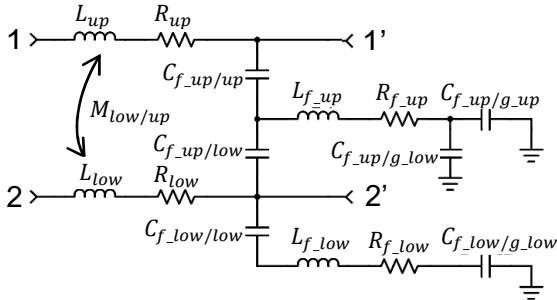


Fig. 5. FS-CPW elementary cell equivalent electrical model

Due to the symmetry, right and left sides of the model (ribbons inductances and resistances, capacitances to the ground) were merged. Finally, the magnetic coupling between the upper and the lower signal strips is modeled by the mutual inductance $M_{low/up}$. The value of these components were extracted with Ansys Maxwell 3D, and finally optimized with ADS. This model was applied to the 3D structure described in section II.C. The results are shown in Fig. 6, with a very good agreement between the measurements and the electrical model.

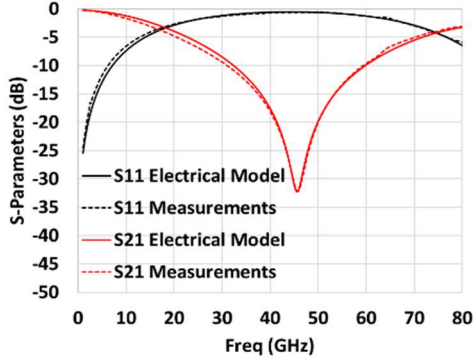


Fig. 6. S-parameters (a) magnitude of electrical model (dotted line) and measurements (full line) of the 3D structure.

As preliminary discussed above, the added third-dimension gives a lot of degrees of freedom, allowing to use the structure as or a resonator either as an impedance transformer. Indeed, the given dimension allows the designer to carry out various impedance transformation ratios. Those are defined by determining firstly the dimensions, and then with the choice of the environment of the structure (connection ports, loads: Open or short-circuit). Using it as a matching network, this impedance transformation can be used as is. As a resonator, and if multiple zeros are needed, multiple structures have to be connected in a more complex circuit, as detailed in section III.

III. FULL RESONATOR DESIGN

To design a full resonator, the FS-CPW was used to set a given impedance, which permits the placement of multiple transmission zeros (TZs) on the 15 – 45 GHz band to define an operating frequency of 29 GHz for the targeted bandpass filter.

With an optimization carried out on ADS, resonators were interconnected with microstrip lines, whose electrical lengths

are still short at the operating frequency, i.e. from 5° to 10° . These interconnections have an impact on the frequency of each TZ, according to the connected part of the resonator. Thus, the optimization gives some extra part of degrees of freedom (each characteristic impedance and electrical length) to precisely place the TZs frequency and to set the input impedance.

The choice of the dimensional parameters for each FS-CPW was optimized using the electrical model presented in section II, with a sweep of the main dimensions (length, gap, width...), and finalized with an EM simulation setup on ANSYS HFSS.

The whole structure after the final optimization of the schematic on ADS is given in Fig. 7. It is composed of three parts, A, B and C.

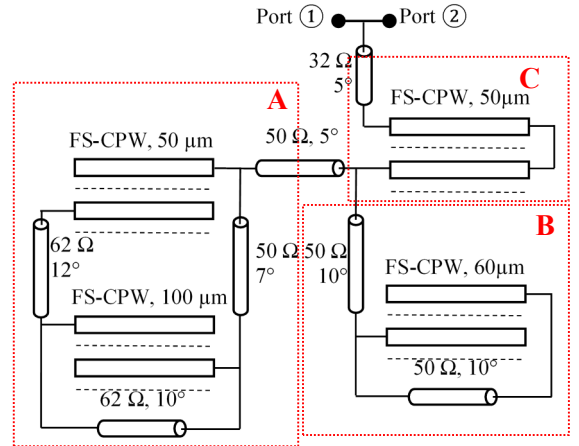


Fig. 7. Schematic of the full resonator.

The parts A and B set three TZs at 21 GHz, 35 GHz and 42 GHz, respectively. The part C permits to optimize the center frequency of the filter, since it modifies the electrical lengths of the two stubs realized by the parts A and B.

IV. RESULTS

The final layout has to follow some classical rules given by the Design Rule Manual of the technology: physical placement of the structures and microstrip lines, and Design Rules Check in terms of metals density at each layer level. The first constraint leads to minor modifications on the electrical length and characteristic impedance that can easily be taken into consideration in the post-layout simulation process. The second point brings some complexity on designing the interconnections, due to the metal density needed for each layer.

All the FS-CPWs were simulated with ANSYS HFSS, whereas the microstrip lines were simulated in ADS where the total circuit was simulated. EM simulations were not considered for the microstrip junctions, which probably explains the disagreement between simulation and measurement results, as shown below.

Finally, to reduce the size of the overall circuit, GSGSG pads were used for the filter feeding, as shown in Fig. 8. The circuit has a final size of about 0.125 mm^2 . S-parameters measurements were performed using Anritsu VectorStar® ME7838A4 Vector Network Analyzer (VNA), with an on-wafer TRL calibration, from 5 GHz to 60 GHz. Simulation and measurement results are given in Fig. 9.

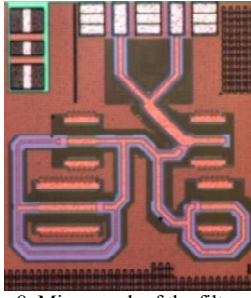


Fig. 8. Micrograph of the filter

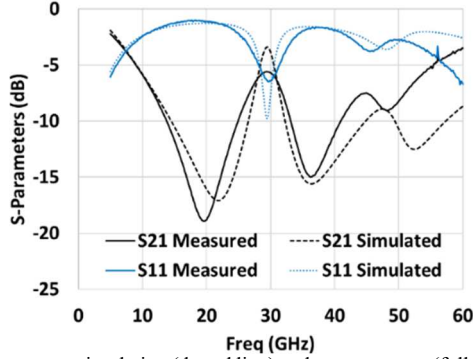


Fig. 9. S-parameters simulation (dotted line) and measurement (full-line) results.

The operating frequency of 29 GHz is in good agreement between simulation and measurement results. The measured bandwidth is about 22%, as compared to 11% as predicted by the simulation. The measurement shows significant insertion loss of 5.6 dB at the center frequency, instead of 3.5 dB predicted by the simulation. The measured return loss is equal to 6 dB, which partly explains the large insertion loss. A power budget ($S_{11}^2 + S_{21}^2$) was calculated for the simulated and the measured S-parameters, as shown in Fig. 10.

The power budget of the resonator confirms that the measured insertion loss is partly due to the mismatch; an insertion loss of about 3 dB could be obtained with a better return loss, giving the real potential of the 3D structure. This could be optimized in a future realization, by considering all the microstrip junctions by running EM simulations, so that a full EM post-layout simulation of the whole circuit can be performed, which was not the case herein.

Finally, a comparison to some state-of-the-art filters designed in CMOS technology around 30 GHz is given in Table 1. Very few integrated filters have been published in this frequency range, which limits the comparison. In addition, the BEOL of the technology used has a very strong influence on the electrical performance. Nevertheless, it is interesting to compare the results obtained in the work presented in this paper with recent results from the literature. The elements of comparison are the fractional relative bandwidth (FBW), the insertion loss (IL), the return loss (RL) and the surface area. The filter presented in this paper has the lowest bandwidth, which partly explains why it exhibits the highest insertion loss, knowing that these can be greatly reduced by improving the return loss, which is not acceptable, as previously discussed. In terms of area, it falls between the two filters used for the comparison.

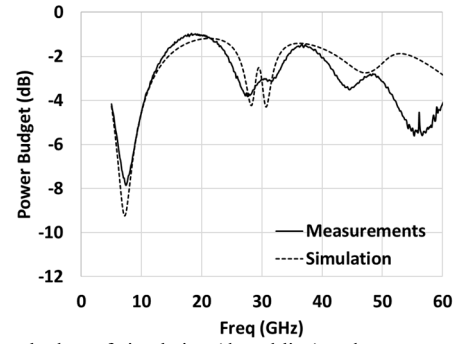


Fig. 10. Power budget of simulation (dotted line) and measurement (full-line) results.

Table 1. Comparison with the state-of-the-art.

Ref	F_0 (GHz)	FBW (%)	Area (mm^2)	IL (dB)	RL (dB)	Type
[5]	33	33	0,038	2,6	13	BCMLR
[6]	26,5	50,9	0,176	3,8	15	Hybrid Coupling
This work	29	22	0,125	5.6	6	3D S-CPW

V. CONCLUSION

In this paper, the first results of a new resonator topology based on 3D slow-wave transmission lines was proposed. It was designed on the BiCMOS 55-nm technology from STMicroelectronics. An equivalent electrical model topology was proposed, then an experimental implementation was able to show the potential of the proposed 3D structure. These first results will pave the way towards the development of more efficient filters, in particular with regard to return loss and out-of-band rejection, but also very compact matching networks for LNAs and PAs.

REFERENCES

- [1] T. S. D. Cheung et al., "On-chip interconnect for mm-wave applications using an all-copper technology and wavelength reduction," 2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC., 2003, pp. 396-501 vol.1, doi: 10.1109/ISSCC.2003.1234353.
- [2] A. Bautista, A. -L. Franc and P. Ferrari, "Accurate Parametric Electrical Model for Slow-Wave CPW and Application to Circuits Design," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 12, pp. 4225-4235, Dec. 2015, doi: 10.1109/TMTT.2015.2495242.
- [3] P. Chevalier et al., "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," 2014 IEEE International Electron Devices Meeting, 2014, pp. 3.9.1-3.9.3, doi: 10.1109/IEDM.2014.7046978.
- [4] A.-L. Franc, et al., "High-performance Shielded Coplanar Waveguides for the Design of CMOS 60-GHz Band-pass Filters", *IEEE T-ED*, Vol. 59, No.5, pp. 1219 - 1226, May 2012.
- [5] Y. Zhong, Y. Yang, X. Zhu, E. Dutkiewicz, K. M. Shum and Q. Xue, "An On-Chip Bandpass Filter Using a Broadside-Coupled Meander Line Resonator With a Defected-Ground Structure," in IEEE Electron Device Letters, vol. 38, no. 5, pp. 626-629, May 2017, doi: 10.1109/LED.2017.2690283.
- [6] M. Li, Y. Yang, K. D. Xu, X. Zhu and S. W. Wong, "Microwave On-Chip Bandpass Filter Based on Hybrid Coupling Technique," in IEEE Transactions on Electron Devices, vol. 65, no. 12, pp. 5453-5459, Dec. 2018, doi: 10.1109/TED.2018.2876324.