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Alina Maksimova, Alexander Uvarov, Artem Baranov, Alexander Gudovskikh, Dmitri Kudryashov, et al.. Investigation of Plasma Deposited Boron Phosphide and Its Contact to Silicon. ACS Applied Energy Materials, 2022, 5 (5), pp.5367-5373. <10.1021/acsaem.1c02704>. <hal-03832802>

**HAL Id: hal-03832802**

**<https://hal.science/hal-03832802v1>**

Submitted on 27 Oct 2022

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# Investigation of Plasma Deposited Boron Phosphide and its Contact to Silicon

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## KEYWORDS

Semiconductors, Solar cells, silicon, selective contacts, PECVD, boron phosphide

## ABSTRACT

Boron phosphide layers were fabricated using plasma enhanced chemical vapor deposition and modified atomic layer deposition methods and electrical contact properties to silicon were

investigated. Presence of boron and phosphorus was proved by energy dispersive X-ray spectroscopy and secondary ion mass spectrometry. Influence of the deposition parameters on characteristics of the layers and on the silicon substrate was studied. The band gap of boron phosphide was evaluated by optical measurements at 2.1-2.2 eV. In Au/BP/Si structures, capacitance measurements revealed the presence of electron accumulation at the BP/Si interface. This regime can be explained by lowly doped or undoped BP and Fermi level pinning at the BP/Si interface due to the presence of interface defect states. We also used the deep level transient spectroscopy (DLTS) method from which we detected defects in the near-surface silicon region that may be formed under the influence of the high-power plasma during the deposition of the boron phosphide layer. However, insertion of a thin a-Si:H layer between BP and Si acts as a passivating layer, thus allowing one to decrease the interface state density and increase the minority carrier lifetime and open-circuit voltage, which is promising for photovoltaic applications.

## **Introduction**

One of the main objectives of solar energy research work nowadays is the development of a new configuration of solar cells (SC) in order to increase efficiency and reduce fabrication cost. Silicon solar cells have several significant advantages required for photovoltaic systems, such as abundance, scalability, low toxicity and low cost. These explain the prevalence of silicon in the photovoltaic market and the strong increase of photovoltaic installations all around the world, that are expected to continue and even accelerate in the future [1].

For any solar cell, it is necessary to separate photo generated electrons and holes and collect them at opposite contacts. In most crystalline silicon solar cells, this is achieved by the diffusing dopants of opposite polarity onto opposite surfaces of a c-Si substrate, which creates regions of

very high conductivity for only one of the two types of charge carriers [2]. Despite the proven effectiveness, this approach can limit the performance due to recombination losses and technological imperfections. These problems have motivated research on alternative approaches to make contacts to silicon [3].

One of these approaches is the development of selective contacts (SC) to silicon. The fabrication of such SC does not require using of high-temperature steps like in the formation of a dopant diffusion p – n junction. For instance, thin stacks of undoped and doped a-Si:H layers deposited at temperatures below 250°C have been used for selective contacts to c-Si, and they made it possible to achieve an efficiency of 26.7% with an integrated back contact (IBC) design [4].

The main principle of this approach is the deposition of a thin layer on a Si-substrate, which selectively separates charge carriers. The transport of charge carriers of only one polarity (either holes or electrons) through the heterointerface occurs freely and the transport of the other one is blocked and avoids surface recombination at the interface between the material and the metal electrode. This approach can indeed lead to increasing the efficiency of c-Si cells through reduction of absorption, simplification of technological processing steps and lowering process temperature (less than 250°C) for the manufacturing of silicon SCs.

The most recent papers report a comparative study involving three transition metal oxides (TMOs): MoO<sub>3</sub>, WO<sub>3</sub>, and V<sub>2</sub>O<sub>5</sub>, which can form a hole-selective heterojunction to n-type c-Si solar cells [5]. These oxides have been widely used in organic semiconductor devices as hole-transport layers due to the proven selectivity of holes and a large optical band gap [6].

Another recently proposed approach uses a structure composed of an ultra-thin silicon oxide layer (SiO<sub>2</sub>) and a heavily doped polysilicon layer. The first one must provide passivation of c-

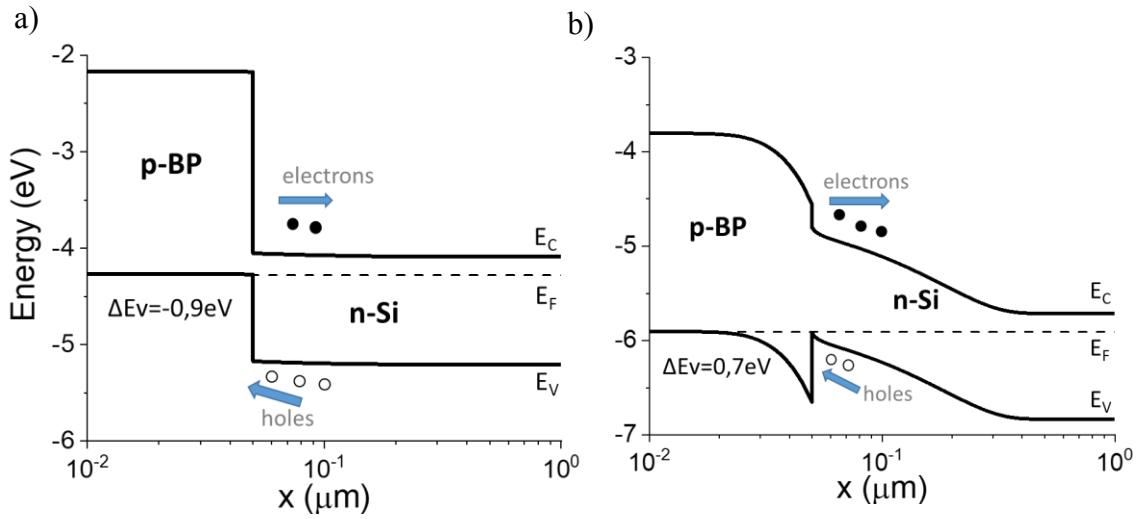
Si, while still allowing charge carriers to pass through it (either by tunneling or through shunt nanocontacts), the second ensures carrier selectivity, and it can be obtained by the deposition of amorphous silicon followed by the high-temperature crystallization annealing. Conversion efficiency of such SC was over 25% for small elements, but the industrialization of this process is not yet on the agenda, and it faces a number of additional steps that must be implemented [7].

However, such contacts have low temperature stability and parasitic absorption in a short-wavelength region [8]. Therefore, an intensive search for new materials that could avoid the disadvantages of a-Si:H and transition metal oxides is underway.

In this work, it is proposed to consider a new material for the formation of contacts to silicon, namely boron phosphide (BP), which has high thermal and mechanical stability. BP is quite chemically inert, it does not react with mineral acids or any common semiconductor etchant, and only the molten NaOH weakly reacts with it [9]. Boron phosphide is resistant to the oxidation at high temperatures [10], thus it has a potential to create devices operating in extreme conditions, as a promising material due to its stable mechanical properties. Therefore, almost all the work was focused so far on the study of its mechanical properties. Electrical properties have not received much attention, and they thus need to be investigated.

It was theoretically shown in ref. [11] that BP is one of the most promising binary compounds for creating a transparent conducting p-type coating, since it has an indirect bandgap and a large difference between the energies of the direct (4 eV) and indirect transition (2 eV), which implies low optical losses. Consequently, the use of BP/Si heterojunctions instead of poly-Si/SiO<sub>x</sub>/Si or (p)a-Si:H/(i)a-Si:H/Si can lead to an increase in short-circuit current. Therefore, BP could in principle be used to create a selective contact to silicon of the both types of conductivity.

According to ref. [12], the BP/Si interface has a negative ( $-0.3 \pm 0.1$  eV) valence band offset ( $\Delta E_V$ ) therefore it can provide the necessary selectivity, which makes BP an excellent candidate as a selective hole contact, without requiring an additional ITO layer [13]. However, according to the literature data, values of the valence band offset for the BP/Si interface scatter over a wide range from  $-0.9$  eV to  $+0.7$  eV [14]. It can be found either negative or positive, in the first case ensuring the selectivity of charge carriers (Figure 1a), in the second, it can form a potential barrier that blocks the flow of charge carriers (Figure 1b). In addition, the magnitude of the valence band offset at the interface can significantly affect the sensitivity to the surface states [15]. Thus, in order to predict the efficiency of solar cells based on p-BP/n-Si, it is necessary to determine the study of electrical properties of the BP/Si heterojunction first.



**Figure 1.** Schematic band diagram at the heterojunction between p-type BP and n-type silicon, p-BP/n-Si, a) with a negative valence band offset,  $\Delta E_V = -0.9$  eV; b) with a positive valence band offset,  $\Delta E_V = 0.7$  eV.

The growth of BP can be carried out by different methods on different substrates: gas-phase epitaxy on Si [16], plasma-chemical deposition on Si and ZnS [17], magnetron sputtering on Si

[18]. Boron phosphide layers can also be grown by plasma enhanced chemical vapor deposition (PECVD) [11]. It is a reliable, industrial method, which allows electronic-quality films to be grown at low temperatures over large areas. However, for BP layers, according to ref. [19], synthesis is difficult due to the difference in the reactivity of B and P. To solve this problem, it was proposed to use the plasma enhanced atomic layer deposition-like (pseudo PE-ALD) approach, in which the B and P atoms precursors are decomposed with the help of the RF plasma.

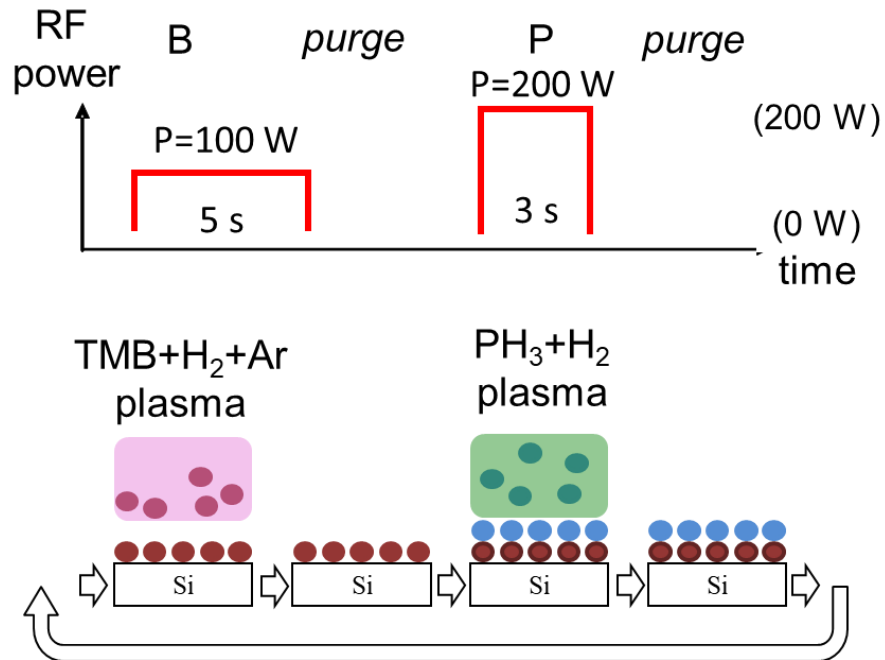
## Experiment

The growth of undoped BP films was carried out in a standard Oxford PlasmaLab 100 PECVD (13.56 MHz) plasma chemical deposition unit in two modes, continuous (PECVD) and cyclic (pseudo PE-ALD). Gas mixtures of hydrogen and trimethylboron (TMB) or phosphine ( $\text{PH}_3$ ) were used as precursors, with gas ratios (TMB)/ $\text{H}_2$  and  $\text{PH}_3$ / $\text{H}_2$  of 2% and 5%, respectively. BP layers were deposited on n-type double-sided polished c-Si substrates grown by the Czochralski method with a doping level of  $N_d=1 \cdot 10^{15} \text{ cm}^{-3}$ . Immediately before loading into the working chamber, substrates were treated in a 10% HF/ $\text{H}_2\text{O}$  solution to remove the native oxide.

In the continuous PECVD mode, BP layers are deposited on quartz and silicon substrates at different temperatures of 250°C and 380°C, with a plasma power of 30 W and pressure of 350mTorr.

In the pseudo PE-ALD mode, the first step is the decomposition of the TMB/ $\text{H}_2$  mixture using addition of Ar, which is necessary to ensure the guaranteed ignition of the plasma with a power of 100 W and a duration of 5 seconds (see figure 2). Without the addition of Ar the growth rate is extremely slow and layers have a high nonuniformity. Then, after the purge and blowing,

unreacted TMB molecules are removed from the chamber that is subsequently filled with  $\text{PH}_3$ .  $\text{PH}_3$  decomposition occurs at a plasma power of 200 W during 3 seconds. Phosphorus atoms form bonds with boron atoms, and a BP monolayer can thus be formed. After that, the chamber is evacuated again, purged, and the whole process is repeated again. During the process, which consists of 200 cycles, layers of different thicknesses are deposited. Parameters of the process are shown in Table 1. The growth rate in both modes is higher at a lower temperature. For all samples, layer thicknesses were determined using a Horiba PZ2000 laser ellipsometer with 632,8 nm He-Ne source, results are presented in table 2.



**Figure 2.** Pseudo PE-ALD process sequence.

**Table 1.** Parameters of the pseudo PE-ALD method deposition process steps.

ALD 250/380°C 200 cycles		Gas mixture	Flow rate, sccm	p, mTorr	P, W	
Step 1	5s	TMB/Ar/H <sub>2</sub>	100/50/100	350	100	TMB deposition
Step 2	10s	Ar	100	0	0	Purge

Step 3	3s	PH <sub>3</sub> /Ar/H <sub>2</sub>	30/50/200	350	0	Pressure stabilization
Step 4	3s	PH <sub>3</sub> /H <sub>2</sub>	10/200	350	200	Phosphorus deposition
Step 5	4s	Ar	100	0	0	Purge
Step 6	4s	Ar	200	350	0	Pressure stabilization

To estimate the composition of the resulting structure, the method of energy dispersive X-ray spectroscopy (EDX) was used. To determine the profile of the composition, measurements were performed by the method of secondary ion mass spectrometry (SIMS) on a Perkin-Elmer PHI 4300 setup. Sputtering was carried out with Ar ions with an energy of 4 keV in the mode of surface scanning with an ion beam.

To study structural properties and surface morphology an image of the BP layer deposited on a silicon substrate was obtained using scanning electron microscopy (SEM) from a Zeiss Supra 25 set-up.

Optical transmission and reflection spectra were obtained on samples of BP films deposited on quartz substrates with Avantes ULS2048 spectrometer and Xe light source. Optical band gap parameters for BP thin layers were evaluated by a Tauc plot for indirect band gap semiconductors [20].

Electrical properties were investigated on Au/BP/n-Si/n-a-Si:H/Ag structures, with top Au electrode deposited by thermal evaporation through a circular mask (with 1 and 2 mm diameter ?). An n-type amorphous hydrogenated silicon (a-Si:H) layer was deposited on the back side of the c-Si substrate by PECVD at 250 °C, and Ag was thermally evaporated on it to form a back ohmic contact. Current-voltage characteristics of the samples were measured at room temperature using ???. Capacitance versus voltage measurements were performed using Agilent E4980A-001 precision RLC meter.

To investigate electrically active defects, deep level transient spectroscopy (DLTS) was used. DLTS measurements were carried out using an automated set-up based on a Boonton-7200B capacitive bridge and a Janis VPF 100 nitrogen cryostat, which provides measurements in the temperature range of 80 – 360 K. DLTS is based on measuring the relaxation of the space-charge region (SCR) capacitance at different temperatures. The behavior of the relaxation of the capacitance at a fixed temperature is determined by the concentration of defects, their activation energy, and their capture cross section. By applying different bias voltages to the structure, we can change the SCR width and, accordingly, change the spatial region for detecting possible defects. The measurement time sufficient to fill traps was found to be 50 ms. The offset region from 1 to -4 V corresponds to a depth of more than 700 nm from the surface of the substrate. After the voltage returns to -4 V, the transient capacitance is measured. A filling forward voltage pulse applied to the structure leads to band flattening and injection of electrons into the subsurface region. During a filling pulse, carriers can be captured by defects located in this region, and then they are emitted back after returning to zero bias voltage.

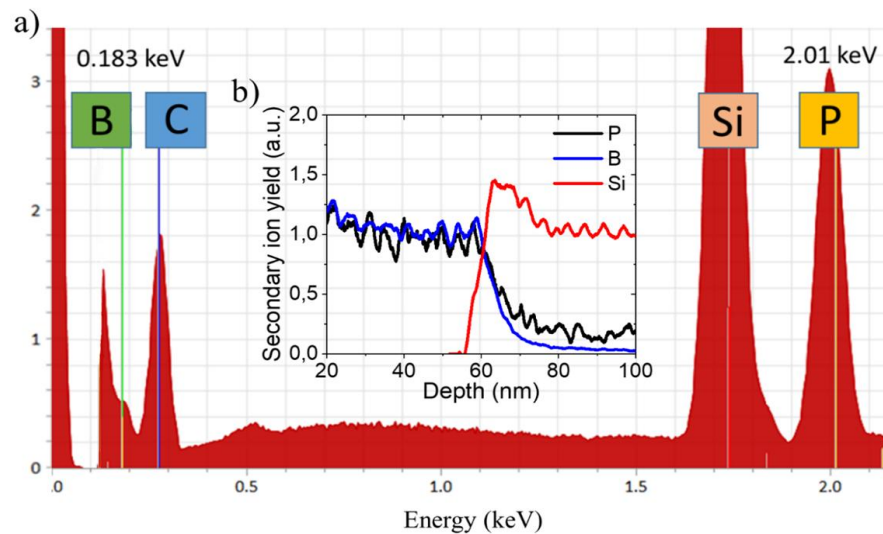
Finally, in order to study the impact of the plasma during the deposition of the BP layers on the passivation of the silicon surface, lifetime testing was performed. Minority carrier lifetime was measured by the quasi-steady-state photo conductance (QSSPC) method using Sinton instruments WCT-120. To this purpose special symmetrical samples were fabricated on double-side polished FZ (100) n-Si 5-10 ohm·cm with bulk lifetime larger than 10 ms. The BP layers were deposited on both sides of the Si wafer by PECVD at 250 °C. Additionally, for one sample, a thin (3 nm) intermediate undoped a-Si:H layer was deposited on Si before BP deposition.

## **Results and discussions**

As can be seen from Figure 3a, the EDX spectrum contains peaks of significant intensity at 0.183 and 2.01 keV, which corresponds to  $K_{\alpha}$  lines of characteristic emission for boron and phosphorus, respectively. This indicates the successful deposition of boron phosphide on a silicon substrate. Quantitative analyses performed using reference samples give the concentration values in the range of 45-65% for boron and 35-55% for phosphorous. Due to the small thicknesses of the layers a precise determination is difficult.

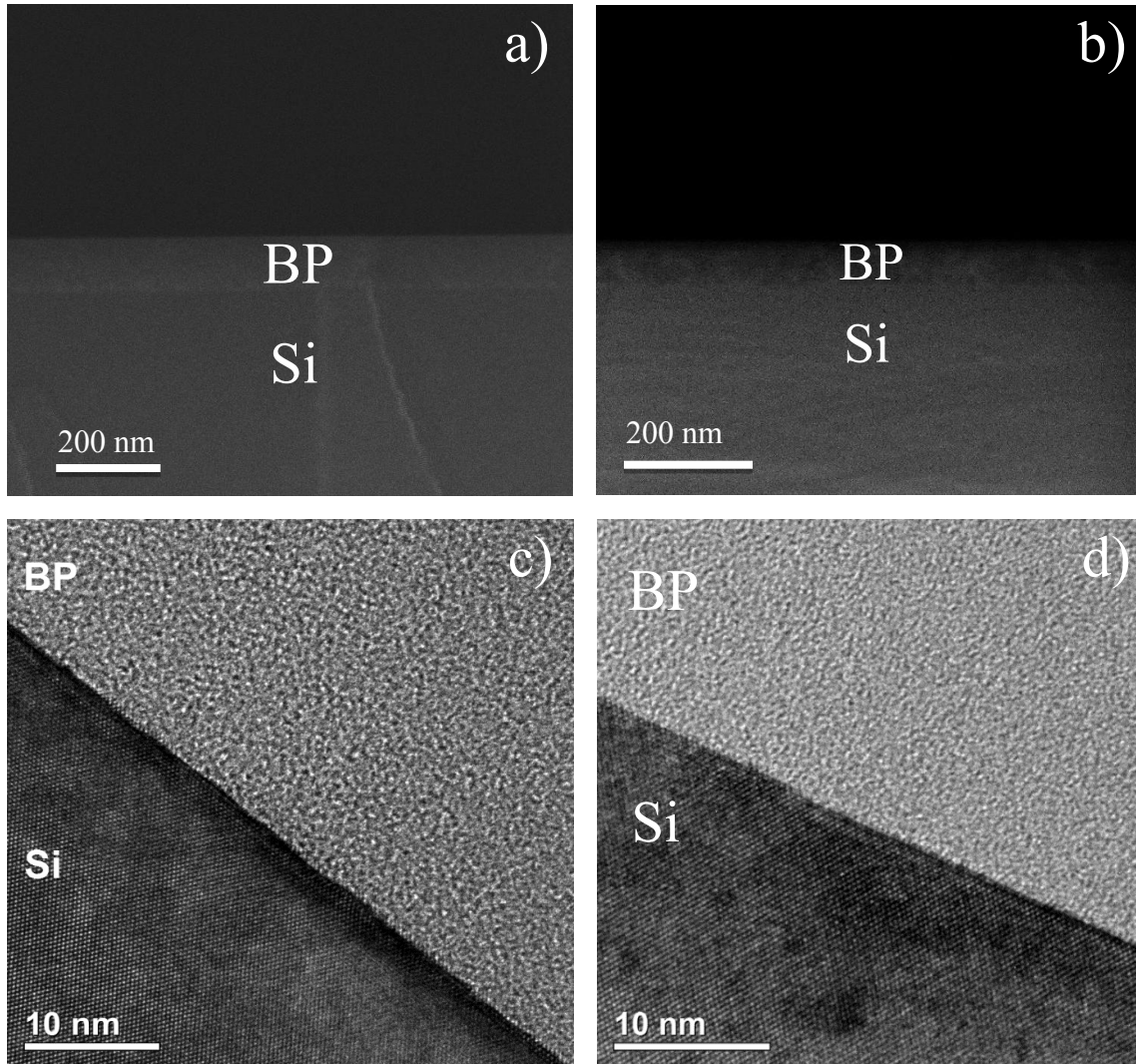
Figure 3b shows SIMS profiles of boron, phosphorus, and silicon in the region of the layer-substrate interface. Two regions can be clearly distinguished: 1) boron phosphide layer of 50-60 nm thick; 2) silicon substrate.

The near-surface layer is characterized by a high yield of boron ions, which is most likely due to contamination or disruption of the structure surface. Boron and phosphorus are uniformly distributed in the boron phosphide layer. In a silicon substrate, the boron signal is reduced to a minimum level. The disordered surface layer of the substrate causes an increased signal from silicon, since atomic bonds in the disordered layer are weaker than in the bulk crystal.



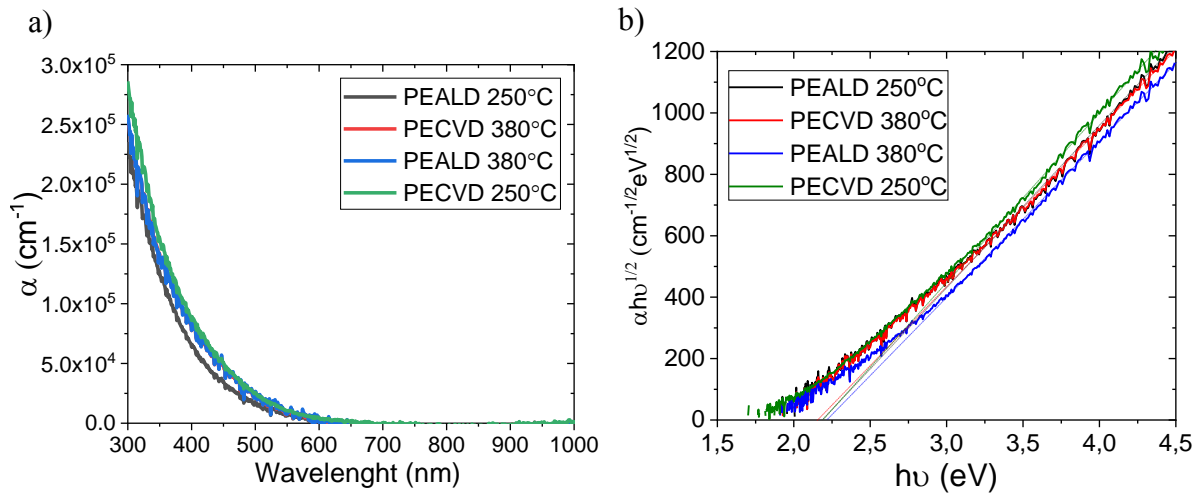
**Figure 3.** a) Energy dispersive X-ray spectrum; b) distribution profiles of elements evaluated by SIMS.

SEM images demonstrate that layers obtained at different modes have a smooth surface and a homogeneous structure (Figure 4). Analysis of the structural properties by Electron Backscatter Diffraction method (EBSD), X-ray Diffraction (XRD) and Raman spectra indicates that the obtained BP layers are amorphous. Raman spectra did not show any hydrogen incorporation, there was no B-H-B, P-H or B-H peaks on the Raman spectra [12].



**Figure 4.** SEM images of BP/Si interface a) PECVD 250 °C; b) PEALD 250 °C; c) HRTEM image of PEALD 250 °C; d) HRTEM image of PECVD 380 °C.

Figure 5a shows absorbance spectra, boron phosphide is quite transparent in the long wavelength region (from 500-1000 nm), while in the short-wavelength region absorbance increases for all the samples. Figure 5b shows the Tauc plot for indirect bandgap [ref 20], in which the gap can be extracted. The gap values vary from 2.155 to 2.218 eV (table 2), which is in agreement with literature data. According to ref. [12], the band gap for a-BP:H is in the range of 2.0–2.1 eV and depends on both the hydrogen and phosphorus proportion. Optical measurements show weak dependence of optical properties of boron phosphide on deposition conditions. Therefore, low temperature processing is preferred for the boron phosphide contact fabrication.



**Figure 5.** Optical properties of BP films a) absorbance spectra; b) Tauc plot for indirect bandgap.

**Table 2.** Properties of the BP films deposited by plasma.

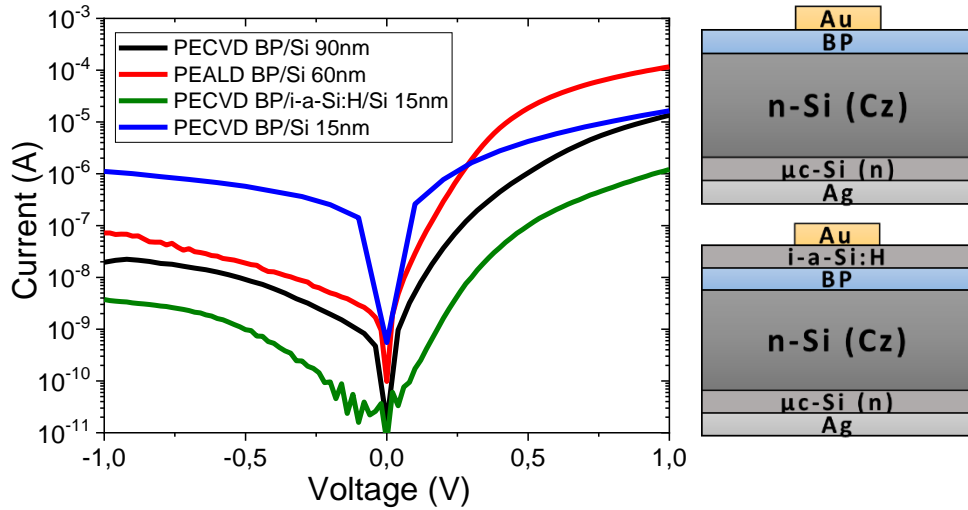
PECVD	no Ar	no Ar	PEALD	Ar	Ar
T, °C	250	380	T, °C	250	380
t, min	20	20	Cycles	200	200

P, W	30	30	P, W	200	200
Growth rate, nm/min	4,5	2,4	Growth rate, nm/cycle	0,3	0,2
Thickness, nm	90	48	Thickness, nm	60	40
E <sub>g</sub> , eV	2,192	2,155	E <sub>g</sub> , eV	2,218	2,186

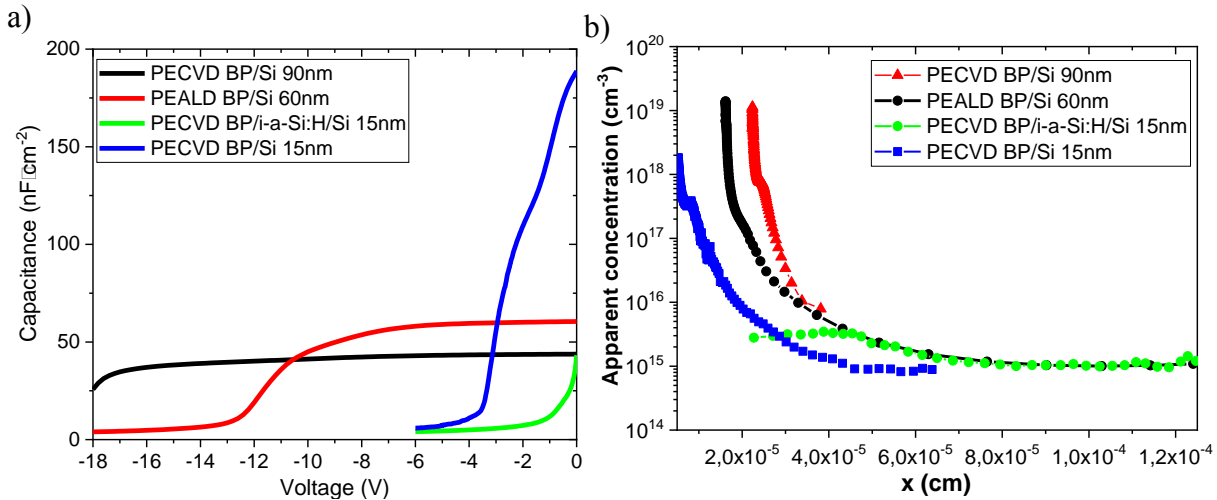
During the growth of layers in the near-surface region of silicon, radiation defects can form due to the plasma exposition. Thus, it is necessary to investigate the electrical properties of the interface, which was performed on the Au/BP/n-Si/n-a-Si:H/Ag structures using I-V, C-V and DLTS methods as described in the experiment section. The obtained I-V curves (Figure 6) have a rectifying behavior, which may indicate the presence of a space charge region in Si. The capacitance-voltage characteristics are presented in Figure 7a. The structures with the largest BP thickness (90 and 60 nm) exhibit a weak dependence on reverse voltage in the range from 0 to 9 V. Further increase in reverse voltage leads to a drastic drop of the capacitance. It should be noted that this threshold voltage increases with the thickness of BP. In case of thin (15 nm) BP layer, this drop appears at lower reverse voltage. The absolute value of the capacitance at zero voltage increases with the BP thickness. The observed behavior of C-V curves is representative of a MIS structure, BP acting as an insulator and the silicon substrate being the semiconductor, with electron accumulation in Si near the BP/Si interface. Indeed, the apparent electron concentration from the experimental C-V curves (Figure 7b), which was calculated according to the procedure described elsewhere [21], demonstrates a high electron concentration near the BP/Si interface. The electron concentration decreases to the value equal to the doping density of the Si substrate ( $10^{15} \text{ cm}^{-3}$ ) with increasing the distance from the interface. On the other hand, the BP layer is fully depleted because the absolute value of the capacitance at zero bias exactly corresponds to the geometrical capacitance, defined as  $C = \varepsilon/d$  (per unit area) where  $\varepsilon$  is the

dielectric permittivity, and  $d$  the thickness of BP layer. It is in contradiction with the observed accumulation in Si, because if a 90 nm thick BP layer is fully depleted, in case of 15 nm thick BP the depletion region due to the Au/BP Schottky barrier should extend into Si and create a depletion region instead of accumulation. The observed behavior of C-V curves could be explained by the pinning of the Fermi level at the BP/Si interface due to a high interface defect density. The calculated band diagram for the BP/Si structure with a defect layer at the interface is presented in Figure 8a (use of AFORS-HET software). The undoped BP layer is completely depleted. However, inserting a thin (3 nm) layer between BP and Si with a large defect density that provides the pinning of the Fermi level near to the conduction band at the interface, leads to the formation of electron accumulation in Si. In this case the calculated C-V curves for different BP thicknesses corresponds quite well to the experimental data (Figure 8b). The absolute value of the capacitance at zero voltage corresponds to the BP layer thickness, while the voltage corresponding to the capacitance drop increases with the thickness. Additionally, the C-V curve was calculated for the case when no defect layer at the BP/Si interface is introduced (green line in figure 8b)). In this case the Fermi level is not pinned at the interface and the depletion region penetrates the Si substrate. The absolute value of the capacitance corresponds to the depletion region width, while the voltage dependence is determined by the doping level of the Si substrate. Similar behavior of C-V curves was experimentally obtained for the structure with a thin (3nm) intermediate a-Si:H passivation layer deposited on Si prior to the 15 nm thick BP layer growth (green line in figure 7a). The absolute value of the capacitance is much lower than the geometrical capacitance corresponding to the BP thickness, indicating Si depletion. Moreover, the dependence of the capacitance on reverse bias above 0.5 V corresponds well to the doping level of the Si substrate. The observed difference in behavior of C-V curves for the structures

with and without a-Si:H passivation layer is in good agreement with simulation results. Lower defect density at the interface is expected in this case because a-Si:H is known to have good passivation properties of the Si surface.



**Figure 6.** Dark current-voltage characteristics and schematic representation of structures with a top Au electrode.



**Figure 7.** a) Capacitance-voltage (C-V) characteristics and b) carrier concentration at 100 kHz extracted from the C-V data.

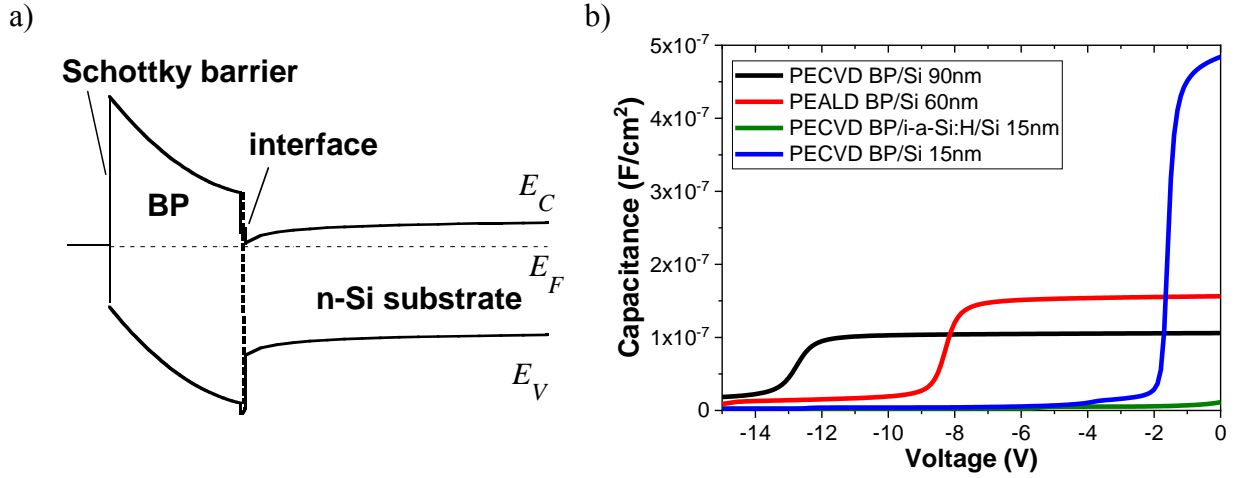
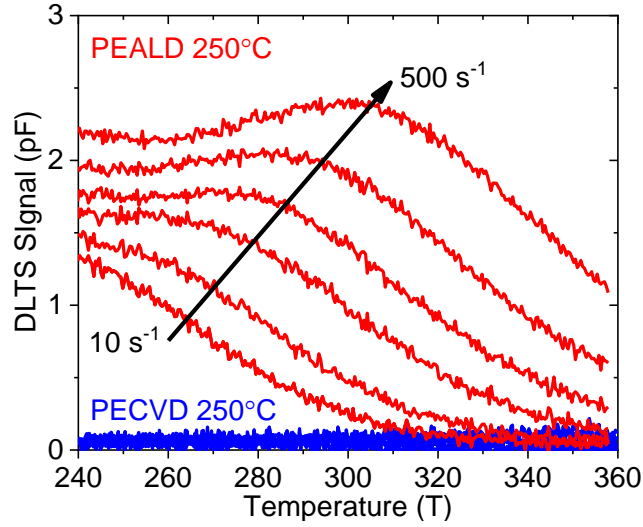


Figure 8. a) Calculated band diagram of Au/BP/Si with pinning of the Fermi level at the BP/Si interface. b) Calculated C-V curves for different thicknesses of the BP layer with (15, 60, 90 nm) and without (15 nm) pinning at the interface.

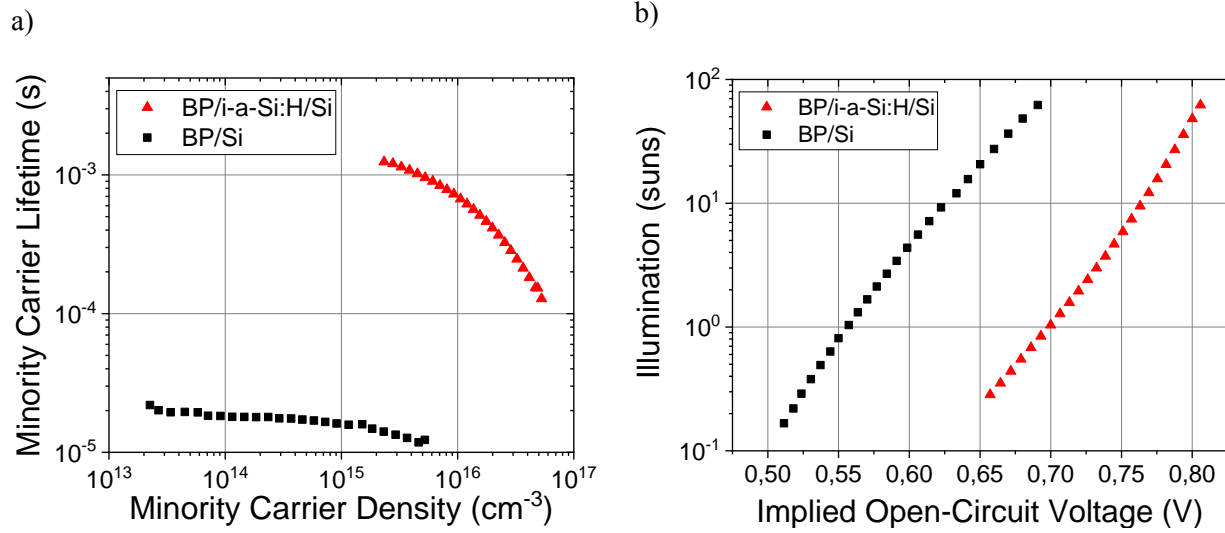
Thus, a high defect density at the BP/Si interface, which leads to the pinning of the Fermi level, is suggested for the fabricated structures.

Then, DLTS measurements were performed at negative bias for two types of the samples grown at 250°C by different way (Figure 9). The sample grown by PECVD without argon plasma does not exhibit any defect response. In contrast, the DLTS spectra for the sample grown by the pseudo PE-ALD method exhibits a response in the range 280-320 K. From the peak position obtained for different emission rates the defect parameters were estimated. The activation energy  $E_a = 0.33$  eV, the capture cross section  $\sigma_n = (1-10) \cdot 10^{-19} \text{ cm}^2$  and defect concentration  $N_T \approx 10^{13} \text{ cm}^{-3}$  were obtained. This defect was described for n-type silicon as a  $(X \cdot V)_D$  vacancy [22]. Such results may indicate the negative impact of both argon plasma and the high power of TMB and  $PH_3$  plasma used in the cyclic process. Thus, the PECVD process, which creates less defects seems to be preferable for photovoltaic applications.



**Figure 9.** DLTS spectra for the emission rate of 10, 20, 50, 100, 200, 500 s<sup>-1</sup> at a bias voltage from 1 to -4 V

Finally, the passivation quality of BP layers was tested using QSSPC measurements. The dependence of minority charge carrier's lifetime on excess carrier concentration for BP/Si structures fabricated by PECVD with and without intermediate a-Si:H passivation layer are presented in Figure 10a. The QSSPC measurements demonstrate lifetime values for the BP/i-a-Si:H/Si structure of approximately 1 ms while for BP on Si without the a-Si:H passivation layer the lifetime values are only in the range of 10  $\mu$ s. This result is in good agreement with our conclusions from C-V measurements, which predict high defect density at the BP/Si interface, when BP is directly deposited onto the Si surface. In contrast, introduction of a thin a-Si:H layer allows one to significantly improve the passivation properties. A value of implied open-circuit voltage equal to 0.7 V could be reached at one sun in this case (Figure 10b) being a promising result for photovoltaic applications.



**Figure 10.** a) Minority Carrier Lifetime and b) Implied  $V_{OC}$  of BP/i-a-Si:H/Si and BP/Si structures.

## Conclusion

The possibility of growing thin layers of boron phosphide using the method of plasma-chemical deposition was shown, both in PECVD and pseudo PE-ALD modes. Deposition was carried out on Si and fused silica substrates at the temperatures of 250 °C and 380 °C. Energy dispersive X-ray spectroscopy showed the presence of boron and phosphorus with 45-65% and 35-55% proportion values, respectively. According to SIMS boron and phosphorus are uniformly distributed in the BP layer. SEM images showed that BP layers have a smooth surface and a homogeneous structure. The extracted band gap value is equal to 2.1-2.2 eV and it is in agreement with values from the literature for boron phosphide. Capacitance measurements reveal the presence of a high defect states density at the BP/Si interface. DLTS measurements have shown that high-power plasma affects electrical properties of the structure. Insertion of a thin a-Si:H layer between BP and Si, acting as a passivating layer, allows to decrease this interface state

density. This also leads to an increase of the minority carrier lifetime and implied open-circuit voltage, which is promising for photovoltaic applications.

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## Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. ‡These authors contributed equally. (match statement to author names with a symbol)

## Funding Sources

The reported study was supported by Ministry of Science and Higher Education of the Russian Federation (research project FSRM-2020-0004).

## ABBREVIATIONS

SC Solar cell, PECVD plasma enhanced chemical vapor deposition, ALD atomic layer deposition, DLTS deep level transient spectroscopy, SCR space charge region

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