

Process challenges and perspectives of vertical GaN power transistors on foreign substrates

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Despite considerable progress in their process technology during the last years, vertical GaN power transistors are currently not finding market entry due to the small size and high cost of native GaN substrates. This issue can in principle be circumvented by using heteroepitaxial GaN on more affordable substrates. Recently, first demonstrations of vertical diodes [1] and transistors [2] for GaN-on-silicon have been published where vertical current flow was enabled by backside removal of the silicon substrate and the isolating buffer layers.

The approach of such membrane power transistors, which essentially reduces the transistor to the active layers and removes all other parasitic substrate resistances, is naturally appealing since it may eventually integrate into the existing silicon ecosystem. However, some of the technologies needed for realizing vertical membrane transistors on industrial level are largely at their infancy. YESvGaN, a KDT-funded European project of 23 partners [3], aims at advancing the required technologies from the heteroepitaxial growth of thick drift layers on affordable substrates such as silicon and sapphire, over transistor chip technology, the backside processes for accessing the drain of the transistor up to its assembly into converter applications.

This contribution presents the envisioned route towards membrane power transistors, the challenges for integrating the respective process steps and a collection of the latest project results from the various partners. For example, YESvGaN reports the growth of drift layers on silicon with above 350 V hard breakdown in quasi-vertical configuration and doping-dependent on-resistance characterization of drift zones on sapphire. It was furthermore possible to demonstrate GaN membranes on 150 mm silicon wafers with 5 mm membrane diameter. These have been shown for residual wafer thicknesses down to 100 μm using a temporarily bonded carrier during backside processing. Last, backside contacts with a specific contact resistance below 100 $\mu\Omega\text{cm}^2$ were achieved by laser-annealing in order to prevent the bonding adhesive from degrading.

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References

- [1] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng and T. Palacios, *IEEE Electron Device Lett.*, **39**(5), 715 (2018)
- [2] R.A. Khadar, C. Liu, R. Soleimanzadeh, E. Matioli, *IEEE Electron Device Lett.*, **40**(3), 443 (2019)
- [3] www.yesvgan.eu

Supplementary information

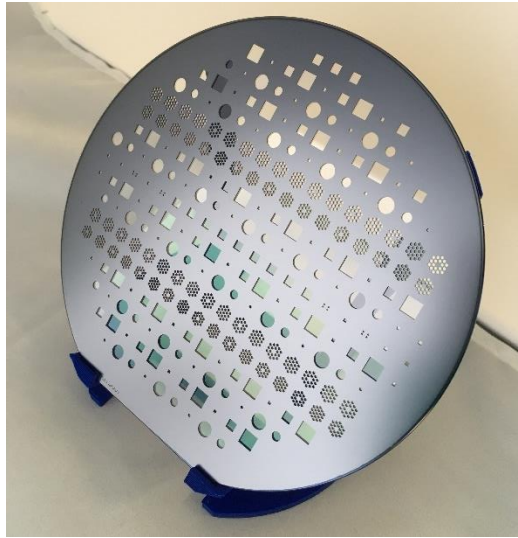


Figure 1: Backside of a 150 mm GaN-on-Si wafer with up to 5 mm diameter cavities fabricated via deep-reactive ion etching

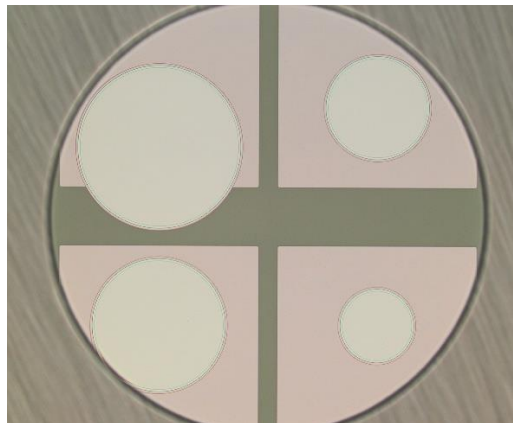


Figure 2: Frontside metal pads on GaN epitaxy seen from the backside through a trenched backside access cavity.