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Youssef Hamdaoui, Idriss Abid, Katir Ziouche, F Medjdoub. [Invited] Local substrate removal for next generation GaN-on-Silicon power transistors. 14th Topical Workshop on Heterostructure Micro-electronics (TWHM) 2022, Aug 2022, Hiroshima, Japan. hal-03828927

HAL Id: hal-03828927

<https://hal.science/hal-03828927>

Submitted on 25 Oct 2022

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Local substrate removal for next generation GaN-on-Silicon power transistors

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GaN-on-Si lateral transistors suffer from poor critical electrical field strength of the Si substrate together with a parasitic conduction at the buffer/substrate interface leading to device breakdown. In order to suppress the parasitic conduction phenomenon, local Si substrate removal (LSR) was proposed in 2010 [1]. The Si substrate removal around the drain electrode enabled electrical isolation of the gate and source from the drain across the buffer layer/Si interface, leading to an enhanced blocking voltage of GaN-on-Si HEMT above 3 kV with low leakage current [2].

Fig.1 shows the schematic cross-section of the fabricated AlGaIn/GaN MISHEMTs after front side process, LSR technique including thick PVD AlN deposition and Cu deposition as well as an optical backside image of a wafer with and without LSR. Once the front-side processing was completed, the Si substrate was locally etched up to the AlN nucleation layer around the entire device (50 μm away from the sidewalls). Fully functional transistors with a slight drop of the maximum current density were observed due the thermal dissipation degradation. On the other hand, for devices with LSR / thick AlN and Cu, the substrate leakage contribution is suppressed, and the blocking voltage drastically increased with the gate-to-drain distance while still delivering low specific on-resistances (see **Fig.2**). Furthermore, we performed back-gating transients at RT on both samples in order to study the trapping effects of devices with and without LSR. The measurement procedure is divided into stress and recovery phases. For the stress phase the device is kept in trapping conditions for 10 s; then the recovery phase is immediately carried out by keeping the device in rest conditions. The recovery drain current transient is recorded for 120 s. Several bulk bias stresses are tested, from -200 V up to -1.3 kV. During the stress drain, gate and source are kept at 0 V, whereas during the recovery the drain terminal is at 1 V. The plots of the drain current transients as a function of time for the different bulk bias stress are reported in **Fig. 2**. The back-gating measurements show no trapping effects all the way to 1.3 kV for devices with LSR while the same devices without LSR under the same conditions deliver significant trapping above 600 V. As shown in **Fig. 3**, we have been able to apply the LSR technique on large normally-off transistors delivering more than 10 A. this work demonstrates that the substrate removal approach and subsequent replacement by a wider bandgap not only enable to extend drastically the operation voltage capabilities of GaN-on-Silicon HEMTs with low R_{ON} but also may allow to reduce trapping affecting the dynamic behavior of power switching transistors. This points out that a large part of the electron trapping under high bias occurs at the AlN nucleation layer and Si substrate interface.

In turn, the LSR approach also enables new type of GaN-based vertical power transistors. These transistors combine the advantages of GaN as WBG material, the vertical transistor architectures known from SiC and Si-power transistors and the affordability of silicon as substrate materials to allow power ratings up to 1.2 kV and 100 A at low cost. Vertical device operation is then enabled by selective removal of the substrate and electrical contacting the backside of the active layers directly thus yielding a true vertical membrane transistor combining all advantages inherent to a vertical architecture with an ultrathin device as shown in the center part of **Fig. 4**. A key feature of these devices is the backside drain ohmic contacts that we will optimize using a novel lift-off process within the membranes (see **Fig. 5**) by laser writing. Progress on this innovative power transistor configuration will be presented such as the ability to uniformly achieve the backside removal substrate and buffer layers within a foundry line (Bosch).

References

- [1] P. Srivastava *et al*, IEEE Electron Device Lett. 32, p.30–32 (2011)
- [2] E. Dogmus *et al*, Applied Phys. Express, 2018 11 034102

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007229. The JU receives support from the European Union's Horizon 2020 research and innovation programme and Germany, France, Belgium, Austria, Sweden, Spain, Italy.

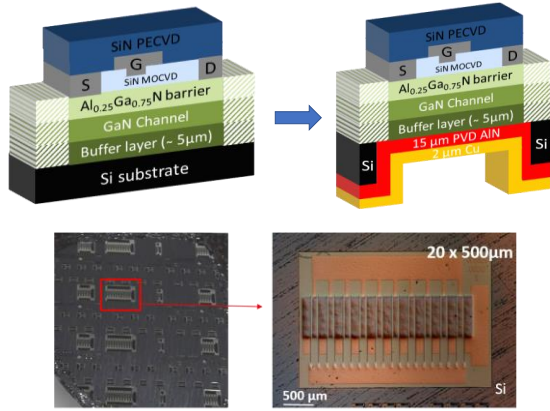


Fig.1. Schematic cross-section of AlGaIn/GaN MISHEMT after front side process, LSR technique including thick PVD AlN deposition and Cu deposition. Optical backside image of a wafer with and without LSR.

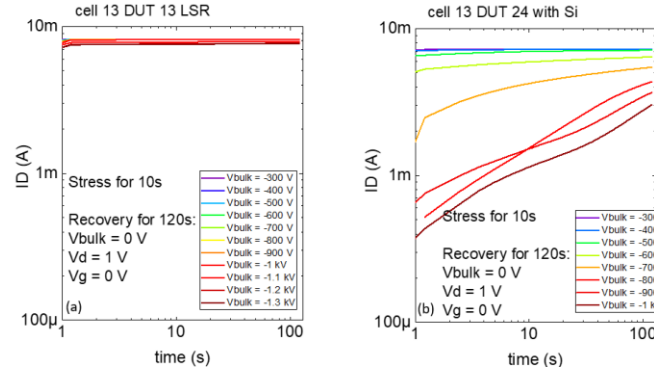
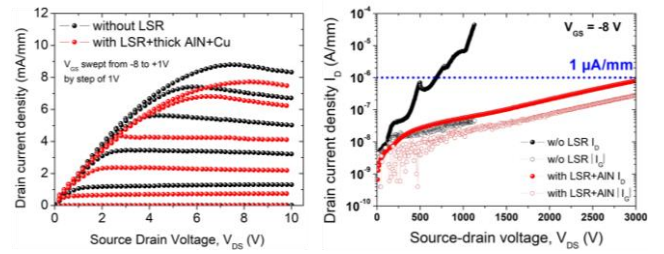


Fig.2. $I_D V_{DS}$ and off-state characteristics and Back-gating transients of normally-ON small GaN HEMTs with LSR and with Si substrate.

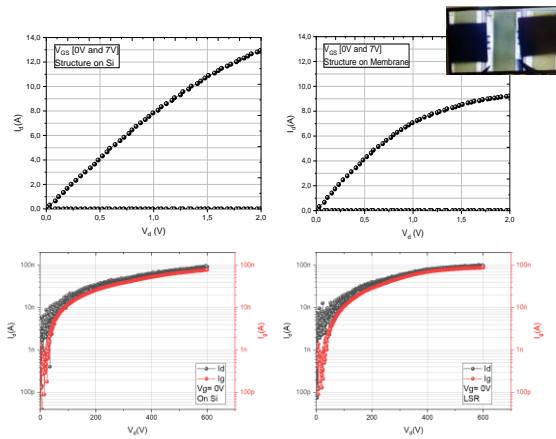


Fig.3. Output characteristics (open channel and off-state) and blocking voltage at $V_{GS} = 0V$ up to 600 V of large normally-off transistors with and without LSR

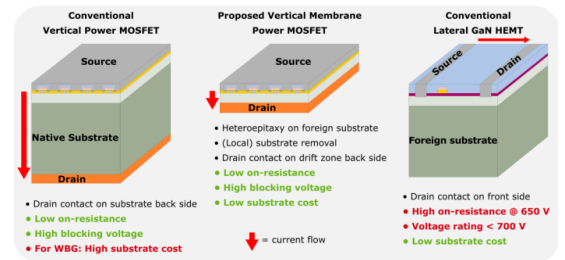


Fig.4 Cross-sectional comparison between established vertical as well as lateral power transistors and the proposed vertical membrane power transistor.

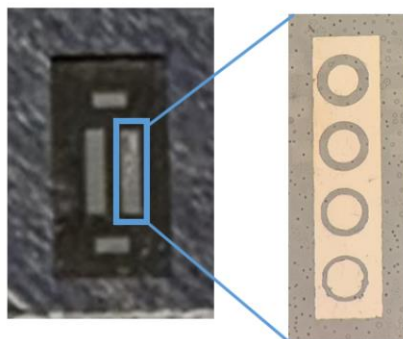


Fig.5 Optimization of a lift-off process within the membranes to assess the backside drain ohmic contacts

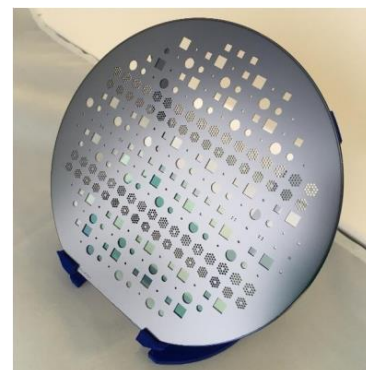


Fig.6 Backside of a 150 mm GaN-on-Si wafer with up to 5 mm diameter cavities fabricated via deep-reactive ion etching by our industrial partner Bosch