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Impact of undoped channel thickness and carbon concentration on AlN/GaN-on-SiC HEMT performances

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Abstract: We report on a vertically scaled AlN/GaN HEMT technology design optimization for millimeter-wave applications. The undoped GaN channel thickness and carbon concentration into the buffer are extensively varied and systematically characterized. It is found that a thin GaN channel, typically below 150 nm improves the electron confinement, but increases the trapping effects, especially when using shorter gate lengths. Moreover, high carbon concentration into the buffer enables not only high electron confinement but also low leakage current under a high electric field at the expense of trapping effects. As a result, the optimum epi-design enabled state-of-the-art RF performances at 40 GHz.

GaN-based RF power devices have drawn great attention owing to its outstanding material properties. Recent improvements have allowed a demonstration of a variety of next generation millimeter-wave devices such as military, SATCOM and 5G networks [1]. Nevertheless, those applications need compact system for which maintaining high power added efficiency (PAE) at high frequency with strong device robustness under high electric field become a major challenge. Moreover, further reducing the gate length to reach higher frequency requires a complete change of the standard AlGaIn/GaN epitaxial stack and device design [2–7]. Breakthrough technologies are needed to simultaneously achieve high efficiency and robustness under high output power density. GaN high electron mobility transistor (HEMT) designs have continued to enhance the power density over other III-V semiconductor technologies. Recent GaN HEMTs demonstrated attractive performances in Ka-band [8–13], Q-band [14–17] and above [18–25]. For instance, an output power density

(P_{OUT}) of 10.5 W/mm using a 160 nm AlGaIn/GaN HEMT technology at 40 GHz, with a peak PAE of 33% that was limited by a small signal gain of 6 dB [12]. A technology based on N-polar GaN Metal Insulated Semiconductor HEMTs (MISHEMTs) has shown 56% PAE at 30 GHz and 28.8% at 94 GHz while the output power density remained constant at 8 W/mm for both frequencies [8]. Recently, graded-channel (GC) AlGaIn/GaN HEMTs with an output power density of 2.1 W/mm associated with a PAE of 75% at 30 GHz has been demonstrated [26]. Nevertheless, the GC AlGaIn/GaN HEMTs are still limited to a rather low drain voltage operation below 15 V. Also, at 96 GHz an output power density of 3 W/mm has been measured with an 80 nm InAlGaIn/GaN HEMT [23]. Despite high RF performances, the reliability has not been reported yet on these technologies. Therefore, in order to satisfy the whole millimeter-wave requirements and better exploit the benefits offered by GaN transistors including a low leakage current and a high device robustness under high drain bias when downscaling the device size, the electron confinement needs to be improved while controlling trapping effects.

In this work, an extensive buffer engineering optimization has been performed in an ultrathin sub-5 nm AlN barrier layer GaN HEMTs in order to maximize the power gain while improving the electron confinement under high electric field. A variation of the carbon concentration into the buffer from $2 \times 10^{19} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ together with the undoped GaN channel thickness from 100 to 500 nm is carried out in order to evaluate the impact on both trapping effects and 2DEG electron confinement in short GaN HEMTs.

A total of 6 heterostructures have been grown by metal organic chemical vapor deposition (MOCVD) on 4-in. SiC substrates. Fig.1 (a) shows a schematic cross section of the structure consisting in an AlN nucleation layer, a variation of GaN buffer carbon concentration from $2 \times 10^{19} \text{ cm}^{-3}$ down to $1 \times 10^{18} \text{ cm}^{-3}$ combined with an undoped GaN channel thickness varying from 100 nm to 500 nm. A 3 nm AlN ultrathin barrier layer is used to benefit from both a high polarization and a high aspect ratio gate length/gate-to-channel distance L_G/a . Finally, the structures were capped with a 6 nm in-situ SiN layer to efficiently passivate the surface states. The source drain ohmic contacts have been formed by Ti/Al/Ni/Au metal stack annealed at 850°C directly on top of the AlN barrier by etching the in-situ Si₃N₄ layer. Then, Ni/Au T-gates with various gate lengths were defined by e-beam lithography. Fig.1 (b) shows

focused ion beam (FIB) images of gate lengths varying from 100 nm to 250 nm with gate-to-drain distance (L_{GD}) of 1.5 μm . Finally, a 200 nm PECVD Si_3N_4 layer was deposited as final passivation. Hall measurements at room temperature shows 2DEG concentration $n_s \sim 2 \times 10^{13} \text{ cm}^{-2}$ with a mobility around $\sim 950 \text{ cm}^2/\text{V}\cdot\text{s}$ and a sheet resistance $R_{\text{sheet}} \sim 300 \Omega/\square$ similar for all structures.

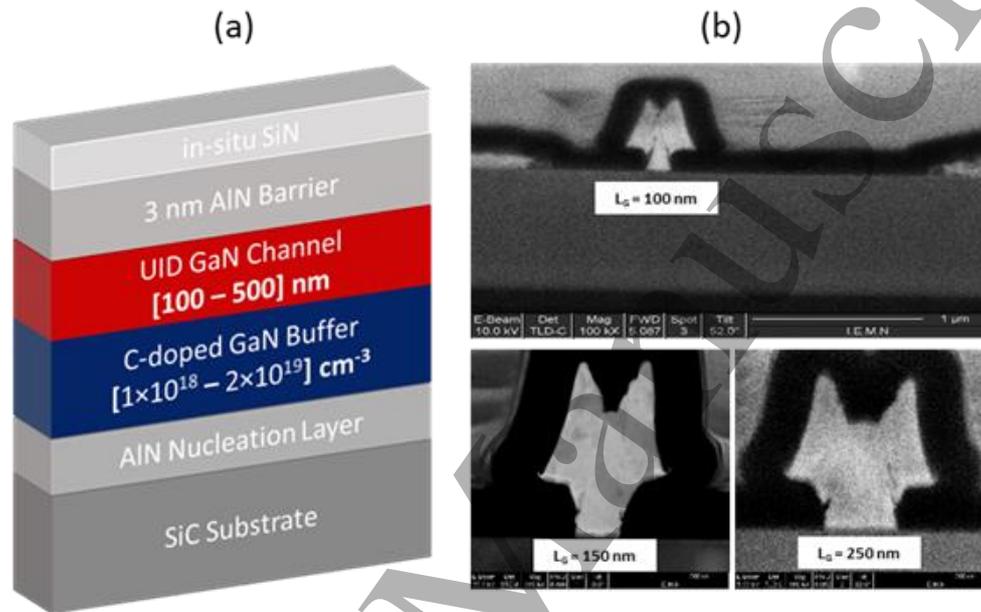


Fig.1. Schematic cross section of the epitaxial structure with C-doping concentration in the buffer varying from 2×10^{19} to $1 \times 10^{18} \text{ cm}^{-3}$ and the channel thickness varying from 100 nm to 500 nm (a), and FIB view of the fabricated gate lengths of 100, 150 and 250 nm (b).

Table I summarizes the carbon concentration and channel thickness of the GaN HEMTs used for the first study. The undoped GaN channel layer thickness is varied from 100 nm to 500 nm corresponding to the structures Tch.100, Tch.150, Tch.250 and Tch.500 while maintaining the carbon concentration into the buffer at $2 \times 10^{19} \text{ cm}^{-3}$.

Table I. Channel variation from 100 nm to 500 nm associated to a high carbon concentration of $2 \times 10^{19} \text{ cm}^{-3}$.

Structures	Channel thickness	C-doping buffer concentration
Tch.100	100 nm	$2 \times 10^{19} \text{ cm}^{-3}$
Tch.150	150 nm	
Tch.250	250 nm	
Tch.500	500 nm	

Fig.2 shows the transfer characteristics of each structure with a compliance fixed at 150 mA/mm and swept from $V_{DS} = 2 \text{ V}$ up to 20 V in order to extract the Drain Bias Induced Lowering (DIBL) parameter. This allows evaluating the quality of the 2DEG electron confinement. Pulsed I_D - V_{DS} characteristics revealing the trapping effects when using various quiescent bias points also appears in Fig. 2. The open channel DC pulsed measurements are shown at $V_{GS} = +2 \text{ V}$ with various quiescent drain voltages at room temperature. The specific trapping pulsed I-V protocol based on I-V characteristics has been settled with the following quiescent bias points : cold point at ($V_{GQ} = 0 \text{ V}$, $V_{DQ} = 0 \text{ V}$), gate lag at ($V_{GQ} = -4 \text{ V}$, $V_{DQ} = 0 \text{ V}$) and drain lag at ($V_{GQ} = -4 \text{ V}$, $V_{DQ} = 15 \text{ V}$) using a pulse width of 1 μs and a duty cycle of 1%. $2 \times 50 \mu\text{m}$ transistors with L_{GD} of 1.5 μm and L_G of 100 nm show that trapping effects are reduced with the increase of the channel thickness as shown from the pulsed I_D - V_{DS} characteristics. However, a severe degradation of the electron confinement is observed as the DIBL parameter strongly increases from 31 mV/V for the structure Tch.100 to 357 mV/V for the structure Tch.500. Additionally, the off-state leakage current degrades linearly with thicker channel, especially at higher drain voltage, resulting in a poor device robustness. Other gate lengths were measured in order to evaluate the impact on the electron confinement for each channel thickness.

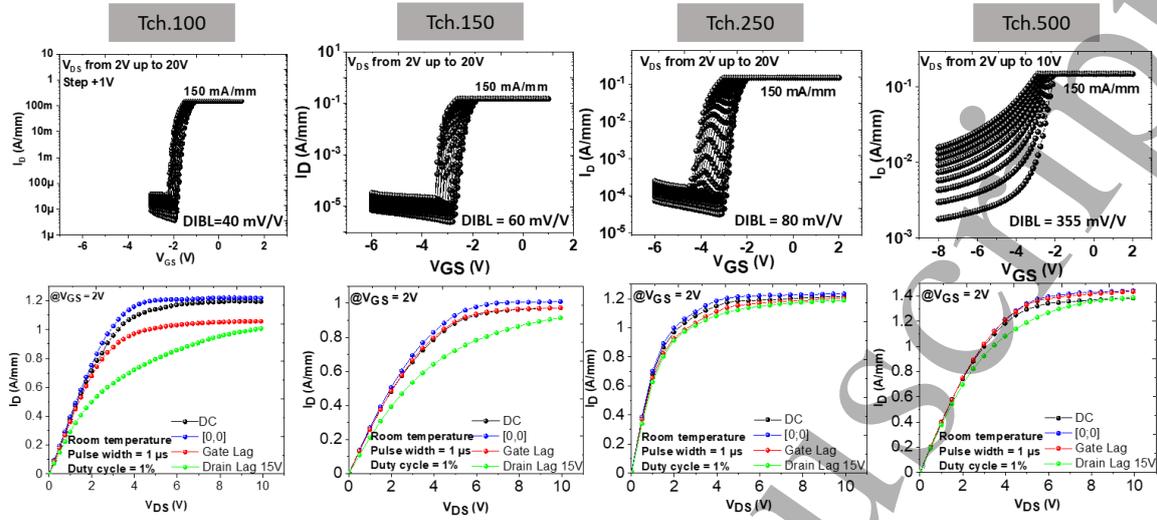


Fig.2. Transfer characteristics up to $V_{DS} = 20$ V and open channel pulsed I_D - V_{DS} output characteristics of 2×50 μm transistors with $L_{GD} = 1.5$ μm and $L_G = 100$ nm for various channel thicknesses.

Fig.3 shows the DIBL and delta pulsed output characteristics I_D - V_{DS} extracted between the drain lag at $V_{DS} = 15$ V and the cold point as a function of the gate length for each structure. The trapping effects are significantly reduced when using thicker channel thickness but inversely a degradation of the electron confinement is observed, which is reflected by the increase of the DIBL parameter. We also observed that the use of shorter gate lengths leads to a strong degradation of the leakage current especially with thicker channel. Therefore, the carbon is at the origin of the electron trapping [27–30]. Nevertheless, higher electric field resulting from shorter gate lengths requires a back barrier (in this case high resistive layer by doping compensation) close to the 2DEG, typically below 150 nm should be used when using sub-150 nm gate lengths but at the expense of higher trapping effects.

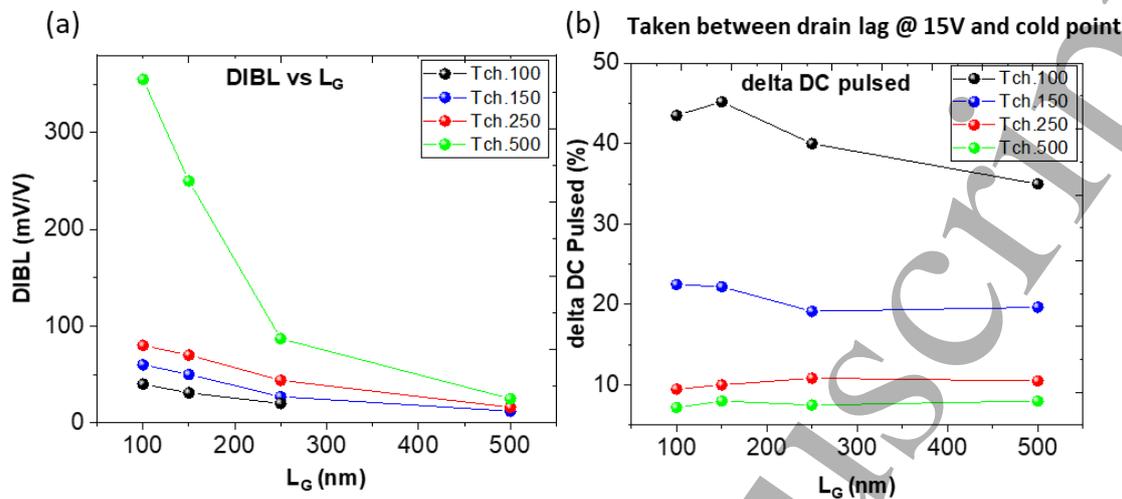


Fig.3. DIBL (a) and delta DC pulsed (b) as a function of the gate length for the structures with various channel thicknesses.

A similar study has been carried out but with a variation of the carbon-doping concentration into the buffer from $2 \times 10^{19} \text{ cm}^{-3}$ down to $1 \times 10^{18} \text{ cm}^{-3}$ for a fixed channel thickness of 100 nm as shown in Table II.

Table II. Carbon-doped variation from $2 \times 10^{19} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$ with an undoped GaN channel thickness of 100 nm.

Structures	Channel thickness	C-doping buffer concentration
High C-doping	100 nm	$2 \times 10^{19} \text{ cm}^{-3}$
Medium C-doping		$5 \times 10^{18} \text{ cm}^{-3}$
Low C-doping		$1 \times 10^{18} \text{ cm}^{-3}$

Transfer characteristics up to $V_{DS} = 20 \text{ V}$ with a compliance fixed at 150 mA/mm and pulsed I_D - V_{DS} characteristics of $2 \times 50 \mu\text{m}$ transistors with $L_{GD} = 1.5 \mu\text{m}$ and $L_G = 100 \text{ nm}$ appear in Fig. 4. The reduction of the carbon concentration into the buffer clearly leads to reduced trapping effects but on the other hand to a degradation of the electron confinement reflected by a significant increase of the drain leakage current and threshold voltage shift as a function of the drain bias.

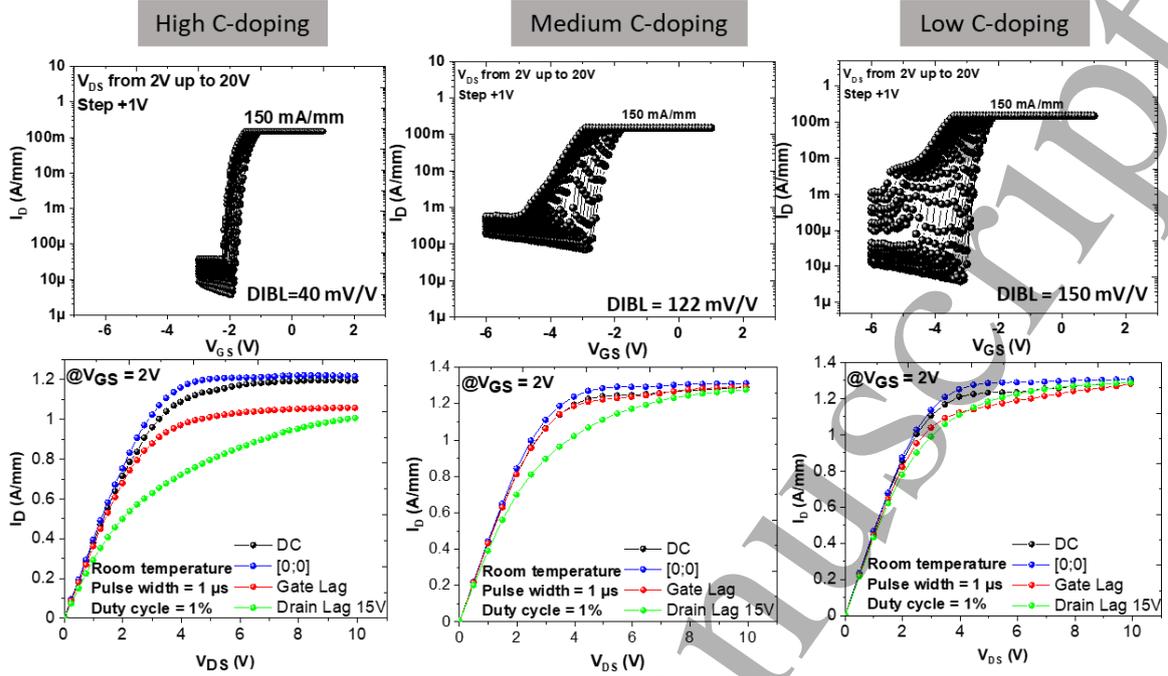


Fig.4. Transfer characteristics up to $V_{DS} = 20$ V and open channel pulsed I_D - V_{DS} output characteristics of $2 \times 50 \mu m$ transistors with various carbon-doping ($L_{GD} = 1.5 \mu m$ and $L_G = 100$ nm).

Fig. 5 shows the DIBL and delta pulsed output characteristics I_D - V_{DS} extracted between the drain lag at $V_{DS} = 15$ V and the cold point as a function of the gate length for each structure. The trapping effects are significantly reduced when using lower carbon concentration but inversely a degradation of the electron confinement is observed with a higher DIBL, especially for shorter gate lengths. This further confirms that the carbon concentration into the buffer plays a critical role and must be carefully optimized since it affects not only the device performances, but also the trapping effects as well as the robustness under high drain bias. The carbon doping concentration is required to be high enough in order to achieve highly resistive buffer but generate acceptor traps that can capture channel electrons.

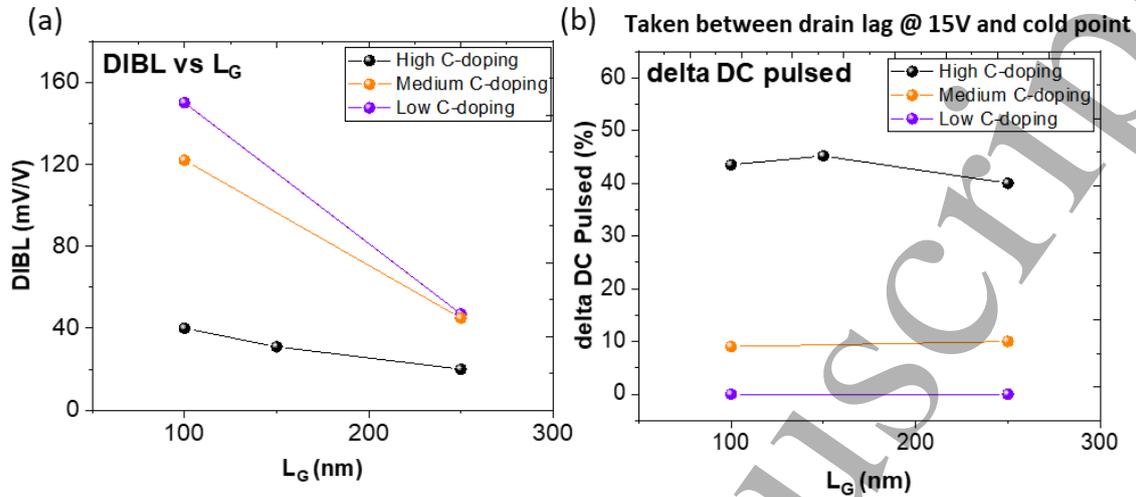


Fig.5. DIBL (a) and delta DC pulsed (b) as a function of the gate length of $2 \times 50 \mu\text{m}$ transistors with various carbon-doping.

CW and pulsed Load-pull measurements at 40 GHz have been performed on devices using 100 nm channel thickness and high C-doping buffer concentration. Details of the power bench used for these measurements can be found in [31]. According to our study, this heterostructure enables higher voltage operation despite the use of a gate length as short as 100 nm. Fig. 6 shows a $2 \times 50 \mu\text{m}$ transistor with $L_G = 100 \text{ nm}$ and $L_{GD} = 0.5 \mu\text{m}$ delivering a state-of-the-art PAE above 70% at $V_{DS} = 30 \text{ V}$ (deep class AB) with a corresponding saturated power density of 5.1 W/mm in pulsed conditions. In CW, a PAE of 58% associated with an output power density of 4.3 W/mm is obtained under the same bias conditions. Therefore, a high carbon concentration into the buffer enables outstanding power performances owing to the possibility to operate at higher drain bias despite residual trapping effects.

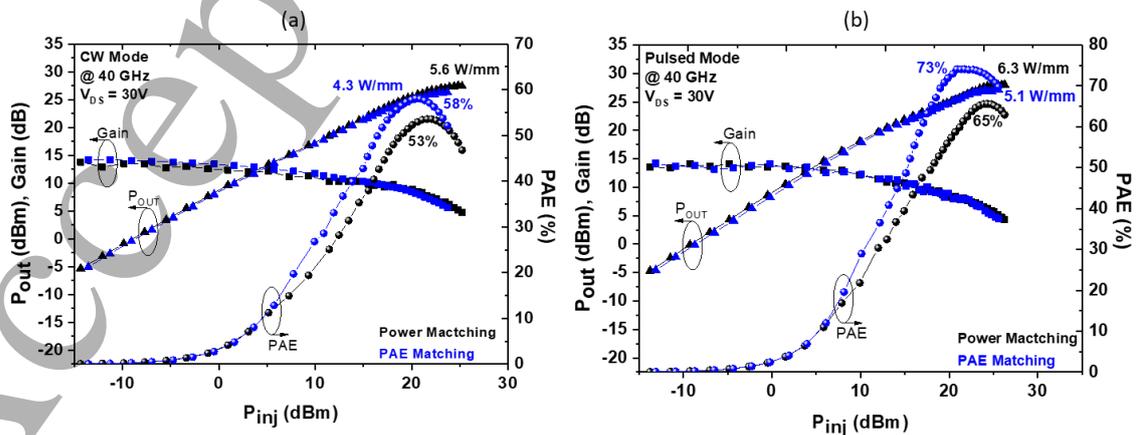


Fig.6. CW and pulsed large signal performances at 40 GHz for a $2 \times 50 \mu\text{m}$ transistor with 100 nm channel thickness and high C-doping buffer ($L_G = 100 \text{ nm}$ and $L_{GD} = 0.5 \mu\text{m}$) at $V_{DS} = 30 \text{ V}$.

In this study, we evaluated the impact of various carbon-doping concentration into the buffer and undoped GaN channel thickness on the device performances. A matrix based on an extensive experimental variation of these two parameters as a function of the gate length showed a clear trade-off between electron trapping and short channel effects. Thinner undoped channel typically below 150 nm with high carbon doping into the buffer exhibits a good electron confinement and low leakage current under high electric field at the expense of trapping effects. In contrast, a thicker channel reduces trapping effects but degrades the electron confinement when using short gate lengths. Furthermore, with lower carbon concentration, the electron confinement degrades but trapping effects are strongly reduced, which is attributed to the reduction of point defects and nitrogen vacancies enhanced when using higher carbon concentration. Therefore, the channel thickness and the carbon concentration are subject to a clear trade-off with respect to the DIBL and electron trapping in short GaN HEMTs. Consequently, a careful choice of those parameters enables enhancing the device performances and robustness under high electric field (e.g. short gate length and high drain bias). Indeed, state-of-the-art power performance at 40 GHz could be achieved with the structure using high carbon-doping and 100 nm thick undoped GaN channel.

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