# Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories

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***Abstract*—This work presents the energy advantages allowed by the technology and voltage scaling of spin-transfer torque magnetic random access memories (STT-MRAMs) based on perpendicular double-barrier magnetic tunnel junction (DMTJ), with two reference layers. DMTJ is benchmarked against the single-barrier MTJ (SMTJ) based alternative, and a comprehensive evaluation is carried out through a cross-layer simulation framework, considering a state-of-the-art Verilog-A based SMTJ and DMTJ compact models, along with a 0.8 V FinFET technology. Simulation results show that thanks to the lower voltage operating point, DMTJ-based STT-MRAM allows energy savings for write/read operations of about 38%/45%, as compared to its SMTJ-based counterpart. Moreover, scaling from the 28 nm down to the 20 nm node, the DMTJ-based offers improvements in terms of write/read energy of about 29%/33% at the expense of longer access times.**

***Index Terms*—Double-barrier magnetic tunnel junction (DMTJ), FinFET, STT-MRAM, embedded memory, energy-efficient, low-voltage**

## I. Introduction

Spin-transfer torque magnetic random-access memory (STT-MRAM) technology has grown in popularity thanks to its promising features, which include a relatively large endurance, reduced area footprint, inherent non-volatility, compatibility with CMOS processes, and ability to operate at low-voltages [1]–[3]. In addition to application domains such as standalone and embedded non-volatile memories (NVMs), where STT-MRAMs have shown maturity, embedded NV cache memory has shown interesting characteristics not only in studies based on conventional CMOS technology, but also in designs that use low-power technologies like FinFET and TFET [2], [4], [5], to cryogenic applications to enable low-power computing [6]–[8]. In particular, the study reported in [4] presents a fine-grained technology scaling study of STT-MRAMs based on single- and double-barrier magnetic tunnel junctions (MTJs) [SMTJ and DMTJ], along with FinFET technology. Despite the promising DMTJ-based STT-MRAM results in terms of energy, and based on the insight that DMTJ-based STT-MRAM cells can operate at much lower voltages in contrast to SMTJ-based alternative [9], further energy improvements can be exploited.

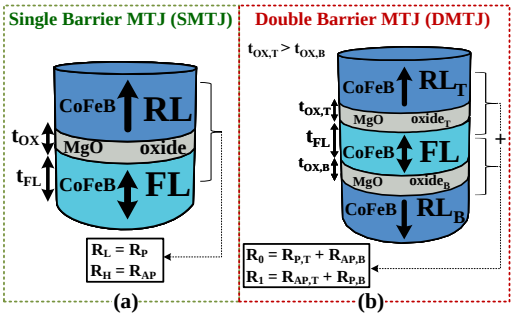


Fig. 1. Device sketch of (a) single-barrier MTJ (SMTJ) and (b) double-barrier MTJ (DMTJ) structures.

Under this framework, we present the energy advantages allowed by the technology and voltage scaling of DMTJ-based STT-MRAMs. In our study, DMTJ-based STT-MRAM is mainly compared against the SMTJ-based solution. The main results of this work demonstrate that, as compared to SMTJ-based STT-MRAM, the DMTJ-based proposal allows the memory architecture to operate at a lower voltage operating point, enabling energy savings of about 38% and 45% for write and read access times, respectively, at the cost of increased write/read access latency of about 47%/10%.

The remainder of this work is organized as follows. Section II briefly introduces single and double MTJ devices. Section III presents the simulation setup used in this work, and provides obtained results at bitcell- and memory architecture-level. Finally, Section IV concludes this work.

## II. Double-Barrier versus Single-Barrier Magnetic Tunnel Junctions

Fig. 1 shows the STT SMTJ and DMTJ, which consist of a stack of two and three ferromagnetic (FM) layers, respectively, along with thin oxide barrier/s between its FM layers [10], [11]. For the SMTJ (DMTJ) device (see Fig. 1(a) [Fig. 1(b)]), the top (top and bottom) FM layer, known as

the reference layer (RL) ($RL_{\mathrm{T}}$ and $RL_{\mathrm{B}}$, respectively), has a fixed magnetization orientation. Both devices present one FM, known as free layer (FL), which has a variable magnetization orientation, i.e., parallel (P) or antiparallel (AP) with respect to that of the RL (two RLs in the DMTJ), thus giving rise to two possible states. For the SMTJ, the resistance states can be high ($R_{\mathrm{H}}$) [AP orientation] or low ($R_{\mathrm{L}}$) [P orientation], based on the relative orientation of magnetization of the RL and FL. Conversely, for the DMTJ, the $R_{\mathrm{H}}$ and $R_{\mathrm{L}}$, or $R_1$ and $R_0$, respectively, correspond to the FL in P (AP) and AP (P) configurations with respect to that of the top and bottom RLs, respectively, and are calculated as $R_0 = R_{\mathrm{P,T}} + R_{\mathrm{AP,B}}$ and $R_1 = R_{\mathrm{AP,T}} + R_{\mathrm{P,B}}$, where $R_{P,T(B)}$ and $R_{AP,T(B)}$ are the P and AP resistances associated with the top (bottom) barrier. In contrast to the SMTJ, thanks to the presence of the two RLs (i.e., $RL_{\mathrm{T}}$ and $RL_{\mathrm{B}}$), the DMTJ presents an enhancement on the total torque acting on the FL [12], leading to lower switching currents [12], [13], at the cost of increased resistance (due to the extra oxide barrier), and reduced tunnel magnetoresistance (TMR) ratio [12].

Table I reports the main SMTJ and DMTJ device parameters considered in this study. The two perpendicular MTJ structures have been coherently scaled, and described through on-purpose developed macrospin-based Verilog-A compact models [10], [11]. As stated in Table I, we take into account the effect of process variability on MTJ devices, considering Gaussian-distributed variations with a variability ($\sigma/\mu$) of 5% and 3% for the MTJ cross-section area and TMR ratio, respectively, and 1% for $t_{\mathrm{OX}}$, $t_{\mathrm{OX,T}}$, $t_{\mathrm{OX,B}}$, and $t_{\mathrm{FL}}$ [10]. Note, the data reported in Table I are referred to data provided in [4]. For a deep insight of the device-level modeling and analysis used in this work, we suggest the reader refer to [4].

## III. Simulation Setup and Results

Fig. 2 shows the two-stage simulation flow used in this analysis. At the circuit-level, we have carried out hybrid FinFET/STT-MTJ electrical simulations into Cadence Virtuoso environment using the Spectre simulator by exploiting a state-of-the-art Verilog-A based SMTJ and DMTJ compact models [10], [11], along with transistor models provided by a 28 nm down to 20 nm FinFET technology featuring a nominal supply voltage ($V_{\mathrm{DD}}$) of 0.8 V. For the bitcell-level analysis, we referred to the two complementary transistors one-MTJ (2T1MTJ) cells, which in addition to being the best write energy-efficient topologies according to the assessment carried out in [4], they help to mitigate the effect of source degeneration that affects the one-transistor one-MTJ configurations [1]. In particular, as shown in Fig. 2, we consider the 2T1MTJ bitcells in reverse connection (access transistors connected to FL) and standard connection (access transistors connected to RL) for SMTJ- and DMTJ-based bitcells, respectively. Bitcell-level results are then exploited for evaluations in DESTINY memory architecture tool [14]. This latter, as shown in Fig. 2, is configured with one memory bank, consisting of an array of Mats, in which each one is composed of an array of sub-arrays, along with a predecoder. The sub-array is the core memory block that includes the bitcells and peripheral circuits. It is worth mentioning that DESTINY tool was properly calibrated for the considered FinFET technology node [15].

TABLE I
SMTJ and DMTJ device parameters

| Parameter | Value (28nm, 24nm, 20nm) |
|---|---|
| Saturation magnetization - $M_S$* | $1000 \times 10^3$ A/m |
| Magnetic damping - $\alpha$* | 0.025 |
| MTJ radius - $r$* | (14, 12, 10) nm |
| MTJ cross-section area - $A$* ($\sigma/\mu$ = 5%) | (6.16, 4.52, 3.14) $\times 10^{-16}$ m$^2$ |
| Thermal stability factor - $\Delta$* | (59, 51, 44) |
| SMTJ oxide thickness - $t_{OX}$ ($\sigma/\mu$ = 1%) | 0.85 nm |
| DMTJ top oxide thickness - $t_{OX,T}$ ($\sigma/\mu$ = 1%) | 0.85 nm |
| DMTJ Bottom oxide thickness - $t_{OX,B}$ ($\sigma/\mu$ = 1%) | 0.4 nm |
| Anisotropy field × FL thickness ($\sigma/\mu$ = 1%) - ($H_k \times t_{FL}$) | (1, 1.18, 1.47)‡ |
| Resistance-area product – $RA$, $RA_t$ , $RA_b$ | 5.0 Ω·μm$^2$ |
| SMTJ resistance in P state - $R_p$ | (8.12, 11.1, 15.9) kΩ |
| SMTJ resistance in AP state at 0V - $R_{ap}$ | (20.3, 27.6, 39.8) kΩ |
| DMTJ resistance in P state at 0V - $R_0$ | (8.64, 11.8, 16.9) kΩ |
| DMTJ resistance in AP state at 0V - $R_1$ | (20.5, 27.9, 40.2) kΩ |
| TMR ratio† @ 0V ($\sigma/\mu$ = 3%) | 150 % |
| SMTJ P→AP critical current - $\lvert I_{c0(P\rightarrow AP)}\rvert$ | (40.21, 31.34, 22.35) μA |
| SMTJ AP→P critical current - $\lvert I_{c0(AP\rightarrow P)}\rvert$ | (15.29, 11.92, 8.49) μA |
| DMTJ P↔AP critical current - $\lvert I_{c0(P\leftrightarrow AP)}\rvert$ | (11.08, 8.64, 6.16) μA |

* Same value for SMTJ and DMTJ. ‡ Normalized to the 28nm technology node.
† Same value for SMTJ barrier and DMTJ top/bottom barriers, i.e., $\mathrm{TMR_{SMTJ}}(0) = \mathrm{TMR_{T(B)}}(0)$.

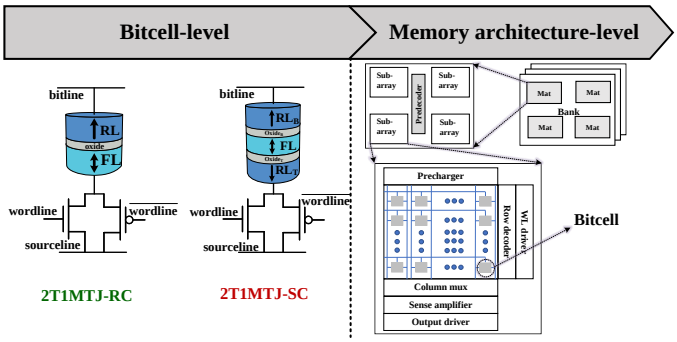


Fig. 2. Simulation flow that includes two levels of abstraction: the bitcell- and the memory architecutre-level.

### A. Bitcell-Level Results

The bitcell solutions mentioned above (i.e., the SMTJ-based 2T1MTJ-RC and DMTJ-based 2T1MTJ-SC topologies) were analyzed in terms of read and write operations through exhaustive Monte Carlo simulations. Fig. 3 shows the technology and voltage scaling results for the write operation in terms of worst-case write delay ($t_{\mathrm{write}}$) to ensure a target write error rate (WER) = $10^{-7}$ [refer to Fig. 3(a)-(b)] and the corresponding average write energy per access ($E_{\mathrm{write}}$) [refer to Fig. 3(c)-(d)] as a function of the voltage for both SMTJ- and DMTJ-based bitcells for different technology nodes. The SMTJ- and DMTJ-based bitcells correspond to an area of 231 F$^2$ and 131 F$^2$, respectively[1]. Despite the fact that the write current decreases as the MTJ resistance increases with the shrink of the device from 28 nm down to 20 nm (refer to Table I), the scaling allows lower $t_{\mathrm{write}}$, and therefore better energy savings

[1]This is the optimal bitcell topology leading to lowest $t_{\mathrm{write}}$ and $E_{\mathrm{write}}$ at a nominal $V_{\mathrm{DD}}$ (refer to [4])

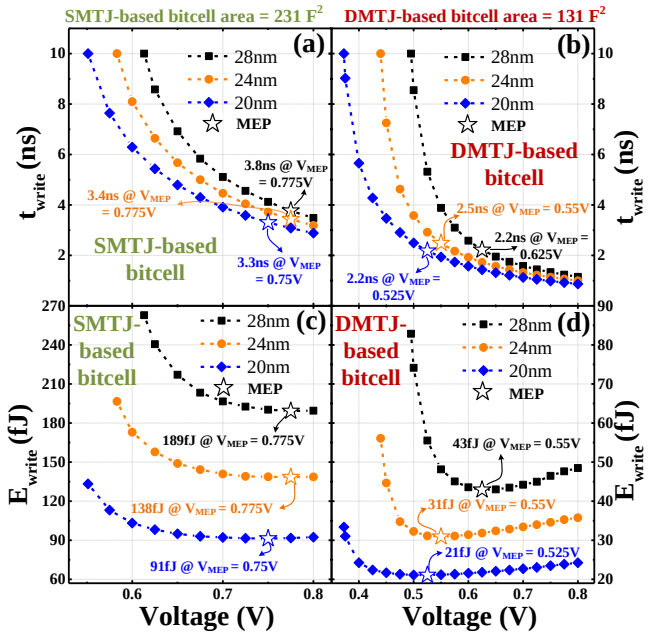


Fig. 3. Technology-voltage scaling – write operation: (a)-(b) $t_{write}$ (@WER=$10^{-7}$) and (c)-(d) average $E_{write}$, versus $V_{DD}$, for SMTJ-based 2T1MTJ-RC and DMTJ-based 2T1MTJ-SC bitcells.

for a given $V_{DD}$, as shown in Fig. 3(a)-(b) and Fig. 3(c)-(d), respectively. This is explained by the reduction of the critical switching current ($I_{c0}$) and thermal stability factor ($\Delta$), as reported in Table I. In addition to the benefits of the technology scaling, voltage scaling of the bitcell shows further energy improvements, since the voltage corresponding to the minimum energy point (MEP), $V_{MEP}$, moves towards lower operating voltages as the technology node scales.

For the reading performance of the bitcells operating at the $V_{MEP}$, we used the conventional voltage sensing (CVS) scheme [16]. The read current ($I_{read}$) is properly set to a value that is sufficiently lower than $I_{c0}$ to ensure a low read disturbance rate (RDR), which is the probability of unintentional flipping the stored bit of information during the read operation. The target RDR is $10^{-9}$ along with a read pulse width ($t_{read}$) of 1 ns [16]. Afterwards, for the considered bitcell topologies and technology nodes, we have calculated the read energy ($E_{read}$) and voltage sensing margin ($V_{SM}$), which is the difference of the $V_{BL}$ in high and low resistance states, i.e., $V_{SM} = V_{BL(AP)} - V_{BL(P)}$. Accordingly, Fig. 4 shows the technology and voltage scaling for the read operation in terms of $V_{SM}$ [refer to Fig. 4(a)] and normalized $E_{read}$ [refer to Fig. 4(b)]. It is worth noting in Fig. 4 that the $V_{SM}$ remains almost the same when the bitcells are operating on either $V_{DD}$ or $V_{MEP}$, mainly due to the adopted CVS scheme. When compared to the SMTJ-based bitcell, the DMTJ-based solution presents reduced voltage sensing margins (–59%, on average) with the technology scaling. From Fig. 4(b), in which each node is normalized to the bitcell operating at nominal voltage $V_{DD}$ = 0.8 V, the SMTJ-based bitcell at $V_{MEP}$ shows a slight difference as compared to the case at nominal $V_{DD}$. This is because the $V_{MEP}$ of SMTJ-based bitcells is very close

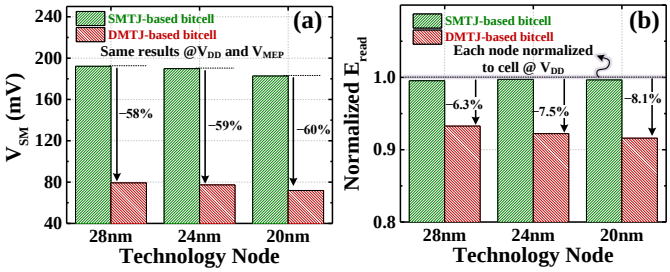


Fig. 4. Technology-voltage scaling – read operation: (a) voltage sensing margin, and (b) normalized $E_{read}$. Note, each node is normalized to the bitcell operating at nominal voltage.

to the nominal $V_{DD}$ [see Fig. 3(c)]. Conversely, the $V_{MEP}$ of DMTJ-based bitcell is much lower (–32%, on average) than the nominal $V_{DD}$, leading to reduced $E_{read}$ of about 7.3%, on average.

Table II summarizes the write and read bitcell-level results of the SMTJ- and DMTJ-based solutions while considering the bitcells operating at the MEP resulted from the technology-voltage scaling analysis. Performance results for write (@WER = $10^{-7}$) and read (@RDR = $10^{-9}$) operations show that, in contrast to SMTJ-based bitcell, DMTJ-based bitcells are more energy-efficient under write/read access of about 77%/42%, thanks to the lower voltage operating point (i.e., $V_{MEP}$), at the cost of reduced (–60%) $V_{SM}$ and increased (34%) write delay. Despite the fact that the considered bitcells present small $V_{SM}$, this issue can be addressed by employing different approaches [17].

### B. Architecture-Level Results

The study in [4] shows a comparison between SRAM vs STT-MRAMs, reporting that STT-MRAM presents increased write/read access times as compared to SRAM for a memory capacity from 32 kB to 2 MB. However, due to the SRAM higher interconnection complexity, this penalty is reduced for larger memory capacities. From these results, we choose a memory capacity of 512 kB, and evaluate the energy benefits allowed by the technology and voltage scaling. Accordingly, Fig. 5 shows the architecture-level comparative results in terms of access times [see Fig. 5(a)-(b)] and energy consumption per access [see Fig. 5(c)-(d)] obtained for different nodes.

TABLE II
SUMMARY RESULTS OF BITCELL WRITE AND READ PERFORMANCE.

| Bitcell type | $V_{MEP}$ (mV) | Writing Operation | | Reading Operation | | |
|---|---|---|---|---|---|---|
| | | Write Delay [ns] | Write Energy [fJ] | Read Current [µA] | Read Energy [fJ] | Voltage Sensing Margin [mV] |
| **28-nm node** | | | | | | |
| SMTJ* | 775 | 3.8 | 189 | 26.1 | 9.06 | 192 |
| DMTJ† | 625 | 2.2 | 43 | 7.2 | 0.94 | 79.3 |
| **24-nm node** | | | | | | |
| SMTJ* | 775 | 3.4 | 138 | 18.7 | 6.10 | 190 |
| DMTJ† | 550 | 2.5 | 31 | 5.1 | 0.63 | 77.3 |
| **20-nm node** | | | | | | |
| SMTJ* | 750 | 3.3 | 91 | 11.9 | 3.54 | 183 |
| DMTJ† | 525 | 2.2 | 21 | 3.3 | 0.35 | 72.0 |

* 2T1MTJ-RC (231 F²) for SMTJ  † 2T1MTJ-SC (131 F²) for DMTJ

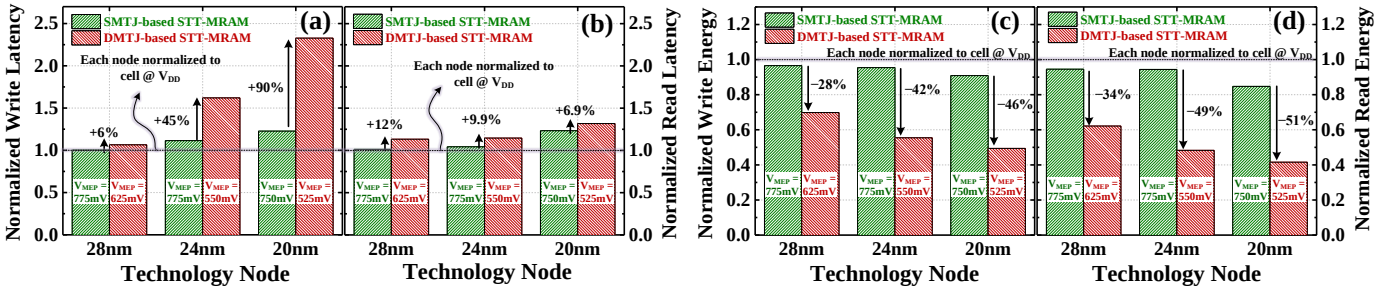


Fig. 5. Memory architecture-level results of 512 kB SMTJ- and DMTJ-based STT-MRAMs normalized to its bitcells operating at nominal $V_{DD}$ = 0.8 V. Latency results in terms of: (a) write access time, and (b) read access time. Energy per access results: (c) write, and (d) read energy consumption.

Here, the reported data considers STT-MRAMs operating at $V_{MEP}$ (refer to Table II), and normalized to its characteristics when operating at the nominal $V_{DD}$. From Fig. 5(a)-(b), we can observe that in contrast to SMTJ-based STT-MRAM, the DMTJ-based solution exhibits a penalty in terms of write and read access times of about 47% and 10%, respectively, on average. Moreover, while the penalty in terms of read access time remains relatively low, the penalty in terms of write access is increased at more scaled nodes (90% at the 20 nm node) due to the lower $V_{MEP}$ allowed by the DMTJ-based alternative. This latter (i.e., lower $V_{MEP}$), permits larger energy savings as shown in the normalized energy per access results of Fig. 5(c)-(d). Here, we can observe that, as compared to the SMTJ-based STT-MRAM, DMTJ-based counterpart has lower write and read energy of about 38% and 45%, respectively, on average. Finally, in addition to the above-mentioned energy benefits, leakage has been also evaluated, showing that leakage presented in STT-MRAM based on DMTJ memory is lower by 57% as compared to the SMTJ alternative.

## IV. Conclusions

In this work, we investigated the impact of technology and voltage scaling on writing and reading performance of a 512 kB STT-MRAM. The analysis has been carried out through a circuit-to-memory architecture level simulation framework, exploiting Verilog-A SMTJ and DMTJ compact models and a 0.8 V FinFET technology, while taking into account realistic scaling and variation effects on both MTJ and FinFET devices. Circuit-level comparative results demonstrate that, operating at the $V_{MEP}$, DMTJ-based bitcells present better technology-voltage scalability, proving to be the most energy-efficient solution under write/read access at the cost of reduced sensing margins and penalty in write delay. Obtained memory architecture-level results show that combining technology with voltage scaling, DMTJ-based STT-MRAM can enable potential read/write energy savings, at the cost of increased write/read access times. This indicates DMTJ-based STT-MRAM to be a competitive candidate for low-power/voltage applications.

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