DMTJ-Based Non-Volatile Ternary Content Addressable Memory for Energy-Efficient High-Performance Systems

Kevin Vicuna, Luis-Miguel Procel, Lionel Trojman, Ramiro Taco

DMTJ-Based Non-Volatile Ternary Content Addressable Memory for Energy-Efficient High-Performance Systems

***Abstract*—This paper explores performance of non-volatile ternary content addressable memories (NV-TCAMs), exploiting double-barrier magnetic tunnel junction (DMTJ) as comparatively evaluated with respect to the single barrier MTJ (SMTJ)-based solution. The comparison is performed at the circuit-level, considering different memory words. Overall, simulation results show that the DMTJ-based NV-TCAM is a good alternative to replace SMTJ-based NV-TCAM, mainly due to the search operation improvement. In particular, for a 144-bit NV-TCAM word operating at a nominal voltage of 1.1 V, the DMTJ-based solution offers improvements in terms of energy and search error rate of 14% and 66%, respectively, while showing similar search delay as the SMTJ-based NV-TCAM.**

***Keywords*—Double-barrier magnetic tunnel junction; Ternary content-addressable memories; energy-efficiency.**

I. Introduction

Ternary content-addressable memories (TCAMs) are being widely used in various applications such as: lookup tables, network switches, IP-filters and virus checkers [1]. This is mainly due to its attractive hardware engine that offers outstanding performance, through a fully parallel search in a single clock cycle [1]. The TCAM cells are typically based on complementary metal–oxide–semiconductor (CMOS) devices, organized as two Static Random-Access Memory (SRAM) cells. Although the high-speed search operation of SRAM-based TCAMs, the cells suffer from high standby power, due to the increased leakage current of scaled of CMOS technologies [2], [3]. Moreover, another issue is the TCAM cell area cost, mainly because of the need of two SRAM cells for each TCAM cell [1], [4].

Magnetic tunnel junctions (MTJs) has been raised as a promising alternative to deal with the technology scaling limitations of classical semiconductor-based architectures. This is due to some attractive properties like high-speed/low-power, small area footprint, long data retention time and compatibility with CMOS process [5]. MTJs have been proposed for a wide spectrum of applications, from logic and memory [6]–[8], to cryogenic and unconventional computing [9], [10]. In particular, logic-in-memory architecture based on spin-transfer torque (STT) perpendicular MTJs (p-MTJs) has been exploited to build voltage-dividing NV-TCAM cells [11], which typically requires fewer transistors than SRAM-based TCAMs. However, the voltage-dividing NV-TCAM presents low reliability in search operation due to the limited resistance ratio of the p-MTJs. Furthermore, typical single-barrier based NV-TCAMs present the challenge of reducing currents, limiting their use for energy-efficient low-voltage non-volatile applications. To deal with this, an effective strategy would be the use of double barrier MTJ (DMTJ) instead of conventional single barrier MTJ (SMTJ) [12], [13].

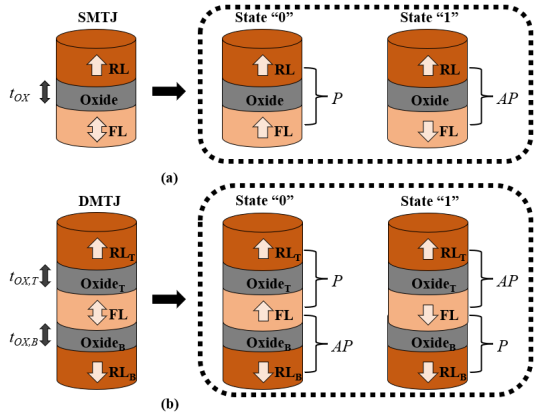

Fig. 1. (a) Structure of single-barrier magnetic tunnel junction (SMTJ); (b) Structure of double-barrier magnetic tunnel junction (DMTJ).

In the context above, this study investigates the impact of using DMTJs in the NV-TCAM cell proposed in [11]. The NV-TCAM was designed considering a commercial 65–nm CMOS technology, along with a state-of-the-art Verilog-A DMTJ compact model [13]. Overall, benchmark analysis was performed between SMTJ- and DMTJ-based NV-TCAMs for different memory words, thus demonstrating that DMTJ-based NV-TCAMs can ensure energy savings at the expense of a slight search delay penalty.

This paper is organized as follows; Section 2 describes the MTJ devices used in this work. Section 3 briefly introduces the voltage-dividing based NV-TCAM architecture used in this work as reference. Section 4 compares and discusses simulation results. Finally, Section 5 summarizes the main conclusions of the work.

978-1-6654-4141-4/21/$31.00 ©2021 IEEE

TABLE I
SMTJ AND DMTJ PARAMETERS

Parameter	Description	SMTJ	DMTJ
D	Diameter of MTJ [nm]	32	
t_{FL}	Free Layer Thickness [nm]	1.2	
Δ *	Thermal Stability factor	71	
$Ic_{P\Rightarrow AP}$	Critical Current for P $\Rightarrow$ AP $[\mu A]$	49	14
$Ic_{AP\Rightarrow P}$	Critical Current for AP $\Rightarrow$ P $[\mu A]$	20	14
t_{OX}	Oxide Barrier Thickness [nm]	0.85	-
$t_{OX,T}$	Oxide Barrier Thickness Top [nm]	-	85
$t_{OX,B}$	Oxide Barrier Thickness Bottom [nm]	-	4
TMR @0V	TMR Ratio With Zero V_{bias} [%]	140	
RA	Resistance-Area Product $[\Omega * \mu m^2]$	5	
R_P	Resistance in P State $[K\Omega]$	6.1	6.9
R_{AP} @0V	Resistance in AP State $[K\Omega]$	14.7	15.9

II. MTJ DEVICES

Fig. 1(a) shows the configuration of the SMTJ, which consists of three layers: two ferromagnetic layers and an oxide layer. The reference layer (RL) has a fixed magnetic orientation, while the free layer (FL) has a variable magnetization orientation. The FM layers (RL and FL) are separated by a thin oxide barrier. The relative magnetization orientation of the FM layers determines the state of the device, being parallel (P) or anti-parallel (AP), corresponding to the low and high resistances (i.e., R0 and R1), respectively. Fig. 1(b) shows the DMTJ with two reference layers, the upper and bottom layer (RL_T and RL_B). The FL is sandwiched between two thin Mg0 oxide barriers that interfaces with the RLs, which are in antiparallel magnetization to each other. Due to the presence of the two reference layers, the FL can be simultaneously in a P(AP) and AP(P) with respect to the RL_T and RL_B, respectively. Similar to the SMTJ, the DMTJ also has two states, which are described as the sum of two individual resistances of the stack formed between FL and the top and bottom RLs. The importance of having two antiparallel RLs are to improve the total torque acting on the FL, which allows reduced switching currents [12], [13]. At the device-level, both SMTJ and DMTJ were described with a Verilog-A based macrospin compact model [13], [14].

Table I reports the MTJ device parameters considered in this work.For comparison purposes, SMTJ and DMTJ devices were properly calibrated by following the scalability trends reported in [15]. In our study, we have exploited state-of-the-art Verilog-A based STT-MTJ compact models for both SMTJ and DMTJ [13], [14], along with transistors models provided by the 65–nm process design kit (PDK) of TSMC.

III. NV-TCAM CELL AND WORKING PRINCIPLE

Fig. 2 shows the considered NV-TCAM cell with nine transistors and two DMTJs (9T-2DMTJ), whose logic-in-memory topology is composed by a sense amplifier and a comparison logic, which forms a voltage-diving network between the M6 transistor and the MTJ device/s. The sense amplifier embedded in the cell is responsible for reading the state of the node Q, which is delivered by the comparison logic circuitry.

A typical TCAM cell performs mainly search operations, while read and write are less frequent. The 9T-2DMTJ TCAM cell has two bits of storage that make possible three types of

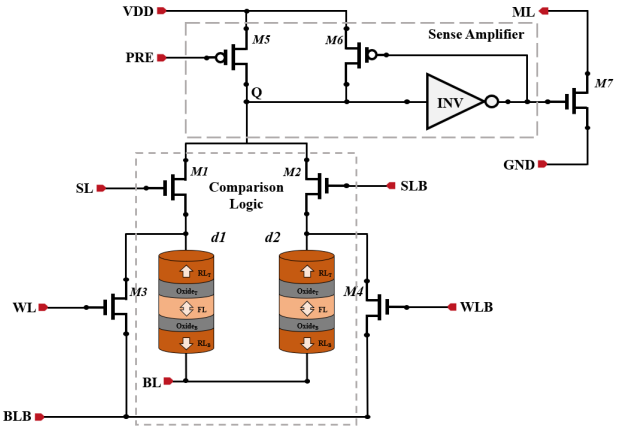

Fig. 2. Voltage-dividing based 9T-2DMTJ NV-TCAM cell [11].

data: zero (“0”), one (“1”) and don’t care (“X”), which are encoded in the states of the MTJs (d1 and d2). To store states “0” and “1”, the MTJs (d1, d2) are written to (0,1) and (1,0), respectively, by properly asserting the bit line (BL), word line (WL), and their complements [i.e., BL bar (BL) and WL bar (WLB)], while the search lines (SL and SLB) are fixed to the ground (GND) [16]. As for “X”, (1,1) values are stored into (d1, d2). The search operation consists of two phases: precharge and evaluation [11], [16]. In the precharge phase, the PRE signal, along with the SL and SLB are connected to GND. Therefore, the node Q is charged to VDD, and the match line (ML) is also precharged to VDD by an external precharge transistor. Afterwards, in the evaluation stage, the PRE signal is connected to VDD, and the SL and SLB are respectively driven to GND (VDD) and VDD (GND) to search a “0” (“1”). Table II summarizes all the possible search cases. In the case of a match, the connected MTJ (asserted by the SL/SLB signal) is in the high resistance state (“1”), while the Q node will remain charged to V_{DD} through the transistor M6 (see Fig. 2). In the case of mismatch, the connected MTJ is in a low resistance state (“0”) and node Q will be discharged to GND. The search result is sensed by the inverter, which delivers a full swing signal to the gate of a pass transistor, generating a short critical path between the ML and GND. Therefore, the result of the ML ensures a high speed. In addition to the cases reported in Table II, for the don’t care (“X”) search operation is done by driving the SL and SLB to GND, avoiding any possible ML discharge regardless of the stored data.

Fig. 3 shows the working principle validation of the DMTJ-based NV-TCAM cell. The timing diagram shows an example for different search operations, where precharge and evaluation phases are clearly stated within a 1 ns. As the data stored into

TABLE II
SEARCH OPERATION OF THE 9T-2MTJ NV-TCAM CELL

Stored Data		SL	SLB	ML
D	(d1, d2)	(Input Data)	(Input Data)	(Output)
0	(0, 1)	0	1	Match (search “0”)
		1	0	Mismatch (search “1”)
1	(1, 0)	0	1	Mismatch (search “0”)
		1	0	Match (search “1”)
X	(1, 1)	0	1	Match (search “0”)
		1	0	Match (search “1”)

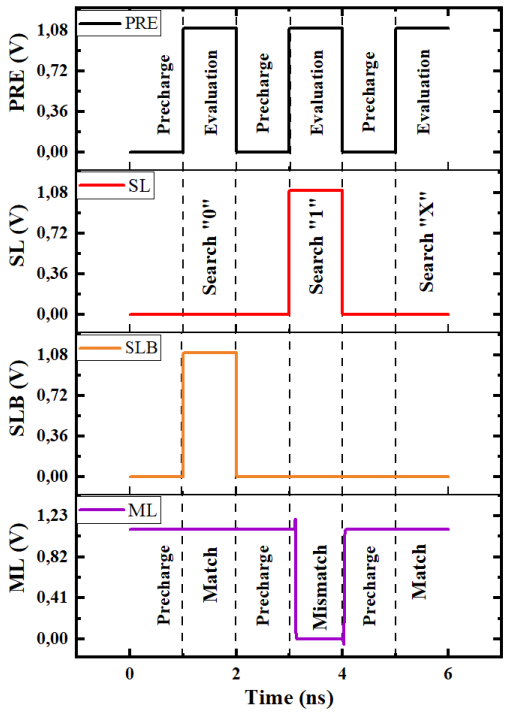

Fig. 3. Timing diagram of the 9T-2DMTJ NV-TCAM cell for different search operations.

the cell is "0", the ML remains high except when searching "1", as shown in 3 to 4 ns timeframe.

IV. Simulation Results

We considered and evaluated the N-bit TCAM architecture presented in Fig. 4 for different memory words ranging from 16- to 144-bits at a V_{DD} of 1.1 V. The 65–nm transistors and compact models of the STT-MTJs (SMTJ and DMTJ) have been exploited into Cadence Virtuoso environment to perform circuit-level simulation through exhaustive Monte Carlo simulations. The reliability and performance, in terms of write and search operations, are done by considering the same transistor sizing of the sense amplifier and comparison logic (refer to Fig. 2) for SMTJ- and DMTJ-based NV-TCAM. Thus, ensuring a fair benchmark analysis of SMTJ- versus DMTJ-based NV-TCAM words.

Fig. 5 shows the search results obtained considering the NV-TCAM words in the worst-case scenario, i.e., where there is only one mismatching bit. Figs. 5(a) and (b) show the search-error-rate (SER) results as a function of the NV-TCAM word length and supply voltage, respectively. The former [refer to Fig 5(a)], shows that for the NV-TCAM words

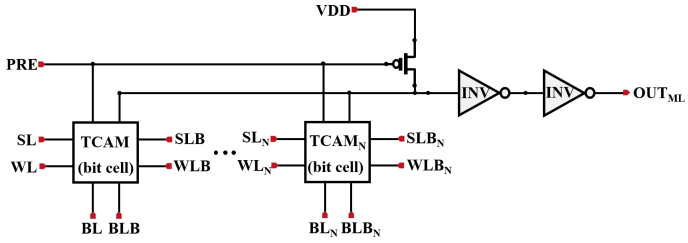

Fig. 4. 9T-2DMTJ NV-TCAM N-bit Word circuit structure.

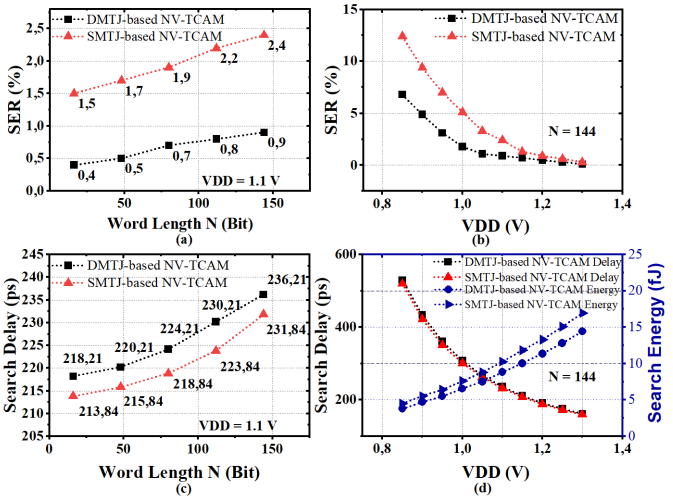

Fig. 5. (a) Search-error-rate (SER) for different NV-TCAM word lengths at 1.1 V. (b) SER of the 144-bit NV-TCAM word with respect to different supply voltages. (c) Search delay versus different word lengths at 1.1 V. (d) Search delay and energy of the 144-bit NV-TCAM word for different supply voltages.

operating at a V_{DD} of 1.1 V, the DMTJ-based alternative presents SER improvements of about 66.64% (on average) as compared to the SMTJ-based counterpart. The latter [refer to Fig 5(b)], shows that DMTJ-based NV-TCAM offers lower SER, although it is comparable at higher ($> 1.2V$) supply voltages. The search operation results in terms of delay and energy are presented in Figs. 5(c)-(d). From Fig. 5(c), the search delay is evaluated as function of the word length, showing that, as compared to the SMTJ-based NV-TCAM, the DMTJ-based solution has a delay penalty of 2.25% (on average) when operating at 1.1 V. Finally, Fig. 5(d) shows a comparison of delay and energy versus different supply voltages. As compared to SMTJ-based alternative, the DMTJ-based NV-TCAM is the best solution, allowing energy savings of approximately 14.57% (on average), while also assuring comparable search delays. This is explained by the small difference in resistance between DMTJ and SMTJ, as reported in Table I.

Based on the insight that the DMTJ devices can operate at lower supply voltages compared to SMTJs as reported in [8], we conclude our analysis by evaluating the reliability of the write operation for different operating voltages. Therefore, it suggests that further energy savings can be achieved for the NV-TCAM search operation. While the SMTJ-based NV-TCAM works correctly from 0.95 V, the DMTJ-based alternative works at lower V_{DD}, from 0.85 V. This is explained due to the lower switching currents allowed by the DMTJ [12]. Comparing the results of the SMTJ- and DMTJ-based NV-TCAM with the allowed minimum operating voltage of 0.95 V and 0.85 V respectively, the DMTJ-based solution allows energy savings of about 41%, at the expense increased (50.73%) delay. Despite working at lower voltage, the DMTJ-based NV-TCAM has comparable SER.

Table III reports an overall comparison between the SMTJ- and DMTJ-based 144-bit NV-TCAMs operating at 1.1 V. In terms of search operation, as compared to the SMTJ-based

alternative, the DMTJ-based solution offers improvements in terms of energy saving and search error rate of 14% and 66%, respectively, while the delay performance of proposed NV-TCAM was affected by 1.85%.

Note that the cell area has been also considered according to the layout design shown in Fig. 6

TABLE III
PERFORMANCE COMPARISON WITH THE SAME SIMULATION CONDITIONS

	9T-2SMTJ	**9T-2DMTJ**
Non-Volatility	Yes	Yes
$SER_{144}[\%]$	2.4	0.9
$T_{search}[ns]$	0.231	0.236
$E_{search}[fJ/bit]$	10.27	8.82
Write Path	1T-1MTJ	1T-1MTJ
$V_{write}[V]$	1.1	1.1
$V_{select}[V]$	1.1	1.1
$Width_{select}[nm]$	240	240
$E_{write}[pJ/bit]$	1.01	0.747
$CellArea[\mu m^2]$	8.53	8.53

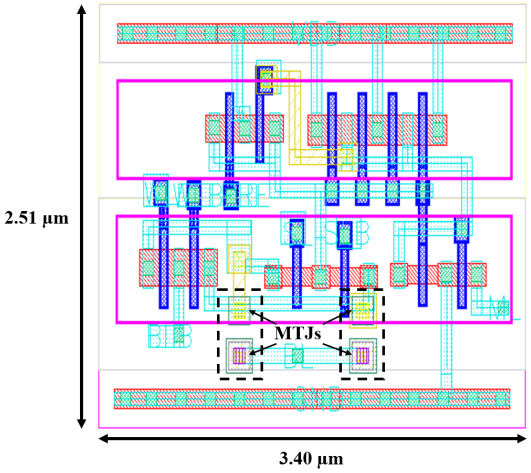

Fig. 6. Layout implementation of the 9T-2DMTJ NV-TCAM cell using the TSMC 65–nm CMOS design kit.

V. CONCLUSIONS

In this work, we propose the use of DMTJ devices in NV-TCAMS cells. The comparative analysis has been carried out by performing circuit-level simulations considering a 65–nm PDK along with Verilog-A based compact models for the MTJs. Obtained results show that, as compared to the SMTJ-based NV-TCAM, the DMTJ-based alternative exhibits search energy savings of 14.57% and SER improvements of 66.64% at the expense of a slight increase in search delay. We also suggest reducing the operating voltages, showing that the DMTJ-based solution offers further energy improvements in contrast to the SMTJ-based counterpart, while presenting comparable SERs. Our study suggests that DMTJ-based solutions is a noteworthy alternative for high-performance energy-efficient non-volatile TCAM systems.

REFERENCES

[1] K. Pagiamtzis and A. Sheikholeslami, "Content-addressable memory (CAM) circuits and architectures: a tutorial and survey," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 712–727, 2006.

[2] M. Alioto, *Enabling the Internet of Things: From Integrated Circuits to Integrated Systems*. Springer, 2017.

[3] D. Kudithipudi and E. John, "On estimation of static power-peformance in TCAM," in *2008 51st Midwest Symposium on Circuits and Systems*. IEEE, 2008, pp. 783–786.

[4] S. Matsunaga, S. Miura, H. Honjou, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, and T. Hanyu, "A 3.14 um 2 4t-2mtj-cell fully parallel tcam based on nonvolatile logic-in-memory architecture," in *2012 Symposium on VLSI Circuits (VLSIC)*. IEEE, 2012, pp. 44–45.

[5] X. Fong, Y. Kim, R. Venkatesan, S. H. Choday, A. Raghunathan, and K. Roy, "Spin-Transfer Torque Memories: Devices, Circuits, and Systems," *Proceedings of the IEEE*, vol. 104, no. 7, pp. 1449–1488, 2016.

[6] E. Garzón, B. Zambrano, T. Moposita, R. Taco, L.-M. Prócel, and L. Trojman, "Reconfigurable CMOS/STT-MTJ Non-Volatile Circuit for Logic-in-Memory Applications," in *2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)*. IEEE, 2020, pp. 1–4.

[7] W. Zhao, M. Moreau, E. Deng, Y. Zhang, J.-M. Portal, J.-O. Klein, M. Bocquet, H. Aziza, D. Deleruyelle, C. Muller *et al.*, "Synchronous non-volatile logic gate design based on resistive switching memories," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 2, pp. 443–454, 2013.

[8] E. Garzón, R. De Rose, F. Crupi, L. Trojman, G. Finocchio, M. Carpentieri, and M. Lanuzza, "Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs," in *2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, 2019, pp. 85–88.

[9] E. Garzón, R. De Rose, F. Crupi, A. Teman, and M. Lanuzza, "Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications," *IEEE Transactions on Nanotechnology*, vol. 20, pp. 123–128, 2021.

[10] G. Finocchio, M. Di Ventra, K. Y. Camsari, K. Everschor-Sitte, P. Khalili Amiri, and Z. Zeng, "The promise of spintronics for unconventional computing," *Journal of Magnetism and Magnetic Materials*, vol. 521, p. 167506, 2021.

[11] S. Matsunaga, A. Katsumata, M. Natsui, T. Endoh, H. Ohno, and T. Hanyu, "Design of a 270ps-access 7-transistor/2-magnetic-tunnel-junction cell circuit for a high-speed-search nonvolatile ternary content-addressable memory," *Journal of Applied Physics*, vol. 111, no. 7, p. 07E336, 2012.

[12] G. Hu, J. Lee, J. Nowak, J. Sun, J. Harms, A. Annunziata, S. Brown, W. Chen, Y. Kim, G. Lauer *et al.*, "STT-MRAM with double magnetic tunnel junctions," in *2015 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2015, pp. 26–3.

[13] R. De Rose, M. d'Aquino, G. Finocchio, F. Crupi, M. Carpentieri, and M. Lanuzza, "Compact modeling of perpendicular STT-MTJs with double reference layers," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 1063–1070, 2019.

[14] R. De Rose, M. Lanuzza, M. d'Aquino, G. Carangelo, G. Finocchio, F. Crupi, and M. Carpentieri, "A compact model with spin-polarization asymmetry for nanoscaled perpendicular MTJs," *IEEE Trans. Electron Devices*, vol. 64, no. 10, pp. 4346–4353, 2017.

[15] E. Garzón, R. De Rose, F. Crupi, L. Trojman, G. Finocchio, M. Carpentieri, and M. Lanuzza, "Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework," *Integration - the VLSI Journal*, vol. 71, pp. 56–69, 2020.

[16] C. Wang, D. Zhang, L. Zeng, E. Deng, J. Chen, and W. Zhao, "A novel mtj-based non-volatile ternary content-addressable memory for high-speed, low-power, and high-reliable search operation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 4, pp. 1454–1464, 2018.