A novel integrated cooling packaging for high power density semiconductors

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***Abstract*—This work investigates a packaging solution for high power density semiconductors ($> 200\,\mathrm{W/cm^2}$), allowing for a dramatic reduction in size and complexity of power electronics modules. The multiple layers in standard packaging structures degrade the cooling efficiency due as they lengthen the path between dies and heatsinks. Here, we reduce the layer count by merging the ceramic substrate and the heat exchanger in a single part. CFD simulations and experimental validation are performed on a single-chip cooling packaging, and demonstrate a 10-20 % reduction in thermal resistance over more traditional cooling solutions.**

***Index Terms*—Insulation, packaging, computational fluid dynamics (CFD), Cooling, power electronics, high power density**

I. Introduction

Power semiconductor devices today show a tendency towards faster, smaller and denser chips. This leads to high power loss densities, which makes their thermal management difficult. The package structure of the module strongly affects the electrical and thermal properties of the system. A lot of different packaging solution are investigated in the literature, and many implement liquid cooling to improve thermal performance. For example, [1] shows that jet impingement cooling concept is better than micro-channel cooler. The thermal resistance was reduced from 0.76 K/W to 0.45 K/W for 16-dies cooler, that gives a thermal resistivity r_{th} ($r_{th} = R_{th} \times A_{heat}$) of 0.29 $\mathrm{cm^2}$K/W for each die. A double-side cooling concept is investigated in [2], improving the performance further from 0.47 $\mathrm{cm^2}$K/W to 0.33 $\mathrm{cm^2}$K/W thermal resistivity, at the cost of a more complex structure.

However, most of these packages structure are formed with many layers of material, making the thermal path longer, and less efficient. Reducing the layer count between the semiconductors and the heatsinks would lead to a simpler, and possibly more efficient heat path. For example, [5] shows a better cooling performance using fewer layers of material. The thermal resistance was reduced by 30 % using a heatsink structure integrated into the baseplate (Fig 1b) compared with the traditional structure [6]. Furthermore, the size of the module could be 40 % smaller than that of a module with a traditional structure (Fig 1a) [6]. This work presents a novel packaging design for high power density semiconductors devices which brings them closer to the heat sinks, by removing many of the layers which are present in a classical package.

TABLE I: Thermal requirements

Die size $[mm^2]$	power losses P_{loss}[W]	th. resistance R_{th}[K/W]	th. resistivity $r_{th}[\mathrm{cm^2K/W}]$	inlet T T_{in}[°C]
9.1×9.1	200	< 0.3	< 0.25	23

Two cooling concepts for a water-cooled heat sink are introduced in section II: one based on jet-impingement, the other on channel-flow. The cooling design optimisation, by the means of Computational Fluid Dynamics (CFD) modelling, is described in section III. The CFD predictions are then compared with experimental results in section IV.

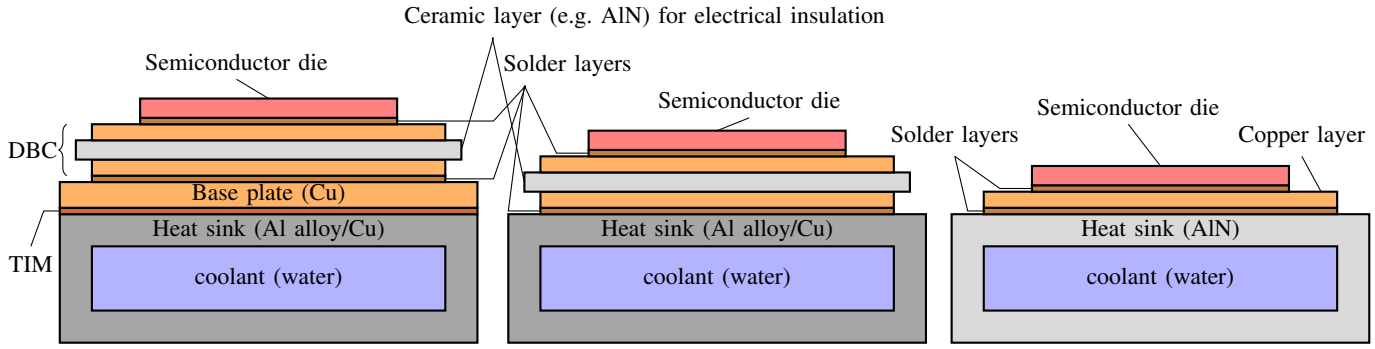
II. Integrated cooling design

In the traditional power module packaging (Fig. 1a), the die is soldered onto a Direct Bonded Substrate (DBC). The copper layers of the DBC help to dissipate the heat from the die to the heat sinks and the ceramic layer provides electrical insulation. For higher mechanical strength and for better heat spreading, the DBC is soldered onto a metal baseplate (typically copper or an aluminium composite), which is bolted to a water-cooled cold-plate through a layer of thermal interface material (TIM).

The proposed structure (Fig. 1c) integrates the liquid cold-plate directly in the ceramic layer. This results in a dramatic reduction in size and complexity of the thermal path, which can lead to a better cooling performance.

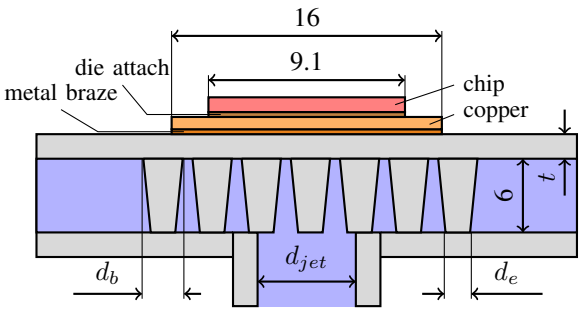
Considering the thermal requirements (Tab. I) and the technical possibilities and limitations related to the manufacturing of a ceramic heatsink, two cooling concepts are investigated: jet impingement and channel flow. The first is depicted in Fig. 2, with an inlet located at the bottom of the heatsink, under the chip, causing the liquid to impinge on the top internal surface of the heatsink. Both left and right sides of the heatsink remain open and serve as outlets. The second concept (channel flow) has a similar internal structure, with the inlet located on one side and the outlet at the other.

In order to increase the heat transfer area and generate turbulence in the system, pin-fins are needed in the cooling

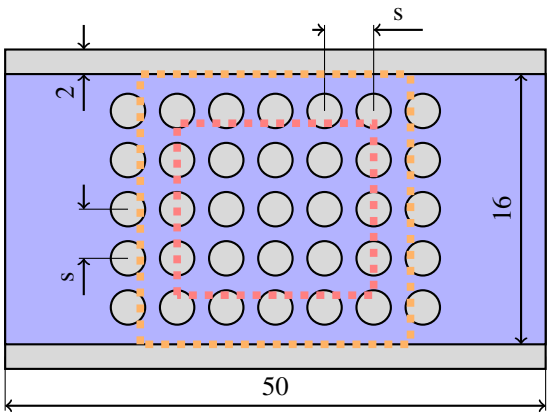


(a) Traditional module packaging (b) Integrated heat sinks into baseplate packaging (state-of-the-art) (c) Novel embedded packaging

Fig. 1: Schematic comparison between the traditional, state-of-the-art and the novel power module packaging



(a) CAD parameter of the jet impingement cooling concept



(b) Cross section in middle of the channel under the chip

Fig. 2: Structure considered for the design, showing the design parameters

channel. Circular/conical pin structures are selected because they are easy to manufacture. Based on the parameter on Fig. 2b, four designs are investigated numerically (CFD) with different flow rate, jet diameter (d_{jet}) and distance between pins s. The geometry parameters for the four designs are shown in Tab. II.

Longer pins provide better cooling as they have a larger surface, and reduce the pressure drop (resulting in lower pumping power). Therefore, we set their length to the maximum value which is practical from a manufacturing point of view

TABLE II: Geometry parameters of the four designs

Parameter	t[mm]	d_b[mm]	d_e[mm]	d_{jet}[mm]	s[mm]
Design 1	1.5	2	2	6 to 9	3.3
Design 2	3	2	2	6 to 9	3.225
Design 3	1.5	2.5	1.8	6 to 9	3.3
Design 4	3	3	1.8	6 to 9	3.225

TABLE III: Layer materials properties

Material	Thermal conductivity λ[W/(mK)]	Thickness b[µm]
Chip (4H-SiC)	370	500
Die Attach (Ag)	100	50
Copper (Cu)	394	300
Metal braze (AgCuTi10)	361	10
Aluminium Nitride (AlN)	170	1500/3000
Aluminium alloy	170	1500/3000
thermal grease (TIM)	5	5
Insulator of DBC (AlN)	170	650
Base plate (Cu)	394	3000

(6 mm). The pin spacing is minimised to get the highest pin density possible under the chip in order to increase the heat exchange surface. The spacing between side walls and pins is also minimised to ensure proper coolant flow under the chip in the case of the channel flow.

The properties (thermal conductivity and thickness) of the materials used for the simulations of the traditional packaging as well as the concepts described here are presented in Tab. III.

III. CFD CALCULATIONS

A. CFD approach

Ansys CFD is used for the simulations presented here. An automated procedure, described in more detail in [7] allows for the simulation of many parameters configurations from Tab. II. For all simulations, the boundary conditions are set as

follows: 200 W power dissipation at the chip surface; constant volumetric flow (1 to 4 L min^{-1}) at the inlet; zero-pressure condition at the outlet; conservative flow condition for all interface regions; adiabatic condition for all the external walls.

B. CFD results

The thermal resistances of the four jet impingement cooler designs from Tab. II are plotted in Fig. 3 and Fig. 4 as a function of pumping power. Both graphs present the same results but with different color scales (flow rate and jet diameter). Each point in these figures corresponds to a simulation with a different flow rate (1 to 4 L min^{-1}), with the largest flow rates obviously resulting in lower thermal resistance, at the cost of higher pumping power. The dataset exhibits a clear Pareto-optimal front curve.

The conical pins (Design 3 and 4) show a better cooling performance (lower thermal resistance and lower pumping power) than the cylindrical pins. This is due to better heat dissipation effect and higher velocity under the semiconductor (less space at the base of the pins leads to higher velocity there).

Design 4 with $t = 3\,\mathrm{mm}$ shows better performance for low flow rate and Design 3 ($t = 1.5\,\mathrm{mm}$) is better for higher flow rate. The explanation is that for higher flow rates, most of the heat is transferred to the liquid directly under the chips; on the contrary, for low flow rates, it is advantageous to allow for more heat spreading in the ceramic so that more pin surface is involved in heat exchange with the fluid. While Design 3 is slightly better than Design 4 in absolute terms (it offers lower R_{th} as soon as sufficient flow-rate is provided), Design 4 is only slightly worse, and has a thicker AlN baseplate ($t = 3\,\mathrm{mm}$). This gives Design 4 an advantage because this thicker ceramic layer increases electrical insulation between the chip and the cooling fluid.

Fig. 3 shows that increasing the flow-rate beyond 3 L min^{-1} only slightly improves the thermal resistance, while pumping power increases dramatically. Using a small diameter jet (down to 6 mm, Fig. 4) also provides small R_{th} improvements at the cost of higher pumping power. Jet diameters of 7 mm and 8 mm offer a better trade-off between cooling performance and pumping power. Therefore Design 3 and 4 are investigated further considering a jet diameter of 7.5 mm in the following sections.

1) Channel flow vs jet impingement: Fig. 5 shows the the simulation results for the selected channel flow and jet impingement cooling designs. Jet impingement cooling is found to offer better cooling performance with much lower pumping power when compared with channel flow. As presented before, both jet impingement coolers exhibit similar cooling performances, with a higher pumping power for Design 4 because of its larger pins.

Velocity distribution maps (50 µm away from the upper wall of the cooler) are presented for these designs in Fig. 6. As analysed in [7], the jet impingement designs has two features which explain the better performance when compared with channel flow: 1- the impingement of liquid onto the hot surface

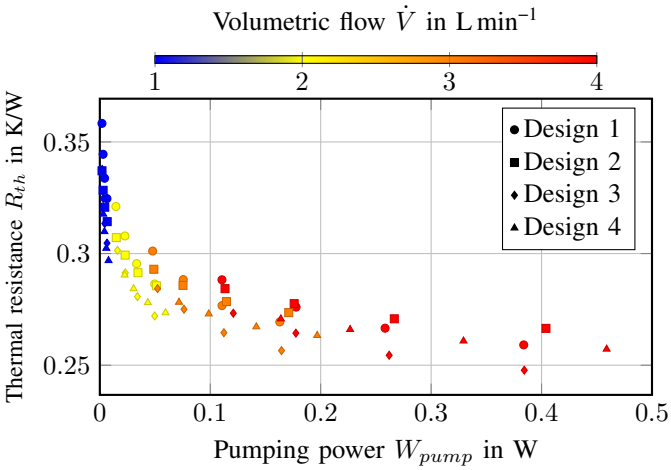


Fig. 3: Thermal resistance as a function of pumping power for all four jet impingement designs, color: flow rate

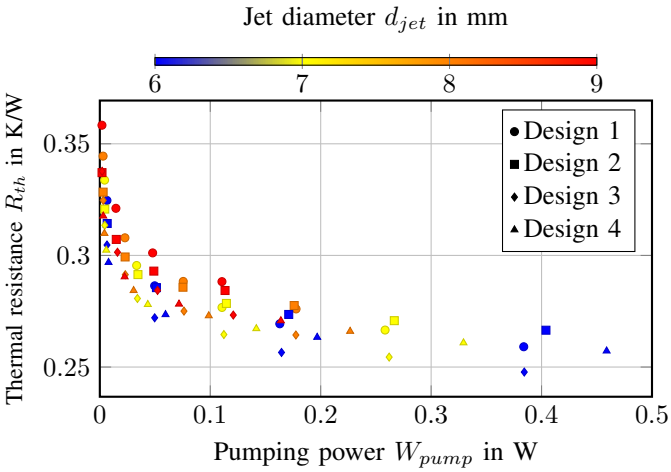


Fig. 4: Thermal resistance as a function of pumping power for all four jet impingement designs, color: jet diameter

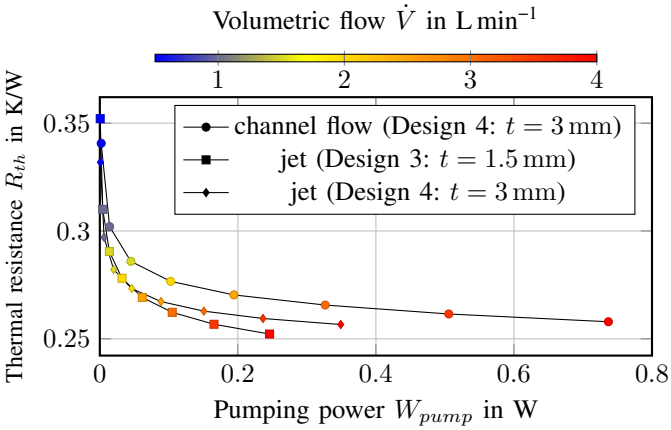
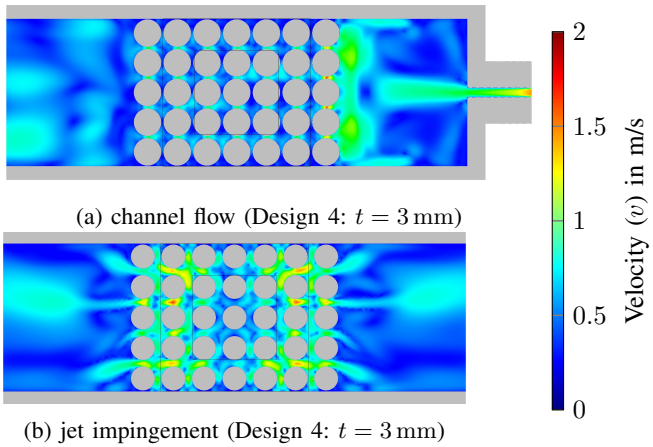


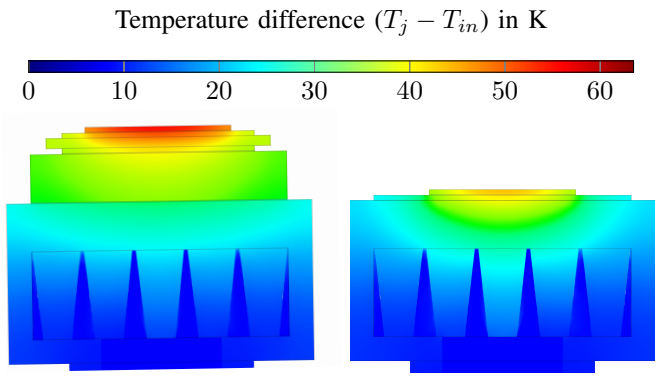
Fig. 5: Thermal resistance as a function of pumping power for different cooling concepts: channel flow and jet impingement (7.5 mm inlet diameter, AlN heatsinks).



(a) channel flow (Design 4: $t = 3\,\mathrm{mm}$)

(b) jet impingement (Design 4: $t = 3\,\mathrm{mm}$)

Fig. 6: Velocity distribution at 50 µm distance from the upper wall under the chip at $3\,\mathrm{L\,min^{-1}}$



(a) traditional packaging (b) novel packaging

Fig. 7: Temperature distribution in the traditional and the novel packaging at $3\,\mathrm{L\,min^{-1}}$

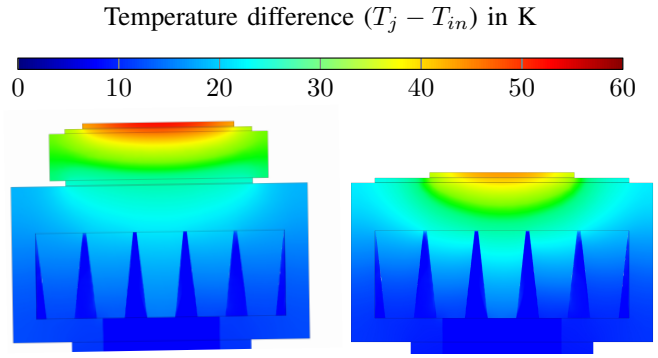
under the chip increases turbulence, hence increasing the heat exchange coefficient; 2- the jet impingement design has two outlets, so the impinging flow is split in two, resulting in much lower pressure drop.

2) Comparison with traditional packaging: Fig. 7 shows the numerical results of the temperature distribution in the traditional and in the novel design(Design 4: $t = 3\,\mathrm{mm}$) with 200 W power losses ($\sim 240\,\mathrm{W/cm^2}$). In this comparison, the traditional package is supposed to be attached to a aluminium alloy heatsink with the same internal design (Design 4) as the novel package. In this configuration, the thermal resistance is reduced from 0.32 K/W (traditional package) to 0.26 K/W (novel package). Furthermore, the AlN heatsink offers additional advantages in terms of voltage isolation: in the traditional package, electrical insulation is provided at the substrate level, where the ceramic is thin (typically 0.65 mm), while the ceramic heatsink uses a much thicker layer (here 3 mm). Furthermore, lower thermo-mechanical stress can be expected for the novel package, as the coefficient of thermal expansion of AlN (4-5 ppm/K) is much closer to that of the chips (in the order of 3 ppm/K) than Aluminium alloy (19-25 ppm/K)and copper (17.8 ppm/K).

If high voltage insulation is a concern, an obvious solution with the traditional approach is to use a thicker ceramic for the DBC substrate, and to solder the DBC directly onto copper heatsinks (Fig. 1b). The temperature distribution of such approach is shown in Fig. 8 together with that of the novel package. Here again, the proposed packaging offers better cooling performance beside its simplicity. This is summarised in Fig. 9, which shows the expected thermal resistance of the three packaging variant investigated here ("traditional", thick DBC for high voltage isolation, and integrated ceramic cooler.

IV. Experimental Study

Three metallised ceramic (AlN) cooler designs are fabricated by CeramTec. Two jet-impingement coolers (Design 3 and Design 4 with 7.5 mm jet diameter) and one channel flow



(a) DBC on copper heatsinks (b) novel packaging

Fig. 8: Temperature distribution a traditional package which would provide the same electrical insulation as the novel packaging (same AlN thickness of 3 mm) and the novel packaging at $3\,\mathrm{L\,min^{-1}}$

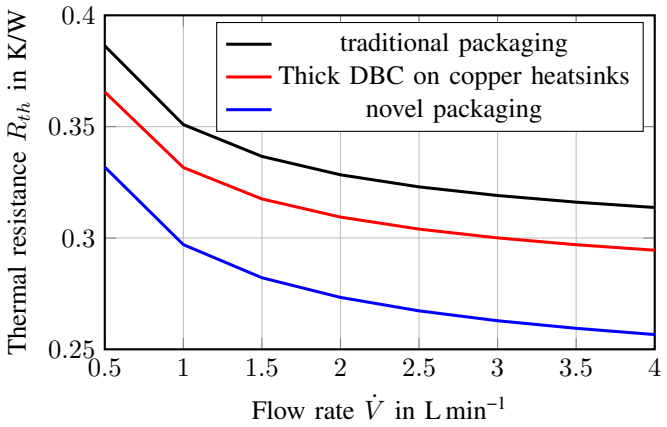
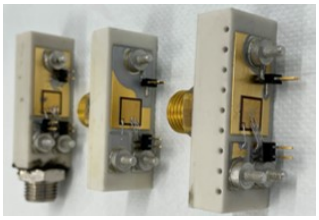
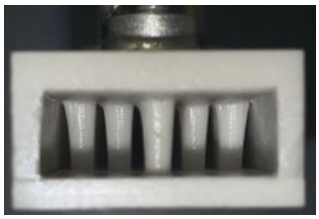


Fig. 9: Thermal resistance comparison between three possible packaging (simulation, jet impingement cooler with the same heat sinks (Design 4))



(a) The three prototypes.



(b) Side view showing the pins.

Fig. 10: The three prototypes: channel flow, jet impingement with two AlN thicknesses (1.5 mm and 3 mm);

cooler (Design 4). Copper metallisations (for the chip interconnects) are brazed onto the coolers. A $9.1 \times 9.1\,\mathrm{mm}^2$ IGBTs is then sintered on the largest metal pad and wirebonded with thick Al wedge bonds. Finally, connectors are soldered on the metal pads for the electrical connection to the outside world and a brass fitting (forming the inlet) is glued to the heatsinks. The baseplate of some heatsinks is equipped with 9 holes so that thermocouples can be inserted to monitor temperature distribution. Fig. 10 shows the populated test vehicles.

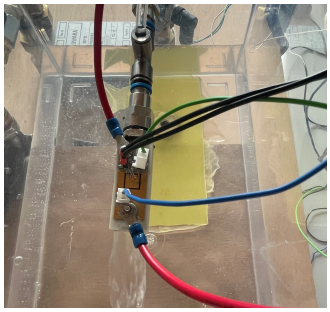
The test vehicles are then connected to a test setup comprising a fluid loop and a thermal analyser (Phase 12B, Analysis Tech) for the measurement of R_{th}. Figs. 11a and 11b show the devices under the test (DUT). A schematic of the electrical and hydraulic connections is given in Fig .11c. Regarding the liquid circuit, water is pumped into the DUT; valves (not shown in the schematic) allow to adjust the flow-rate, which is measured using a flow meter (FM); a heat exchanger, connected to a water chiller maintains the temperature in the circuit at 23 °C; pressure drop Δp is measured between the inlet and outlet (atmospheric pressure).

A. R_{th} characterisation

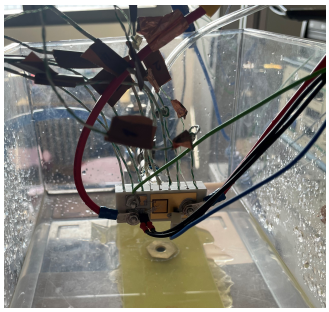
The junction temperature of the IGBT (T_j) is estimated using the collector-emitter voltage drop (V_{CE}), which is a temperature-sensitive parameter [3]. A constant gate bias (9 V) is used here. A first calibration step is performed to characterise the relationship between V_{CE} and T_j: the DUT is put into an oven to control the device temperature (measured using a thermocouple) and the corresponding V_{CE} value is monitored using the thermal analyser under a low reading current (5 mA) to limit self heating. The resulting characteristic is presented in Fig. 12.

In the measurement phase, a large collector current I_C (up to 100 A) is injected in the IGBT by the thermal analyser, to generate heat; the power injection is then briefly interrupted, and the junction temperature is measured using a 5 mA bias. The thermal resistance is then obtained by dividing the temperature difference (between the junction temperature T_j and the fluid temperature at the inlet T_{in}) by the power loss ($P_{loss} = V_{CE} \times I_C$):

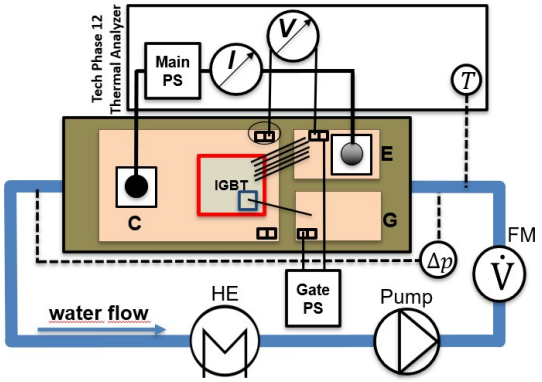
$$R_{th} = \frac{T_j - T_{in}}{P_{loss}}$$



(a) DUT (channel flow)



(b) DUT (jet, Design 4)



(c) schematic of the test setup

Fig. 11: Test setup

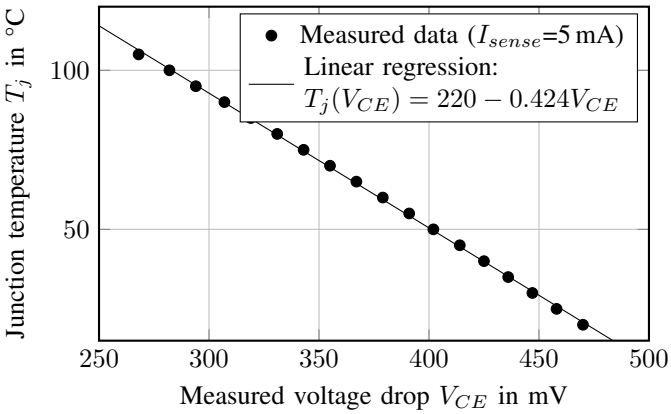


Fig. 12: Calibration the temperature-sensitive electrical parameter used for junction temperature monitoring: V_{CE} with 5 mA sense current and 9 V gate voltage.

The analyser also allow to measure the thermal impedance (i.e. the transient thermal behaviour) according to JEDEC standard JESD 51-14 [4].

B. Test results

A comparison between measured and simulated thermal resistances as a function of pumping power is shown in Fig 13. Although experimental results show some differences with CFD predictions, especially for the channel flow cooler (CF), these remain acceptable ($< 5\,\%$) and show good consistency

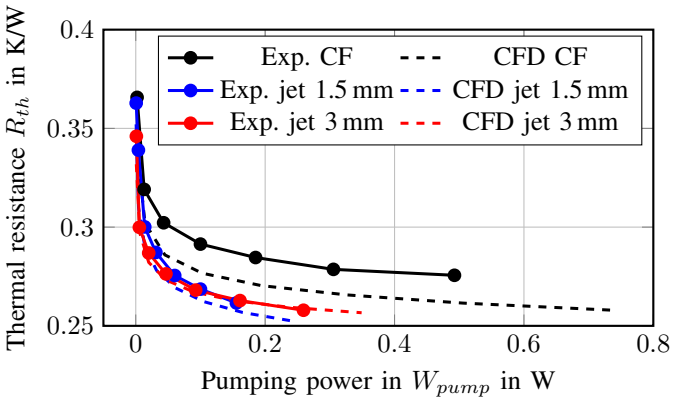


Fig. 13: Measured and simulated thermal resistances as a function of pumping power. "Exp.": experimental result; "CFD": simulation result; "CF": Channel flow configuration.

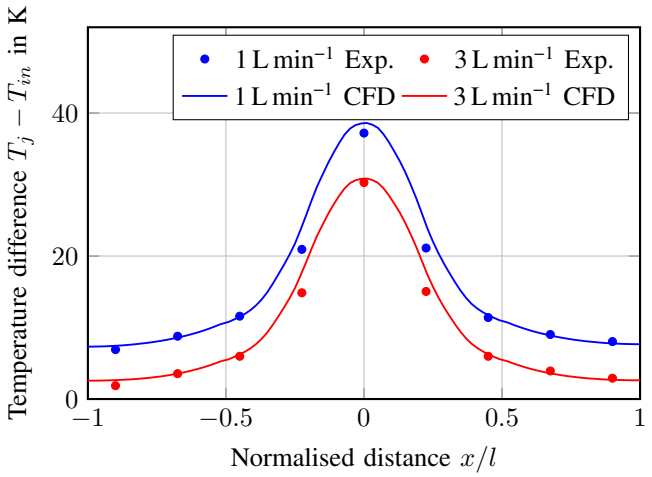


Fig. 14: Temperature distribution in the AlN for the jet cooler ($t = 3mm$), experiment ("Exp.") and simulation ("CFD").

(with the jet impingement cooler having the lowest pumping power).

A second comparison between measurement and simulation results is presented in Fig. 14. Thermocouples are inserted in the ceramic baseplate and the measured temperature distributions is compared with simulation predictions, showing a very good agreement.

Fig. 15 shows the measured peak impedance for the channel flow cooler and the jet cooler (Design 4). The jet impingement cooler has a lower impedance values than that of the channel flow (cf). The cooling performance is better for higher flow rates as discussed earlier. These results confirm the discussed results above and in subsection III-B.

V. Conclusion and Outlook

In this work, an integrated cooling system for high power density semiconductors is introduced and compared with the traditional packaging. A single-chip ($9.1 \times 9.1\,\mathrm{mm}^2$) cooling structure is optimised using CFD simulations considering

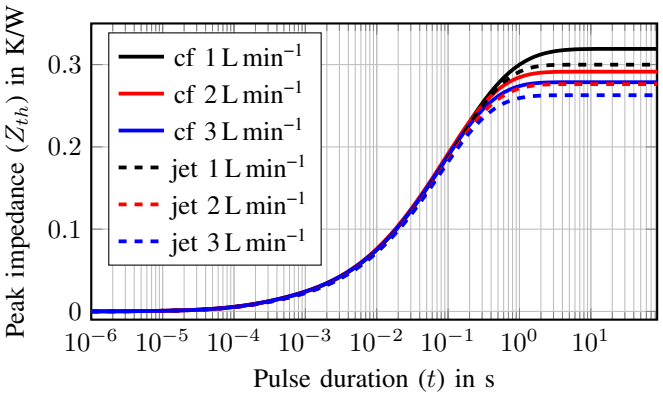


Fig. 15: Measured thermal impedance (Z_{th} for two coolers and different flow-rates.

the manufacturing process, as well as hydraulic and thermal performance. Two implementations (channel flow and jet impingement) are investigated and three prototypes are built. Simulation and experimental results are in good agreement, and show that the novel packaging offers lower thermal resistance ($R_{th} \leq 0.3\,\mathrm{K/W}$, $r_{th} \leq 0.25\,\mathrm{cm^2K/W}$) than the traditional structure or than a hypothetical package (thick DBC soldered on copper heatsink) which would provide comparable electrical insulation capability (same AlN thickness) as the novel package. Because of its lower pressure drop and higher fluid velocity, the jet impingement structure is found to be more efficient than the channel flow structure.

Acknowledgment

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