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Analysis of an Inverter-Based CMOS Envelope Detector

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Abstract—This article derives the scaling factor of a sub-threshold inverter-based envelope detector. The scaling factor was simulated at the transistor-level using BSIM4 model parameters in 180 nm CMOS. A close analysis of the the calculated scaling factor shows that the minimum and the maximum of the scaling factor are within 10 percent of those obtained in simulation, suggesting that the scaling factor of the inverter-based envelope detector biased in the subthreshold region is accurately modeled.

I. INTRODUCTION

Recent studies have shown that by 2027 battery powered Internet of Things (IoT) devices will become ubiquitous [1]. In order to minimize battery usage and prolong battery life, it will be necessary to develop energy efficient wake-up receivers (WuRx) that monitor wireless channel continuously and turn on the battery powered devices on demand.

Despite recent efforts to shorten the wake-up receiver design cycle, WuRx circuits have always been associated with limited portability across technology nodes and required significant time and effort in design, optimization, custom layout, and prototyping. Consequently, there continues to be strong interests in developing digital-friendly WuRx circuits, i.e. WuRx circuits built with digital gates.

The power consumption of wake-up receivers can be significantly reduced by using an envelope detector which eliminates the need for RF amplification and generation of LO frequency [2]. Figure 1(a) shows the inverter-based CMOS envelope detector first reported in [3]. In contrast to prior envelope-detector designs which utilized distortion in elementary amplifiers such as a common-drain amplifier [4], a common-gate amplifier [5], and a common-source amplifier [6], the inverter-based envelope detector uses the second order distortion current generated by an inverter biased in the subthreshold region to generate conversion gain [3]. The conversion gain is maximized with the transistors biased in the subthreshold region. The conversion gain is sensitive to small variations of the gate bias voltage [3]. [3] showed that by using a charge-scaling digital-to-analog conversion (DAC) circuit to generate the gate bias voltage, the circuit's sensitivity to the gate bias voltage is mitigated.

[3] shows that it is feasible to generate conversion gain with a digital inverter, but does not describe the underlying

theoretical framework for generating the conversion gain. This article addresses the knowledge gap by deriving the voltage transfer characteristic (VTC), the small signal gain, and the scaling factor of the inverter-based envelope detector biased in the subthreshold region.

The VTC relates the output voltage of an inverter to its input voltage. The VTC is derived in this article to account for the dependence of the threshold voltage on the drain-to-source voltage through the drain-induced barrier lowering (DIBL) effect. In contrast to the VTC expression derived in [7], the VTC expression produces a gradual descent near V_S , the switching voltage at which the input voltage is equal to the output voltage, and accurately models the small signal gain.

The first derivative of the output voltage with respect to the input voltage is the small signal gain (A_V). A_V can be computed at any point along the VTC. In contrast to A_V derived in [8], the A_V derived in this article is valid not only near the switching voltage, but also for any output voltage and can be used along with the VTC expression to compute the small signal gain as a function of the input voltage. More importantly, since the minimum and the maximum of second derivative of the voltage transfer function occur away from the switching voltage, a general small signal gain expression valid for any input voltage is needed to calculate the scaling factor or the conversion gain of the envelope detector.

The second derivative of the output voltage with respect to the input voltage gives rise to the scaling factor and the voltage conversion gain of the envelope detector (Sec. II-B). Analytical expressions for the scaling factor and the voltage conversion gain are derived in this article. The expressions are valid for any input voltage and can be evaluated along with the VTC expression and the general small signal expression to compute the scaling factor and the voltage conversion gain for an inverter-based envelope detector biased in the subthreshold region.

The close agreement between the simulated and the calculated of the second derivative of the voltage transfer characteristic curve shows that the voltage conversion gain for an inverter-based envelope detector biased in the subthreshold region is accurately modeled.

The article is organized as follows: Section II provides definitions, background, and preliminary simulation results for

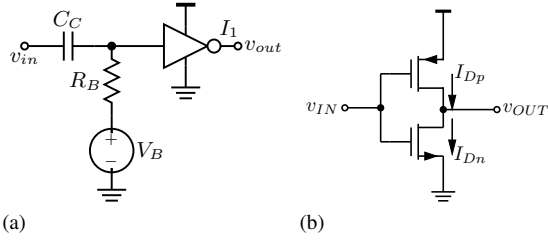


Fig. 1. (a) The simplified schematic of the inverter-based envelope detector. (b) Transistor-level implementation of the inverter cell.

understanding the operation of the inverter-based envelope detector in subthreshold region. Section III describes the derivation of expressions for voltage transfer characteristic, small signal gain, and scaling factor for the envelope detector. Section IV compares the simulated VTC, simulated small signal gain, and the simulated scaling factor with calculations using expressions derived in Sec. III. Conclusions are summarized in Sec. V

II. BACKGROUND

A. Distortion Characteristics of the Inverter Cell

Figure 1(a) is a simplified schematic of the inverter-based envelope detector. C_C is a coupling capacitor. R_B is implemented with an NMOS transistor biased in the subthreshold region. V_B is an adjustable DC voltage source discussed in [3]. Figure 1(b) shows the transistor level implementation of the inverter circuit.

B. Definitions

For weakly nonlinear CMOS inverters, the output voltage (v_{OUT}) can be approximated by the Taylor series expansion as

$$v_{OUT} = V_{OUT} + \frac{dV_{OUT}}{dV_{IN}} v_{in} + \frac{d^2 V_{OUT}}{dV_{IN}^2} \frac{v_{in}^2}{2}. \quad (1)$$

Let v_{in} be an amplitude modulated input,

$$v_{in} = v_m(1 + k_a m(t)) \cos \omega_c t. \quad (2)$$

v_m is the amplitude of the carrier wave and ω_c is the angular frequency of the carrier wave. k_a is the amplitude sensitivity of the modulator. For single tone modulation, $m(t) = A_m \cos \omega_m t$. The amplitude of baseband signal at the output of the inverter-based envelope detector is

$$v_{out,bb} = \frac{d^2 V_{OUT}}{dV_{IN}^2} \frac{v_m^2 \mu}{2}, \quad (3)$$

where μ is the modulation index and is equal to $k_a A_m$. For $\mu = 1$, the voltage conversion gain (G_V) of the inverter-based envelope detector is

$$G_V = \frac{v_{out,bb}}{v_m} = \frac{d^2 V_{OUT}}{dV_{IN}^2} \frac{v_m}{2} \quad (4)$$

and the scaling factor k of is

$$k = \frac{v_{out,bb}}{v_m^2} = \frac{d^2 V_{OUT}}{dV_{IN}^2} \frac{1}{2}. \quad (5)$$

G_V is dependent on v_m while k is independent of v_m .

C. Prior Work

Figure 2(a) shows the second derivative of V_{OUT} with respect to V_{IN} . The minimum of the second derivative occurs at just below V_S while the maximum of the second derivative occurs above V_S . Figure 2(a) suggests that k and G_V are higher with V_{DD} at 0.5 V. This observation is consistent with the observations reported in [3] which showed that k and G_V are maximized and the current consumption is reduced when the transistors operate in the subthreshold region. Figure 2(b) shows the sensitivity of the second derivative of V_{OUT} with respect to V_{IN} to process corners. [3] showed that by using a charge-scaling digital-analog converter circuit to adjust the gate bias voltage (V_B) in small increments, the circuit's sensitivity to process corners can be mitigated.

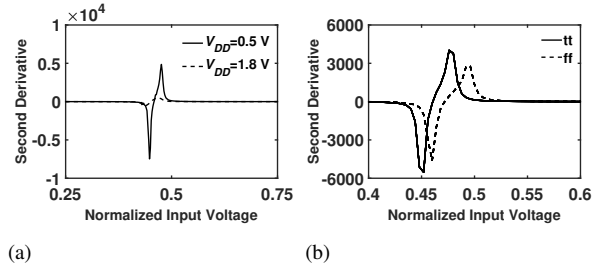


Fig. 2. (a) The second derivative as a function of the normalized V_{IN} and V_{DD} . (b) The second derivative of the voltage transfer function as a function of process corners and the normalized input voltage for V_{DD} of 0.5 V.

III. ANALYSIS OF AN INVERTER-BASED ENVELOPE DETECTOR

A. Transistor Model in Subthreshold Region

For NMOS transistors operating in the subthreshold region, the drain current is [8]

$$I_{Dn} = I_{on} e^{\frac{V_{GS} - V_{tn}}{n_n V_T}} (1 - e^{-\frac{V_{DS}}{V_T}}). \quad (6)$$

V_{GS} is the gate-to-source voltage. V_{DS} is the drain-to-source voltage. $V_T = kT/q$ is the thermal voltage. n_n is the subthreshold slope factor. I_{on} is a technology-dependent parameter

$$I_{on} = (n_n - 1) \frac{W_n}{L_n} \mu_n C_{ox} V_T^2, \quad (7)$$

where W_n/L_n is the aspect ratio, μ_n is the electron mobility, and C_{ox} is the oxide capacitance. V_{tn} is the threshold voltage and can be expressed as [8]

$$V_{tn} = V_{tn0} - \lambda_{DSn} V_{DS} - \lambda_{BSn} V_{BS} \quad (8)$$

V_{tn0} is the zero-bias threshold voltage (i.e., the value extracted under $V_{DS} = V_{BS} = 0$ V, whereas λ_{DSn} and λ_{BSn} are positive technology-dependent coefficients. V_{BS} is the body-to-source voltage.

Equation (6) can be used to model PMOS transistors in the subthreshold region by replacing V_{GS} with $|V_{GS}|$, V_{DS} with $|V_{DS}|$, I_{Dn} with $|I_{Dp}|$, n_n with n_p , V_{tn} with $|V_{tp}|$, I_{on} with I_{op} , and λ_{DSn} with λ_{DSp} .

B. Voltage Transfer Characteristic

The VTC of the inverter-based envelope detector in Fig. 1(b) can be obtained by setting I_{Dp} equal to I_{Dn} in Fig. 1(b), replacing V_{GS} and V_{DS} of the NMOS with V_{IN} and V_{OUT} , respectively, and replacing $|V_{GS}|$ and $|V_{DS}|$ of the PMOS with $V_{DD} - V_{IN}$ and $V_{DD} - V_{OUT}$. The VTC is

$$I_S e^{\frac{V_{IN}}{n_{eff} V_T}} = \frac{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}}, \quad (9)$$

where I_S and n_{eff} are

$$I_S = \frac{I_{on}}{I_{op}} e^{-\frac{V_{DD}}{n_p V_T} - \frac{V_{tn}}{n_n V_T} + \frac{|V_{tp}|}{n_p V_T}} \quad (10)$$

and

$$\frac{1}{n_{eff}} = \frac{1}{n_n} + \frac{1}{n_p} \quad (11)$$

The dependence of (9) on λ_{DSn} and λ_{DSP} can be explicitly expressed by 1) replacing V_{tn} (and V_{tp}) with (8) and 2) simplifying the resulting equation,

$$I_{So} e^{\frac{V_{IN}}{n_{eff} V_T}} = \frac{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}} e^{-(\frac{\lambda_{DSn}}{n_n} + \frac{\lambda_{DSP}}{n_p}) \frac{V_{OUT}}{V_T}}, \quad (12)$$

where

$$I_{So} = \frac{I_{on}}{I_{op}} e^{-\frac{V_{DD}}{n_p V_T}} e^{-(\frac{V_{tnp}}{n_n V_T} - \frac{|V_{tpo}|}{n_p V_T})} e^{-\frac{\lambda_{DSP} V_{DD}}{n_p V_T}}. \quad (13)$$

I_{So} is independent of V_{IN} and V_{OUT} but is a function of V_{DD} . In contrast to the VTC derived in [7], (12) accounts for the DIBL effect, yields a gradual descent near V_S and accurately captures A_V .

C. Small Signal Voltage Gain

A_V , the small signal voltage gain of the inverter-based envelope detector, is obtained by differentiating both sides of (12) with respect to V_{IN} , approximating n_n and n_p as n , and rearranging the resulting equation as

$$\frac{-1}{A_V} = \lambda_{DS} + \frac{n}{2} \frac{e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}} + \frac{n}{2} \frac{e^{-\frac{V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}}, \quad (14)$$

where $\lambda_{DS} = \frac{\lambda_{DSn} + \lambda_{DSP}}{2}$. In contrast to the small signal gain derived in [8], (14) is valid not only near V_S , but also for any V_{OUT} and can be used along with (12) to compute A_V as a function of V_{IN} . More importantly, since the minimum and the maximum of A_V occur away from V_S , (14) is needed to calculate the scaling factor of the envelope detector.

For $\lambda_{DSn} = \lambda_{DSP} = 0$, (14) is simplified to

$$\frac{-1}{A_V} = \frac{n}{2} \frac{e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}} + \frac{n}{2} \frac{e^{-\frac{V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}}. \quad (15)$$

D. Scaling Factor

As shown in (5), the scaling factor (k) is related to A'_V , the first derivative of A_V with respect to A_V as

$$k = \frac{1}{2} \frac{dA_V}{dV_{IN}} = \frac{A'_V}{2}. \quad (16)$$

A'_V can be obtained by 1) differentiating both sides of (14) with respect to V_{IN} and 2) simplifying the resulting equation as

$$A'_V = \frac{A_V^3}{V_T} \frac{n}{2} (\alpha - \beta), \quad (17)$$

where α is

$$\alpha = \frac{e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}} \left(1 + \frac{e^{-\frac{V_{DD} - V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{DD} - V_{OUT}}{V_T}}} \right), \quad (18)$$

and β is

$$\beta = \frac{e^{-\frac{V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}} \left(1 + \frac{e^{-\frac{V_{OUT}}{V_T}}}{1 - e^{-\frac{V_{OUT}}{V_T}}} \right). \quad (19)$$

k , the scaling factor is

$$k = \frac{A_V^3}{V_T} \frac{n}{4} (\alpha - \beta). \quad (20)$$

The dependence of k on λ_{DS} is captured in (17) through A_V . G_V , the voltage conversion gain is a function of v_{in} and is

$$G_V = \frac{A_V^3}{V_T} \frac{n}{4} (\alpha - \beta) v_m. \quad (21)$$

IV. RESULTS

A. Transistor Parameters

Table I summarizes the transistor parameters used to generate characteristic curves for the VTC, the small signal gain, and the scaling factor of the inverter-based envelope detector.

TABLE I
180-NM TRANSISTOR PARAMETERS.

Device	n	I_o [μ A]	V_t^1 [mV]	λ_{DS}
NMOS ²	1.364	29.9	548.8	0.033
PMOS ²	1.427	15.6	571.0	0.026

¹ V_t is extrapolated for $V_{DS} = V_{BS} = 0$ V.

² The W/L ratios for the NMOS and the PMOS transistors are 1.0/0.18 μ m/ μ m and 1.37/0.18 μ m/ μ m, respectively.

B. Voltage Transfer Characteristic

Figure 3 shows the simulated VTC and the calculated VTC. The VTC was simulated at the transistor-level using the BSIM4 model using Cadence Spectre. The calculated VTC was obtained by solving (12) using `fzero` in Matlab using transistor parameters from Table I. Since $n_n \approx n_p$, n_n and n_p are averaged. An averaged n of 1.396 is used in the calculation.

The simulated V_S is 227 mV and the calculated V_S is 230 mV. The close agreement between the simulated and the calculated VTC suggests that in contrast to the VTC derived in [7], (12) accounts for the DIBL effect, yields a gradual descent near V_S , and accurately captures A_V .

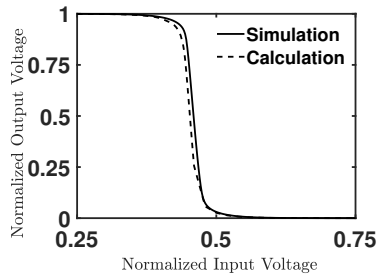


Fig. 3. Simulated and calculated VTC of an inverter cell. The input and output voltage are normalized to V_{DD} of 0.5 V.

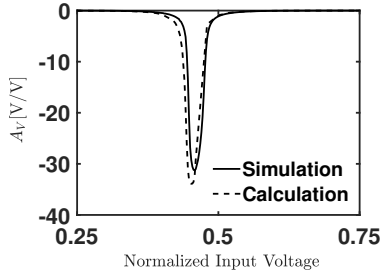


Fig. 4. The small signal voltage gain. The input voltage is normalized to V_{DD} of 0.5 V.

C. Small Signal Voltage Gain

Figure 4 shows the simulated A_V and the calculated A_V . The calculated A_V was obtained by solving (14) with V_{OUT} from (12). The minimum of the simulated A_V is -32.36 V/V and occurs at the normalized input voltage of 0.458. The minimum of the calculated A_V is -33.86 V/V and occurs at the normalized voltage of 0.454. V_{DD} is 0.5 V. The close agreement between the simulated and the calculated A_V shows that in contrast to the small signal gain derived in [8], the expression derived in this article is accurate not only near the switching voltage, but also for any input voltage. More importantly, since the minimum and the maximum of second derivative of the voltage transfer function occur away from the switching voltage, a general small signal gain expression valid for any input voltage is needed to calculate the scaling factor of the envelope detector.

D. Scaling Factor

Figure 5 shows the simulated and the calculated A'_V , the second derivative of the voltage transfer characteristic curve with respect to the input voltage. Since A'_V is equal to $2k$, where k is the scaling factor, A'_V is an indirect measure of k .

The calculated A'_V was obtained using (17). A close analysis of Fig. 5 shows that the minimum of calculated A'_V is $-6,767$ 1/V while that of the simulated A'_V is $-7,476$ 1/V. The percentage error of the minimum A'_V is -9.5% . The maximum of calculated A'_V of $4,779$ 1/V occurs at 3.0 mV above V_S while that of the simulated A'_V of $4,856$ 1/V occurs at 8.0 mV above V_S . The percentage error of the minimum A'_V is -1.6% . The close agreement between the simulated and the calculated

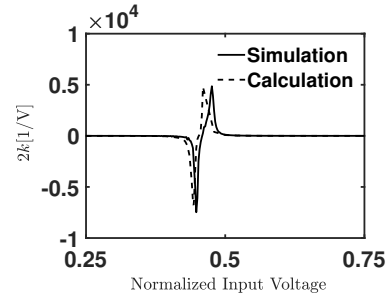


Fig. 5. A'_V , the second derivative of the voltage transfer characteristic curve with respect to the input voltage. A'_V is equal to $2k$, where k is the scaling factor.

A'_V shows that the voltage conversion gain for an inverter-based envelope detector biased in the subthreshold region is accurately modeled using (17).

V. CONCLUSION

This paper derives the formulas for the VTC, the small signal gain, and the scaling factor of the inverter-based envelope detector in the subthreshold region. The VTC expression produces a gradual descent near the switching voltage and accurately models the small signal gain. The small signal gain expression valid for any input voltage is needed to calculate the scaling factor or the conversion gain of the envelope detector. The close agreement between the simulated and the calculated results shows that the subthreshold inverter-based envelope detector is accurately modeled.

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