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Charge Transport Across Au–P3HT–Graphene van der Waals Vertical Heterostructures

Jacopo Oswald, Davide Beretta,* Michael Stiefel, Roman Furrer, Alessia Romio, Michel Daher Mansour, Dominique Vuillaume, and Michel Calame*



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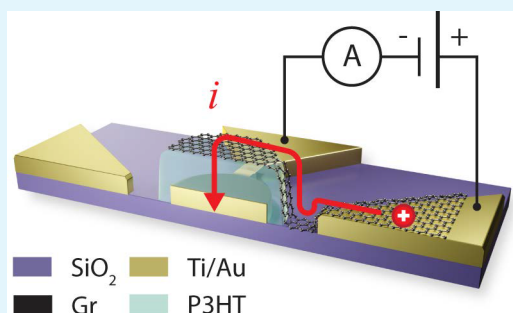


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Supporting Information

ABSTRACT: Hybrid van der Waals heterostructures based on 2D materials and/or organic thin films are being evaluated as potential functional devices for a variety of applications. In this context, the graphene/organic semiconductor (Gr/OSC) heterostructure could represent the core element to build future vertical organic transistors based on two back-to-back Gr/OSC diodes sharing a common graphene sheet, which functions as the base electrode. However, the assessment of the Gr/OSC potential still requires a deeper understanding of the charge carrier transport across the interface as well as the development of wafer-scale fabrication methods. This work investigates the charge injection and transport across Au/OSC/Gr vertical heterostructures, focusing on poly(3-hexylthiophen-2,5-diyl) as the OSC, where the PMMA-free graphene layer functions as the top electrode. The structures are fabricated using a combination of processes widely exploited in semiconductor manufacturing and therefore are suited for industrial upscaling. Temperature-dependent current–voltage measurements and impedance spectroscopy show that the charge transport across both device interfaces is injection-limited by thermionic emission at high bias, while it is space charge limited at low bias, and that the P3HT can be assumed fully depleted in the high bias regime. From the space charge limited model, the out-of-plane charge carrier mobility in P3HT is found to be equal to $\mu \approx 2.8 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, similar to the in-plane mobility reported in previous works, while the charge carrier density is $N_0 \approx 1.16 \times 10^{15} \text{ cm}^{-3}$, also in agreement with previously reported values. From the thermionic emission model, the energy barriers at the Gr/P3HT and Au/P3HT interfaces result in 0.30 eV and 0.25 eV, respectively. Based on the measured barriers heights, the energy band diagram of the vertical heterostructure is proposed under the hypothesis that P3HT is fully depleted.



KEYWORDS: organic, semiconductor, graphene, interface, transport, vertical, van der Waals

INTRODUCTION

Hybrid van der Waals heterostructures based on 2D materials and/or organic thin films are being extensively studied^{1–3} for a variety of applications encompassing field effect transistors, organic solar cells,^{4–6} photodetectors,^{7,8} vertical transistors,^{9–14} and light emitting diodes.^{15,16} Despite solid progress, developing a better understanding of the electron transport across hybrid van der Waals interfaces remains crucial to better control functionality and enhance performance. In this context, graphene is an excellent candidate as 2D electrode to contact organic thin films due to its inherent ability to form π – π stacking and van der Waals bonds.¹⁷ Many studies to date aimed at unraveling the physical mechanisms behind charge injection at Gr/OSC interfaces for applications in diverse fields of micro- and nanoelectronics:^{18–20} typically, graphene is used as the bottom electrode in barristors^{9–14} or transferred on top of an OSC film together with a protecting polymer, e.g., PMMA. However, other more complex multilayer designs could benefit from graphene full potential as monatomic thick, semitransparent, flexible and surface-conformal electrode. For

instance, graphene could replace the base in vertical transistors, enabling organic transistors with nanoscale channels and higher operation frequencies that could meet the requirements of high-frequency applications, or function as interlayer electrode in OLEDs.^{21–24} In this framework, the development of large-scale photolithographic fabrication methods compatible with hybrid architectures that exploit graphene as the top or interlayer electrode, and the understanding and modeling of the charge transport in the latter is crucial for the design and optimization of novel functional devices.

For this study, the authors developed a fabrication process for Au/P3HT/Gr hybrid VdW heterostructures, where PMMA-free graphene lies on top of a p-type OSC and

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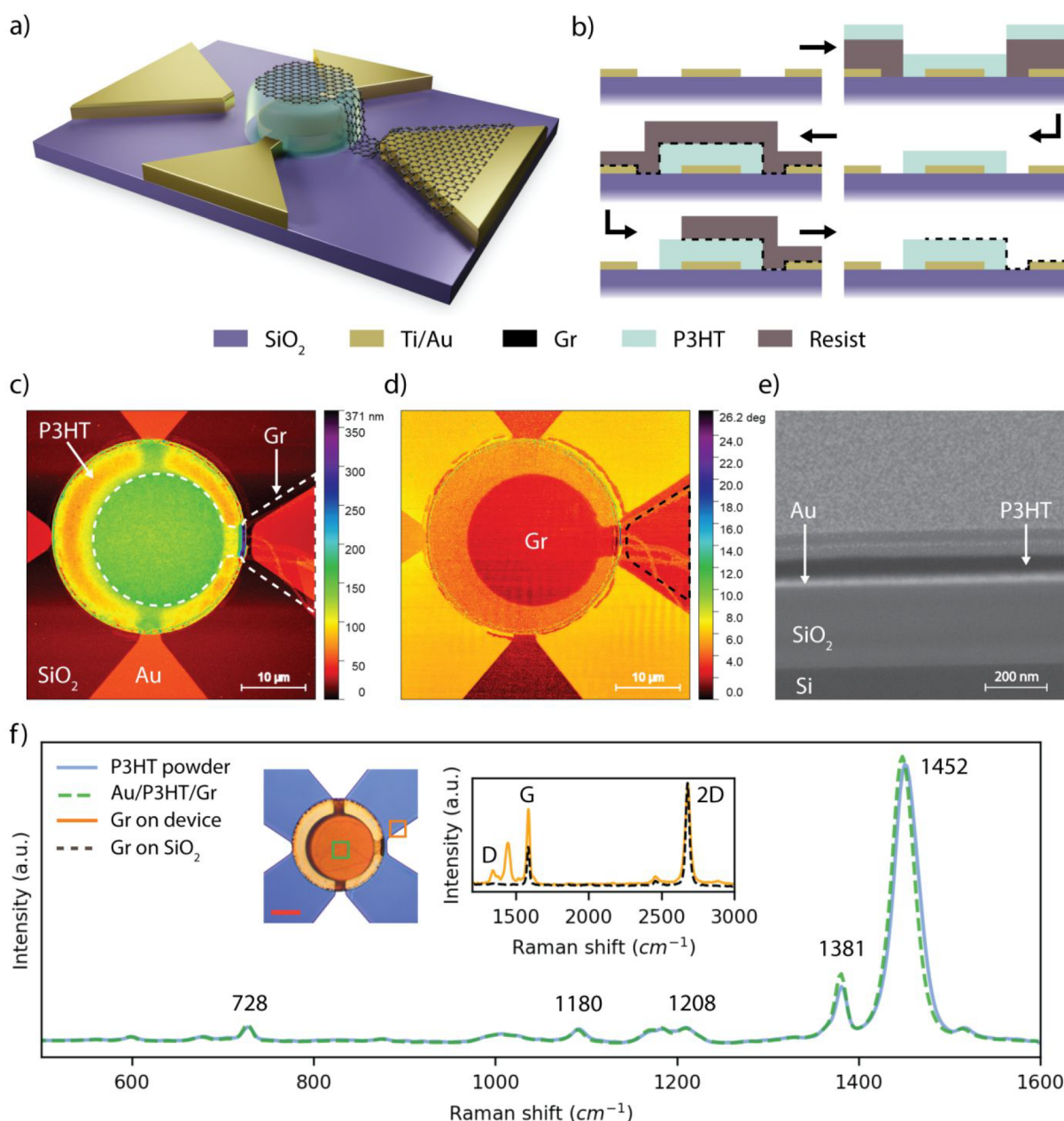


Figure 1. (a) 3D schematic of a representative Au/P3HT/Gr heterostructure (not to scale). (b) Schematic of the fabrication process. AFM (c) height and (d) phase images of a representative $20\ \mu\text{m}$ device. (e) SEM of a FIB cut cross-section of a representative Au/P3HT/Gr heterostructure in the center of the device. (f) Raman spectra of P3HT powder (blue line) and of a representative Au/P3HT/Gr device (dashed green line). The optical image shows the acquisition position of the spectra (the red scale bar is $10\ \mu\text{m}$). The inset shows the Raman spectra of a device graphene against the Raman spectrum of a representative CVD graphene on SiO_2 .

functions as the top electrode for the vertical stack, and investigated and modeled the charge injection across the two interfaces, i.e., Au/P3HT and P3HT/Gr, by temperature-dependent I - V measurements, impedance spectroscopy, and Kelvin probe force microscopy (KPFM). The charge transport across the device was found to be described by the thermionic emission (TE) assisted by image-charge induced barrier lowering model in the high voltage regime ($|V| > 1\ \text{V}$) and by the space-charge limited (SCL) current model in the low voltage regime ($|V| < 1\ \text{V}$). The models allowed us to extract the charge carrier concentration and the out-of-plane mobility of P3HT, and the reduced effective Richardson constant of and the potential barrier height at the two interfaces, ultimately

making it possible to sketch the energy band diagram of the whole stack.

EXPERIMENTAL METHODS

Materials. Poly(3-hexylthiophene-2,5-diyl) (Regio-Regular (RR) $> 99\%$, $M_n = 27\ 000$ – $45\ 000$) was purchased from Tokyo Chemicals and used as received to prepare solutions of $10\ \text{mg/mL}$ in chlorobenzene. Graphene was grown in-house by chemical vapor deposition (CVD) on copper foils with a fully automated setup. The graphene growth protocol can be found in previously reported works.^{25–27}

Fabrication. The study was conducted on a single chip including two different sets of devices: (i) Au/P3HT/Gr vertical stacks (119 devices) and (ii) graphene bridges (34 devices) (refer to Figure 1a

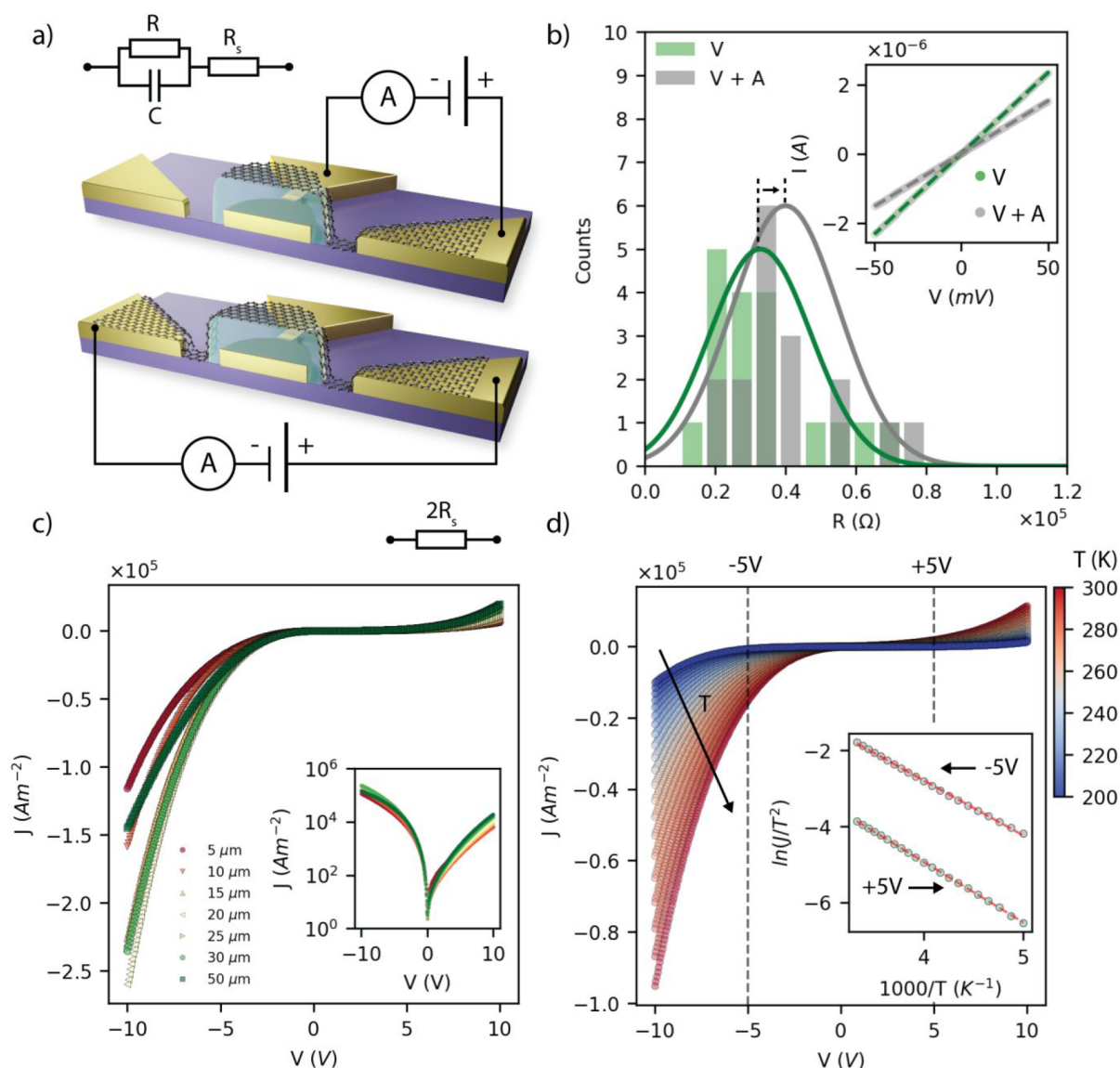


Figure 2. (a) Device schematics and electrical schemes of the Au/P3HT/Gr stack and of the graphene bridge devices. R_s is the graphene series resistance, R is the out-of-plane resistance, and C is the geometrical capacitance of the device. (b) Distribution of R_s in vacuum and in vacuum after annealing (17 samples). The inset shows two representative $I-V$ traces of side-contacted graphene. The resistance is calculated from the linear fit (dashed lines). (c) Current density of representative devices with diameter 5, 10, 15, 20, 25, 30, and 50 μm . The inset shows the same traces on log scale. (d) Temperature-dependent $J-V$ characteristic of a 5 μm device from 200 to 300 K in steps of 5 K. The inset shows the Richardson plot for 5 V and -5 V.

and 2a for a schematic of the devices architecture). The chip was fabricated on a Si(525 μm)/SiO₂(300 nm) substrate at the Binnig and Rohrer Nanotechnology Center (BRNC) and EMPA. In both architectures, P3HT is sandwiched between a gold (bottom) and a graphene (top) circular electrode. In the bridge architecture, graphene is side-contacted so that one can force a current through it to evaluate its resistance independently from the underlying P3HT film (see Figure 2a for the electrical scheme). The chip includes devices having various nominal diameters, i.e. 5, 10, 15, 20, 25, 30, and 50 μm . The bottom gold electrodes are 2 μm larger than the top graphene electrodes. The fabrication was done by photolithography under ambient conditions, as illustrated in Figure 1b and thoroughly described in the Supporting Information. Briefly, Au electrodes were deposited by e-beam physical vapor deposition (EBPVD) and patterned by lift-off. P3HT was then spin-coated at 1000 rpm for 60 s and patterned by lift-off. Finally, the CVD graphene top electrode was wet transferred and patterned by reactive ion etching (RIE).

Electrical Characterization. The electrical characterization at room temperature was done in the dark, in air, under vacuum ($\sim 1 \times 10^{-6}$ mbar), using a Keithley 236 source-measure unit controlled via Python. The voltage was swept in the range from -10 V to $+10$ V in steps of 50 mV, with sweep rate of ca. 100 mV/s and internal averaging of 20 ms, keeping the bottom Au electrode on ground. The graphene resistance was characterized in graphene bridge devices by sweeping the voltage in the range from -50 mV to $+50$ mV in steps of 1 mV, with a sweep rate of ca. 3 mV/s and internal averaging of 20 ms.

The temperature-dependent $I-V$ traces were collected in the range 200–300 K in steps of 5 K in a Lakeshore probe station (CRX-6.5K) operating under vacuum ($\sim 1 \times 10^{-6}$ mbar), in the dark. The electronics comprised an AdWin Gold II ADC-DAC unit operating at 100 kHz and a low-noise current to voltage converter (Basel SP983C). The ADC-DAC was controlled via Python. The voltage was swept in the range from -10 V to $+10$ V in steps of 0.1 V, with internal averaging of 20 ms and a delay between the source and

measurement point of 100 ms, corresponding to an effective voltage sweep rate of ca. 0.8 V/s.

Impedance spectroscopy was carried out on one representative device per area using an Agilent 4294a precision impedance analyzer controlled via *Python*, from 40 Hz to 1 MHz in 201 steps, in the dark, under a vacuum ($\sim 1 \times 10^{-6}$ mbar), with the oscillator level set to 100 mV. Open/short compensation was performed after the acquisition and following the *Agilent Impedance Measurement Handbook*.²⁸ To this purpose, we designed and fabricated devices for open/short compensation on the same chip.

KPFM measurements were carried out at room temperature in air (22 °C and 35% relative humidity) with a Dimension 3100 (Bruker), using a Pt/Ir tip. Topography (tapping mode AFM) and KPFM images were recorded using a standard two-pass procedure, in which each topography line acquired in the tapping mode is followed by the acquisition of CPD (contact potential difference between the tip and the sample) data in a lift mode. Since the CPD images on Au, Gr, and P3HT are acquired with the same tip, the interface barrier energy is directly given by the difference in the CPD values, i.e., $\Phi_{B,Gr/P3HT} = q(\text{CPD}_{Gr} - \text{CPD}_{P3HT})$, where q is the electron charge.

Raman Spectroscopy. Raman spectra were acquired in ambient conditions using a 532 nm excitation wavelength with a WITec Alpha 300R confocal Raman microscope mounting a LD 100 \times objective (Zeiss EC Epiplan-Neofluar Dic, NA = 0.75) and a 300 mm lens-based spectrometer (grating: 600 g mm⁻¹) equipped with a TE-cooled charge-coupled device (Andor Newton). P3HT powder and films spectra were acquired by averaging over a $5 \times 5 \mu\text{m}^2$ area with a laser power and an integration time of 0.1 mW and 0.1 s, while graphene spectra were acquired with a laser power and an integration time of 1 mW and 10 s.

Atomic Force Microscopy (AFM). AFM height and phase images were collected in tapping mode in ambient conditions using a Bruker Icon AFM equipped with a TESPA-V2 cantilever with a tip apex radius of 7 nm (resonant frequency: 320 kHz, spring constant 37 N/m).

FIB-SEM. The device cross-section was prepared by means of a FEI Helios 660 G3 UC FIB/SEM-System. Prior to cutting, a protective layer of platinum was deposited in a two-step process, first by electron-induced deposition (3 keV, 800 pA), followed by ion-induced deposition (30 keV, 230 pA) in order to prevent ion induced damage to the layers of interest. The cross-section was cut in a 30 kV gallium ion beam at an ion current of 47 nA. The cross-section was sequentially polished at different ion currents, down to a minimal current of 790 pA.

Modeling, Fitting, and Plotting. Modeling, fitting, and plotting of the data were done in *Python*. Three main libraries were used (i) *numpy polyfit*,²⁹ for the estimation of graphene series resistance; (ii) *scipy curve_fit*,³⁰ for the SCL and TE modeling; and (iii) *impedance.py*,³¹ for the circuit modeling and fitting of the impedance analysis measurements.

RESULTS AND DISCUSSION

Figure 1a shows the schematic of a Au/P3HT/Gr heterostructure, fabricated according to the procedure illustrated in Figure 1b and described in the *Experimental Methods* and in the *Supporting Information*. Figures 1c,d show the AFM height and phase images of a representative device having a diameter of 20 μm , where a white dashed line marks the contour of the graphene and a black dashed line marks the Au side-electrode. The thickness of the Au/P3HT/Gr stack in the center of the device is ca. 130 nm as measured by AFM (see the *Supporting Information*). Given that the bottom Ti/Au electrode is 35 nm thick, the thickness of the P3HT film is ca. 100 nm. Figure 1e shows a cross-section of the Au/P3HT/Gr stack in the center of the device. Starting from the bottom, one can distinguish Si (525 μm), SiO₂ (300 nm), Ti (5 nm), Au (30 nm), and P3HT (100 nm) as annotated in the figure. The graphene electrode is too thin to be visible in the cross-section.

Figure 1f superimpose the Raman spectrum of the P3HT powder as received, with the Raman spectrum of the Au/P3HT/Gr stack. The vibrational modes of P3HT are found at 728, 1180, 1208, 1381, and 1452 cm⁻¹, in agreement with the literature.^{32,33} The vibrational modes of graphene are not discernible from P3HT for three reasons: (i) the G and D peaks of graphene are hidden by the overlapping modes of P3HT at 1381 and 1452 cm⁻¹, (ii) the 2D peak is hidden by the strong background signal of P3HT, and (iii) the P3HT is much thicker than graphene, therefore resulting in a much stronger spectral signal. Therefore, the Raman spectrum of graphene was measured on SiO₂, in close proximity to the Au contact. The graphene Raman spectrum is shown in the inset of Figure 1f against the Raman spectrum of a representative CVD graphene on SiO₂. The characteristic G (1580 cm⁻¹) and 2D (2680 cm⁻¹) peaks of graphene³⁴ are identified, as well as the D (1350 cm⁻¹) peak, possibly due to defects induced by the fabrication, and an additional peak at 1445 cm⁻¹, most likely due to P3HT or resist residues. The AFM, SEM, and Raman data demonstrate that the fabrication process is compatible with P3HT and graphene and therefore suitable for the fabrication of vertical van der Waals devices based on these materials.

The electrical properties of OSCs are very sensitive to the environment. Figure S3 shows the J - V traces of a representative 10 μm device measured in ambient, in vacuum and in vacuum after annealing at 110 °C for 12 h. The current density is higher in ambient and it decreases in vacuum, reaching a minimum after annealing, with peak current density at -10 V going from $5.4 \times 10^5 \text{ A m}^{-2}$ to $1.5 \times 10^5 \text{ A m}^{-2}$. The traces are asymmetric: defining the rectification ratio as $\text{RR} = J(-10\text{V})/J(10\text{V})$, the latter increases from $\text{RR} = 1.9$ in ambient, to $\text{RR} = 2.6$ in a vacuum, and finally to $\text{RR} = 19.2$ in a vacuum after annealing. This trend is ascribed to the graphene and P3HT dedoping: it is known that P3HT is doped by O₂,³⁵ while graphene is doped by O₂ and H₂O,³⁶⁻³⁸ and that their doping level can be reduced by annealing under a vacuum.^{39,40} Accordingly, an annealing under vacuum shifts the Fermi level of graphene, resulting in a realignment of the energy bands at the OSC/graphene interface, which leads to the observed change in the rectification ratio. The hypothesis is further supported by the graphene resistance shown in Figure 2b: the graphene/Au interface is Ohmic and the graphene resistance increases after vacuum exposure and annealing.

In order to minimize the variability among different devices due to uncontrolled doping of P3HT and graphene, the charge transport analysis that follows was done in a vacuum after annealing for 12 h at 110 °C. Figure 2c shows the current density of five representative devices, one per device area, measured in a vacuum after annealing (see the *Supporting Information* for the J - V s of all devices). The current density is calculated assuming the area of the (smaller) graphene electrode ($J = I/A_{Gr}$). The current density variability falls within ca. one order of magnitude (between 7.3×10^4 and 2.6×10^5 at -10 V, and between 3.1×10^3 and 2.3×10^4 at +10 V) and all J - V s display the same shape. This suggests that the scaling of the device, from 50 μm down to 5 μm in diameter, does not affect the transport mechanism, and that the variability between devices is due to fabrication uncertainties. In all measurements conditions, and for both positive and negative bias, the current density grows exponentially with the applied voltage above a certain threshold. This trend is typically described by a variety of analytical models that allows

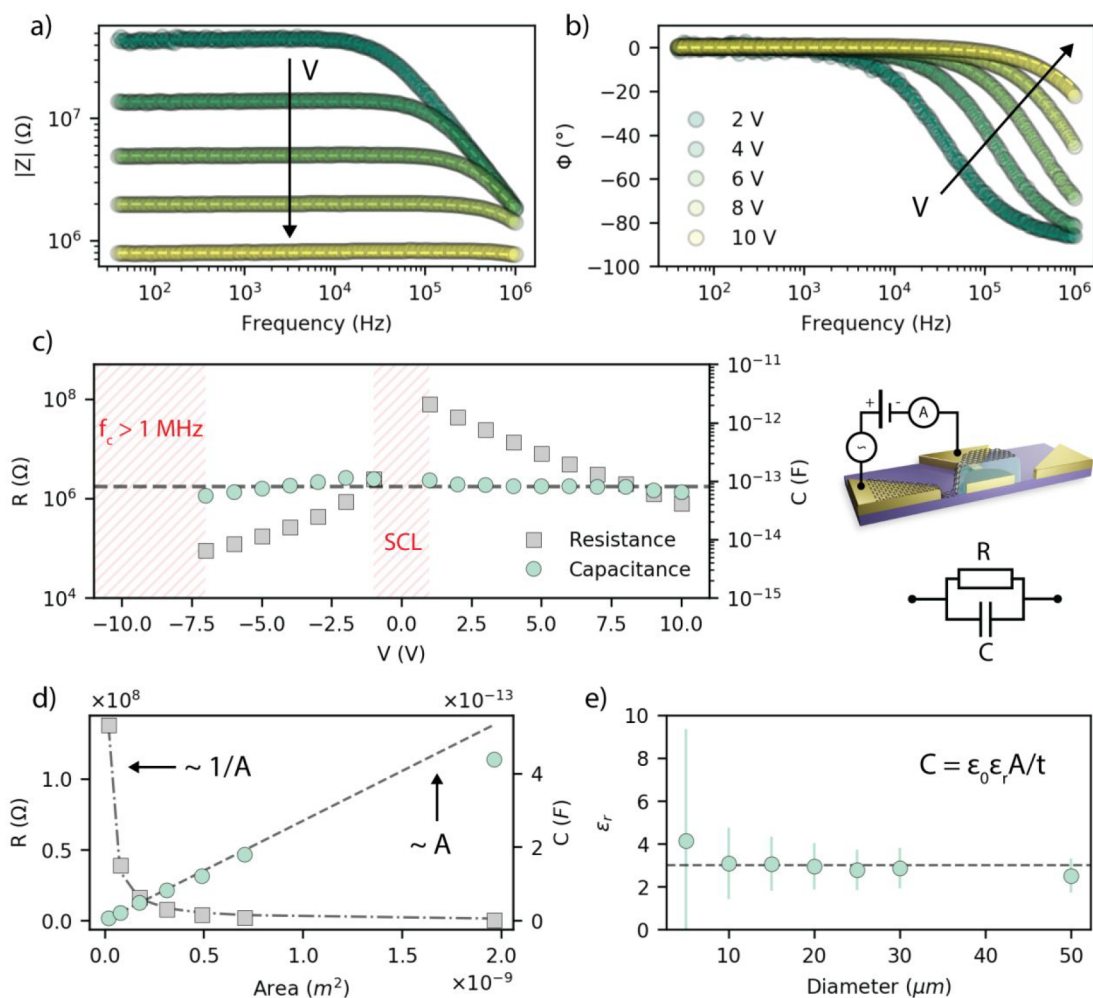


Figure 3. Impedance analysis. (a) Modulus and (b) phase of a representative $20 \mu m$ device: data (circles), R||C model fit (dashed lines) (c) Resistance R and capacitance C extracted from the R||C model fit at different biases. R and C are not calculated in the SCL region and for $V < -7.5$ V, where the cutoff frequency f_c is outside the measurement range. (d) Extracted R and C values for the devices with diameter: 5, 10, 15, 20, 25, 30, and $50 \mu m$. The green dashed line is the linear fit of the capacitance vs area. (e) ϵ_r vs device diameter (error bars calculated as described in the Supporting Information).

us to extract transport parameters (e.g., charge carrier mobility and density and the energy barriers at the interfaces). Among these models are the thermionic emission (TE) assisted by image-charge-induced potential barrier lowering,⁴¹ the Poole–Frenkel emission (PFE),⁴¹ and the modified TE (MTE) for graphene/semiconductor interfaces.^{42,43} The fittings of the J – V s with the PFE model (not reported) were found to return relative dielectric permittivity of P3HT around 20–40, i.e., about 1 order of magnitude larger than what discussed in the literature.^{44–46} Therefore, the PFE model was excluded from the analysis. The hypothesis of the MTE model requires that the charge at the graphene/semiconductor interface depends on the bias. However, the capacitance measurements discussed in the following show that the organic semiconductor is fully depleted. Hence, the charge at the interface is bias independent and therefore the MTE model was not considered for the analysis that follows. The TE model has been successfully applied to metal–OSC interfaces^{47–50} and was found to be in good agreement also with the measurements of this work in the high voltage regime, that is $|V| > 1$ V. According to the TE model, the J – V traces shown in Figure 2c are the reverse currents of the Au/P3HT and Gr/P3HT interfaces for

negative and positive bias, respectively. The reverse current reads:⁴¹

$$J_R^{(TE)} = A^{**} T^2 \exp \left[\frac{-q(\phi_B - \sqrt{qV'/4\pi\epsilon_0\epsilon_r t})}{k_B T} \right] \quad (1)$$

Where A^{**} is the reduced effective Richardson constant, T is the temperature, q is the elementary charge, ϕ_B is the barrier height potential, ϵ_0 is the vacuum permittivity, ϵ_r is the P3HT dielectric permittivity, k_B is the Boltzmann constant, t is the thickness of the device, and $V' = V - R_s I$ is the applied voltage V minus the voltage that drops over the graphene (series) resistance R_s . The $R_s I$ term becomes relevant when the out-of-plane resistance of Au/P3HT/Gr is comparable to R_s , which typically happens for $V < -5$ V and device diameter larger than $10 \mu m$ (see Figure S7).

At lower bias voltage, the J – V traces do not agree anymore with the TE model, but they show the typical trap-free space-charge limited (SCL)^{41,51,52} dependency where, on the one hand, if the charge carrier density at the contact N_0 is larger

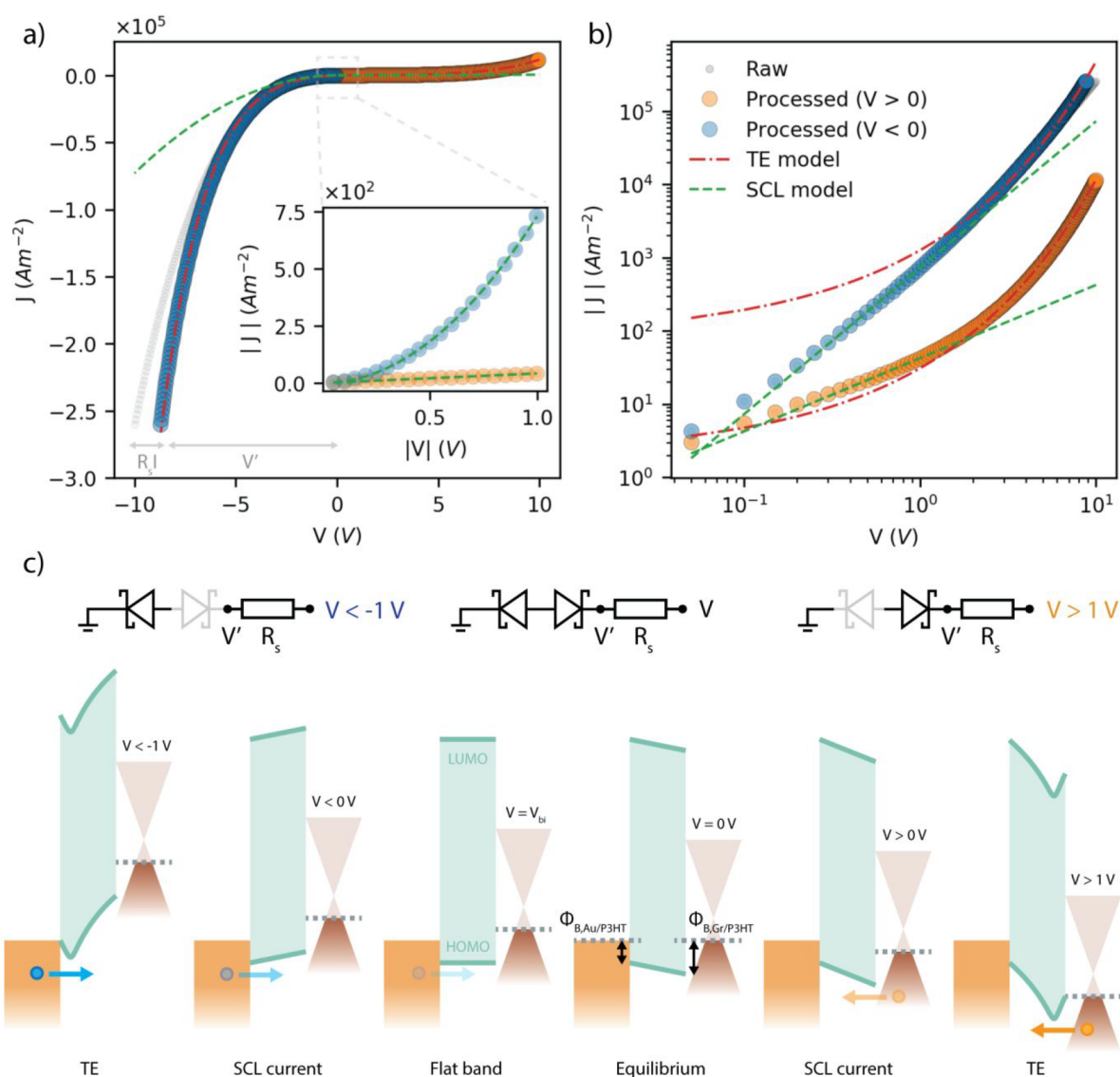


Figure 4. (a) Current density across a 20 μm device. Raw data are represented by gray circles. Processed data (orange and blue circles) takes into account for the graphene series resistance. The graph shows the fitting results of the SCL current (green dashed lines) and TE (red dashed lines). The inset shows the ± 1 V region where the space-charge effect is limiting the current across the heterostructure. (b) Current density shown in logarithmic scale. The current density for positive and negative biases is represented by orange and blue circles, respectively. (c) Band diagram of the Au/P3HT/Gr heterojunction illustrating the charge transport regimes and equivalent circuit. The shaded Schottky diodes are forward biased.

than $\sqrt{\frac{J_0 \epsilon_r}{2 \mu q^2}}$, where μ is the charge carrier mobility of the organic semiconductor, then

$$J = \frac{9}{8} \epsilon_0 \epsilon_r \mu \frac{V^2}{t^3} \quad (2)$$

and on the other hand, if N_0 is smaller than $\sqrt{\frac{J_0 \epsilon_r}{2 \mu q^2}}$ then

$$J = q \mu N_0 \frac{V}{t} \quad (3)$$

From eqs 1–3, one can extract the barrier height ϕ_B , the mobility μ , and the charge carrier density at the interfaces, provided knowledge of ϵ_r and A^{**} . The effective Richardson constant A^{**} can be obtained from temperature-dependent measurements through the Richardson plot ($\ln(J/T^2)$ vs $1/T$), while the dielectric permittivity ϵ_r can be either taken from the literature or extracted from capacitive measurements under the

hypothesis of a fully depleted semiconductor. Since the extraction of the barrier height is sensitive to ϵ_r and the latter depends on the measurement environment, it is beneficial to measure the dielectric permittivity of P3HT on the system under study, if possible. Given that the charge carrier density of unintentionally doped organic P3HT films is typically in the range of 1×10^{17} to $1 \times 10^{18} \text{ cm}^{-3}$,^{35,40} and that the doping concentration is usually reduced to roughly $1 \times 10^{15} \text{ cm}^{-3}$ by annealing in a vacuum,^{40,53} the P3HT can be safely assumed fully depleted and therefore ϵ_r extracted from impedance spectroscopy. This hypothesis can be assessed by measuring the capacitance of the heterostructure as a function of the applied bias: if the capacitance does not depend on the bias, then the depletion region extends over the entire thickness of the device.

A^{**} was extracted from the Richardson plot of a representative device having diameter of 5 μm at bias ± 5 V, such that the graphene series resistance R_s was negligible

Table 1. Statistics of the Fitting Parameters^a

diameter (μm)	P3HT thickness (nm)	space-charge model ($ V < 1\text{ V}$)		thermionic emission model ($ V > 1\text{ V}$)		
		N_0 ($\times 10^{15}\text{ cm}^{-3}$)	μ ($\times 10^{-4}\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$)	R_s (k Ω)	$\Phi_{\text{B,Gr/P3HT}}$ (eV)	$\Phi_{\text{B,Au/P3HT}}$ (eV)
5	130	0.94 ± 0.40	4.36 ± 0.61	35 (fixed)	0.30 ± 0.02	0.25 ± 0.01
10	120	1.14 ± 0.12	3.72 ± 0.92	35 (fixed)	0.29 ± 0.01	0.25 ± 0.01
15	100	1.11 ± 0.26	2.26 ± 0.21	42.0 ± 7.9	0.31 ± 0.01	0.26 ± 0.01
20	100	1.13 ± 0.26	2.37 ± 0.09	19.1 ± 10.9	0.31 ± 0.01	0.25 ± 0.01
25	100	1.44 ± 0.37	2.41 ± 0.21	24.6 ± 16.5	0.30 ± 0.01	0.25 ± 0.01
30	100	1.16 ± 0.26	2.13 ± 0.08	12.7 ± 6.4	0.30 ± 0.01	0.25 ± 0.01
50	100	1.20 ± 0.14	2.32 ± 0.09	11.2 ± 12.8	0.29 ± 0.01	0.25 ± 0.01
all	100	1.16 ± 0.65	2.80 ± 2.17	25.6 ± 24.3	0.30 ± 0.02	0.25 ± 0.02

^aThe average on five devices is given for N_0 , μ , R_s , and Φ . The reported error is the min/max value. All SCL and TE model fits were done using $\epsilon_r \approx 3$, $A_{\text{Gr/P3HT}}^{**} = 4.3\text{ A m}^{-2}\text{ K}^{-2}$ and $A_{\text{Au/P3HT}}^{**} = 20.5\text{ A m}^{-2}\text{ K}^{-2}$. The series resistance of the $5\text{ }\mu\text{m}$ and $10\text{ }\mu\text{m}$ devices is very small compared to the device out-of-plane resistance. In order to prevent the fitting algorithm to maximize R_s , the latter was set to $35\text{ k}\Omega$ for $5\text{ }\mu\text{m}$ and $10\text{ }\mu\text{m}$ devices. Figure S5 shows the current density and the fits of various devices.

compared to the out-of-plane resistance of the stack and therefore $V' (\pm 5\text{ V}) = V (\pm 5\text{ V})$. Figure 2d shows the J - V characteristics as a function of temperature, from 200 to 300 K in steps of 5 K. The current density increases with temperature, peaking at -10 V from $1 \times 10^4\text{ A m}^{-2}$ (200 K) to $9.5 \times 10^4\text{ A m}^{-2}$, (300 K) while the J - V s exhibit the typical exponential character of the TE model over the whole temperature range. The inset of Figure 2d shows the Richardson plot for bias $+5\text{ V}$ (hole injection from Gr) and bias -5 V (hole injection from Au). From the intercept of the linear fit, the reduced effective Richardson constants results in $A_{\text{Gr/P3HT}}^{**} = 4.3\text{ A m}^{-2}\text{ K}^{-2}$ for hole injection from Gr and $A_{\text{Au/P3HT}}^{**} = 20.5\text{ A m}^{-2}\text{ K}^{-2}$ for hole injection from Au, similar to the values previously reported for metal/OSC^{47,48} and Gr/OSC⁴³ interfaces. It is worth observing that A^{**} could be extracted from the Richardson plot in the whole voltage range where the J - V is exponential and R_s is negligible. However, Figure S8 shows that (i) A^{**} does not vary significantly in that voltage range and (ii) the potential barrier heights extracted from the fittings do not depend significantly on the particular choice of A^{**} . Therefore, the chosen values of A^{**} did not affect the results of this work.

The dielectric permittivity ϵ_r was extracted from the impedance spectroscopy on a representative device per device area. Figure 4a, b shows the impedance of a representative device having a diameter of $20\text{ }\mu\text{m}$, in the frequency range of 40 Hz to 1 MHz, for positive bias (refer to the Supporting Information for the impedance for negative biases). The impedance exhibits the typical behavior of an R||C circuit. The resistance R and the capacitance C of the system are therefore extracted by fitting the experimental data with a nonideal capacitor model R||C, and are reported in Figure 3c. The high negative voltage range corresponding to $V < -7\text{ V}$ was not fitted because the cutoff frequency of the system is beyond 1 MHz (upper limit of the measurement range). The low voltage region ($|V| < 1\text{ V}$) was also not considered because the space-charge would result in a capacitance 3 / 2 larger than the geometrical one.⁵² The resistance decreases with the applied bias, from $80.7\text{ M}\Omega$ at 1 V to $791\text{ k}\Omega$ at 10 V , possibly due to the image-charge-induced potential barrier lowering, while the capacitance is bias-independent around 80 fF , confirming that the organic semiconductor is fully depleted.⁵⁴ The dielectric constant of P3HT is estimated from the geometrical capacitance (i.e., $C = \epsilon_0\epsilon_r A/t$, where A is the area of the graphene electrode), without considering the edge effects and assuming a nominal thickness of 100 nm (see Figure S2),

resulting in $\epsilon_r \approx 3$, in agreement with previously reported values for P3HT.^{44-46,55} Figure 3d shows that the resistance and the capacitance scale as $1/A$ and A , respectively. It is worth observing that the dielectric constant calculated for small devices is affected by the large error due to geometrical variability as reported in Figure 4e.

Given A^{**} and ϵ_r , one can finally use eqs 1-3 to fit the experimental J - V s and extract ϕ_B , μ , and N_0 , as anticipated above. Figure 4a shows the J - V curve of a representative device having a diameter of $20\text{ }\mu\text{m}$. The gray circles represent the raw data, while the orange and blue circles are the processed data for the positive and negative biases, respectively, where V is replaced by $V' = V - R_s I$. The barrier height and R_s are obtained by a parametric fit of the TE model (eq 1) in R_s of the processed data in the high voltage regime ($|V| > 1$), where R_s spans the interval 0 - $100\text{ k}\Omega$ in steps of $100\text{ }\Omega$. The fit result in $R_s = 15.4\text{ k}\Omega$, $\Phi_{\text{B,Gr/P3HT}} = 0.31\text{ eV}$, and $\Phi_{\text{B,Au/P3HT}} = 0.25\text{ eV}$, giving a built-in potential of about 60 meV . The barrier height measured by KPFM in ambient on a representative device resulted in $\Phi_{\text{B,Au/P3HT}}^{(\text{KPFM})} = 0.10 \pm 0.03\text{ eV}$ and $\Phi_{\text{B,Gr/P3HT}}^{(\text{KPFM})} = 0.16 \pm 0.03\text{ eV}$, which differ from those extracted from the fit of the J - V s, although they follow the same trend $\Phi_{\text{B,Gr/P3HT}} > \Phi_{\text{B,Au/P3HT}}$ (refer to the Supporting Information for details on the KPFM measurements). This inconsistency should not be a surprise, as the KPFM strongly depends on the purity of the surface and therefore on the measuring environment,⁵⁶ which differs from the environment of the J - V measurements. Nevertheless, the built-in potential measured by KPFM matches the value obtained from the fitting of the J - V curves. This could be ascribed to a similar shift in the graphene and gold work functions, such that the built-in potential of the stack depends mostly on the doping of P3HT when exposed to air.^{35,39} It is worth observing that $\Phi_{\text{B,Au/P3HT}}$ differs from previously reported values for Au/P3HT interfaces measured with other techniques or in different environments,^{57,58} ultimately pointing to the fact that the estimation of the barrier height is very sensitive to both the measurement conditions and the measurement method. The inset of Figure 4a shows the current density in the low voltage regime ($|V| < 1$). Since the built-in potential is very small, the flat-band condition is very close to the equilibrium condition. Therefore, the SCL is observed for small biases, in agreement with eq 2. Fitting the current density for negative biases with eq 2 results in an out-of-plane hole mobility of $\mu \approx 2.4 \times 10^{-4}\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, similar to previously reported values for in-plane hole mobility in P3HT.^{40,53} Fitting

the current density for positive biases with eq 3 gives the density of charge carriers at the Gr/P3HT interface, which corresponds to the intrinsic carrier concentration of P3HT (see the Supporting Information). This results in $N_0 \approx 1.1 \times 10^{15} \text{ cm}^{-3}$, also in agreement with previously reported values for intrinsic P3HT in a vacuum.^{40,53} In the SCL model, the charge carrier density at the contacts depends on the density of states in the semiconductor and on the potential barrier height at the interface. From N_0 , one can therefore calculate the charge carrier density at the Au/P3HT interface, resulting in $\sim 1.2 \times 10^{16} \text{ cm}^{-3}$. The difference between $N_{0,\text{Au/P3HT}}$ and $N_{0,\text{Gr/P3HT}}$ is in agreement with the experimental evidence that $J \sim V$ for positive bias and $J \sim V^2$ for negative bias (see the Supporting Information for a discussion). The J - V dependencies are especially clear in the inset of Figure 4a and in Figure 4b.

Figure 4c shows the energy band diagram of the Au/P3HT/Gr heterostructure sketched using the barrier heights extracted from the fit of the J - V s, and assuming that the P3HT is fully depleted, as proven by capacitive measurements. The curvature of the HOMO and LUMO levels in proximity of the interfaces qualitatively describes the potential barrier lowering due to the image charge effect. The Fermi level of P3HT lies close to the HOMO level, as expected from Fermi level pinning due to interface states.^{59,60}

Table 1 reports a statistical summary on five devices per area of the extracted electrical parameters. The dispersion of the extracted parameters is quite small. In order to take into account the edge effects (see the Supporting Information), the P3HT thickness of small devices was set to a value slightly larger than that measured by AFM on a representative device having a diameter of 20 μm .

CONCLUSIONS

This work demonstrates a potentially upscalable fabrication process for Au/P3HT/Gr VdW heterostructures on Si/SiO₂ and describes the charge injection and transport mechanism across the heterostructures. The device output characteristic is independent from the device size for device diameters from 50 μm down to 5 μm , making device downscaling accessible and possibly limited solely by lithography resolution.

Impedance spectroscopy measurements shows that the P3HT is fully depleted in the high bias regime ($|V| > 1 \text{ V}$ or $|V|/t > 10 \text{ MV/m}$), and therefore, the dielectric constant of P3HT is determined from the geometrical capacitance of the devices, resulting in $\epsilon_r \approx 3$. The electrical transport measurements show that the charge injection across the Au/P3HT and Gr/P3HT interfaces is dominated by TE in the high bias regime ($|V| > 1 \text{ V}$), with potential barriers of $\Phi_{\text{B,Gr/P3HT}} = 0.31 \text{ eV}$ and $\Phi_{\text{B,Au/P3HT}} = 0.25 \text{ eV}$, respectively, and by the SCL current in the low bias regimes ($|V| < 1 \text{ V}$). The intrinsic carrier concentration and the out-of-plane hole mobility of P3HT, determined by fitting the J - V s in the low bias regime with the SCL model, resulted in $\mu \approx 2.8 \times 10^{-4} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $N_0 \approx 1.16 \times 10^{15} \text{ cm}^{-3}$, similar to literature values extracted from in-plane FET measurements. The energy band diagram of the heterostructure shows that the interface traps/defects pin the Fermi level very close to the HOMO level of P3HT.

Since the current in Au/P3HT/Gr heterostructures is injection-limited, the hole mobility of P3HT does not limit the operating frequency of the stack, which exceeds 1 MHz for bias approaching 10 V. Higher cutoff frequencies could be

achieved by making Ohmic the contact between the electrodes and P3HT, for instance, by introducing a (heavily) doped OSC layer between the electrodes and the OSC, such as F₄TCNQ- or F₆TCNQ-doped P3HT.

Overall, this work shows that graphene can be implemented as a top or interlayer electrode in vertical devices based on multilayer van der Waals heterostructures. For instance, the charge injection between gold and P3HT could be optimized to achieve high operating frequencies, while the Gr/P3HT interface is kept as is to exploit its rectifying nature. With graphene acting as a permeable electrode, the Gr/P3HT heterostructure studied in this work could become the core element to build future vertical organic transistors based on two back-to-back Gr/P3HT diodes.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsami.2c13148>.

Fabrication process of Au/P3HT/Gr heterostructures; FIB/SEM/AFM characterizations; electrical transport characterization, including all traces from all devices; Kelvin probe force microscopy (KPFM) analysis of the interfaces; chip overview; space-charge limited (SCL) current modeling. (PDF)

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Author Contributions

J.O. and M.S. fabricated the devices. J.O. took the Raman spectra. J.O. and D.B. did all electrical measurements and modeling. R.F. grew the CVD graphene. J.O. and A.R. took the AFM images. M.D.M. and D.V. performed and analyzed the KPFM experiments. The manuscript was written by J.O. and D.B. with contributions and discussions from all authors. The work was supervised by M.C. and D.B. The SNF and ANR funding were acquired by M.C. and D.V. The H2020 funding was acquired by D.B. All authors have participated to the review of and have given approval to the final version of the manuscript.

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Notes

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ABBREVIATIONS

OSC, organic semiconductor; Gr, graphene; PMMA, poly(methyl methacrylate); VdW, van der Waals; P3HT, poly(3-hexylthiophene-2,5-diyl); TE, thermionic emission; SCL, space-charge limited; PFE, Poole-Frenkel emission; CVD, chemical vapor deposition; RR, regio-regular; OLED, organic light emitting diode

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Supporting information

Charge transport across Au-P3HT-Graphene Van der Waals vertical heterostructures

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Fabrication of Au/P3HT/Gr heterostructures

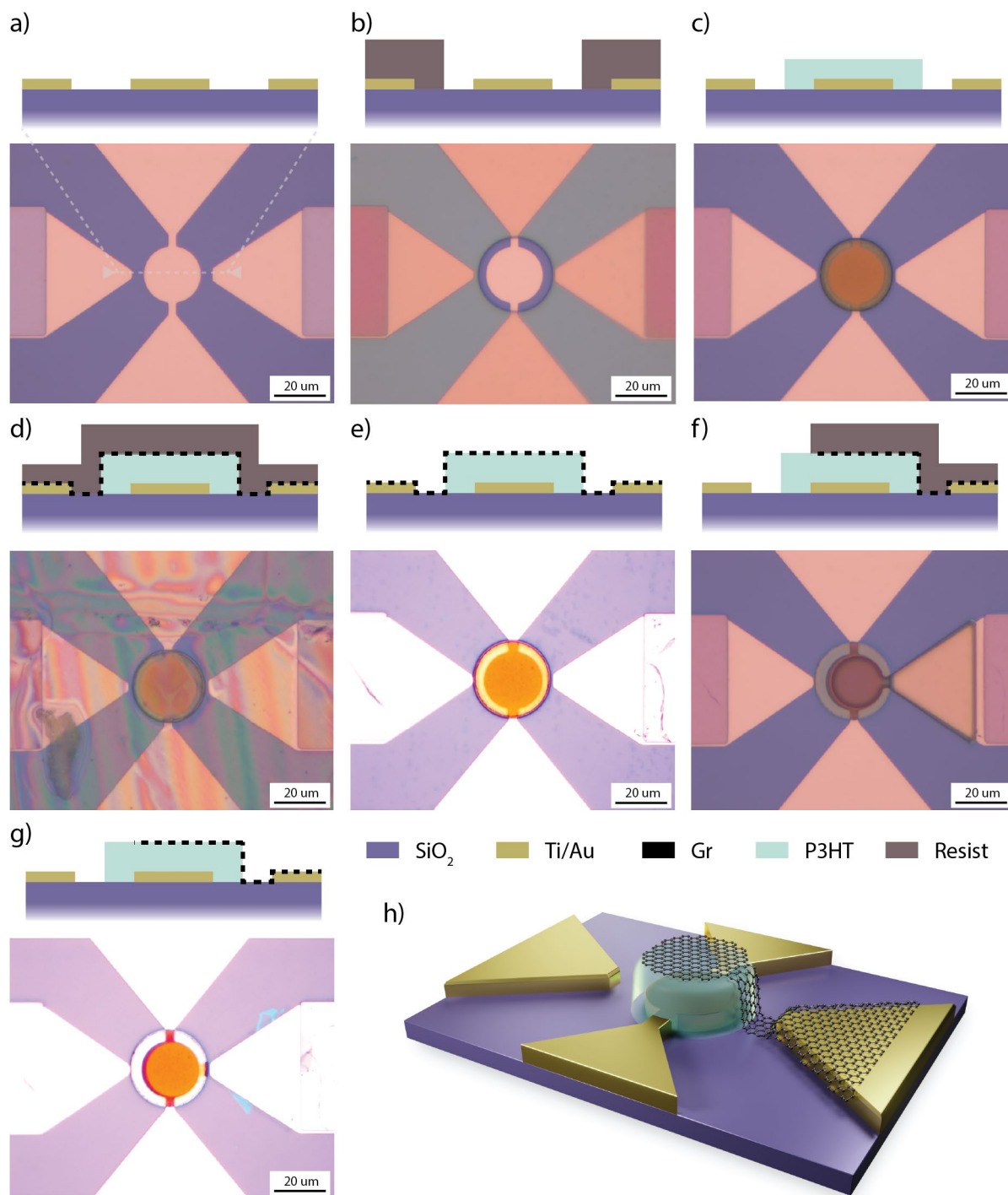


Figure S1. Fabrication steps of the vertical Au/P3HT/Gr heterostructure. (a) Patterning of the bottom electrodes. The grey dashed lines show the schematic of the section (top) on the optical microscope image (bottom). (b) Preparation of the lift-off resist. (c) P3HT deposition and

patterning. (d) CVD graphene transfer. (e) PMMA removal from graphene. (f) RIE patterning of the graphene top electrode. (g) PMMA/Optical resist removal from graphene. (h) 3D schematic of the device (not in scale)

Figure S1 shows the main fabrication steps of the Au/P3HT/Gr heterostructure, which consists in

a) *Patterning of the bottom electrodes*

Ti (5nm) / Au (30 nm) electrodes are fabricated on a 4 inches Si (525 μm) / SiO₂ (300 nm) wafer, which is pre-cleaned in oxygen plasma (600 W for 5 min). The electrodes (Ti/Au) are deposited by e-beam physical vapour deposition (EBPVD) and patterned by lift-off in DMSO at 100°C for 30 min. The resist for the lift-off (AZ2020nlof) is spin-coated (4000 rpm for 60 s), exposed to UV light (lamp intensity 11 mW/cm²) through an optical mask, and then developed (AZ726mif, 35 s).

b) *Preparation of the lift-off resist*

The chip with pre-patterned electrodes (Si/SiO₂/Ti/Au) is ultra-sonicated in Acetone for 5 min, rinsed with IPA and blown dry with nitrogen. Then, it is exposed to oxygen plasma at 600 W for 5 min. After HMDS treatment, the chip is coated with a double layer positive optical resist: first, the chip is spin-coated with a LOR5B resist (4000 rpm, 40 s) and backed at 180°C for 5 min. Then, it is spin-coated with an AZ1505 positive resist (4000 rpm, 40 s) and backed at 110°C for 1 min. The device area is exposed for 1.8 s to UV light (lamp intensity 11 mW/cm², dose 20 mJ) through an optical mask. Finally, the exposed resist is developed in AZ400K (400K:DIW, 1:4) for 25 s and rinsed with de-ionized water.

c) *P3HT deposition and patterning*

A 100 nm film of P3HT is obtained by spin-coating 10 mg/ml solution of P3HT in chlorobenzene (1000 rpm for 60 s) on the substrate. Subsequently, the P3HT film is patterned by lift-off in DMSO (5 min). The chip is then rinsed in de-ionized water, blown dry with nitrogen and finally annealed overnight at 110°C in vacuum (~1mbar).

d) *CVD graphene transfer*

CVD graphene foil (Cu/Gr/PMMA) is placed to float in a copper etchant (Transene CE-100) for 1h, the PMMA layer facing upwards. Once the copper is completely etched (Gr/PMMA), the etchant is removed and replaced with de-ionized water, twice. Then, the foil is transferred to a 10% HCL cleaning solution for 5 min and transferred back to de-ionized water, twice. The

floating graphene foil (Gr/PMMA) is transferred onto the substrate (Si/SiO₂/Au/P3HT/Gr/PMMA) and let dry in air for 1 h.

e) *PMMA removal from graphene*

The chip is annealed overnight at 80°C in vacuum (~1 mbar). The top PMMA layer is removed in Acetone (5 min) and the chip annealed again overnight at 80°C in vacuum (~1 mbar).

f) *RIE patterning of the graphene top electrode*

The chip is first spin-coated with a 50K PMMA resist (AR-P 632.06, 4000 rpm for 60 s), then with an AZ1505 optical resist (4000 rpm, 40 s) and backed at 110°C for 1 min. The device area is exposed for 1.8 s to UV light (lamp intensity 11 mW/cm²) through an optical mask. The exposed optical resist is developed in AZ400K (400K:DIW, 1:4) for 15 s and rinsed with de-ionized water. Then, RIE is used to remove the first layer of PMMA 50K and graphene (O₂, 30 sccm, 25 W).

g) *PMMA/Optical resist removal from graphene*

The PMMA/Optical resist protecting the graphene electrode is removed with Acetone (1 min), then the chip is rinsed in de-ionized water and blown dry with nitrogen.

FIB/SEM/AFM Characterization

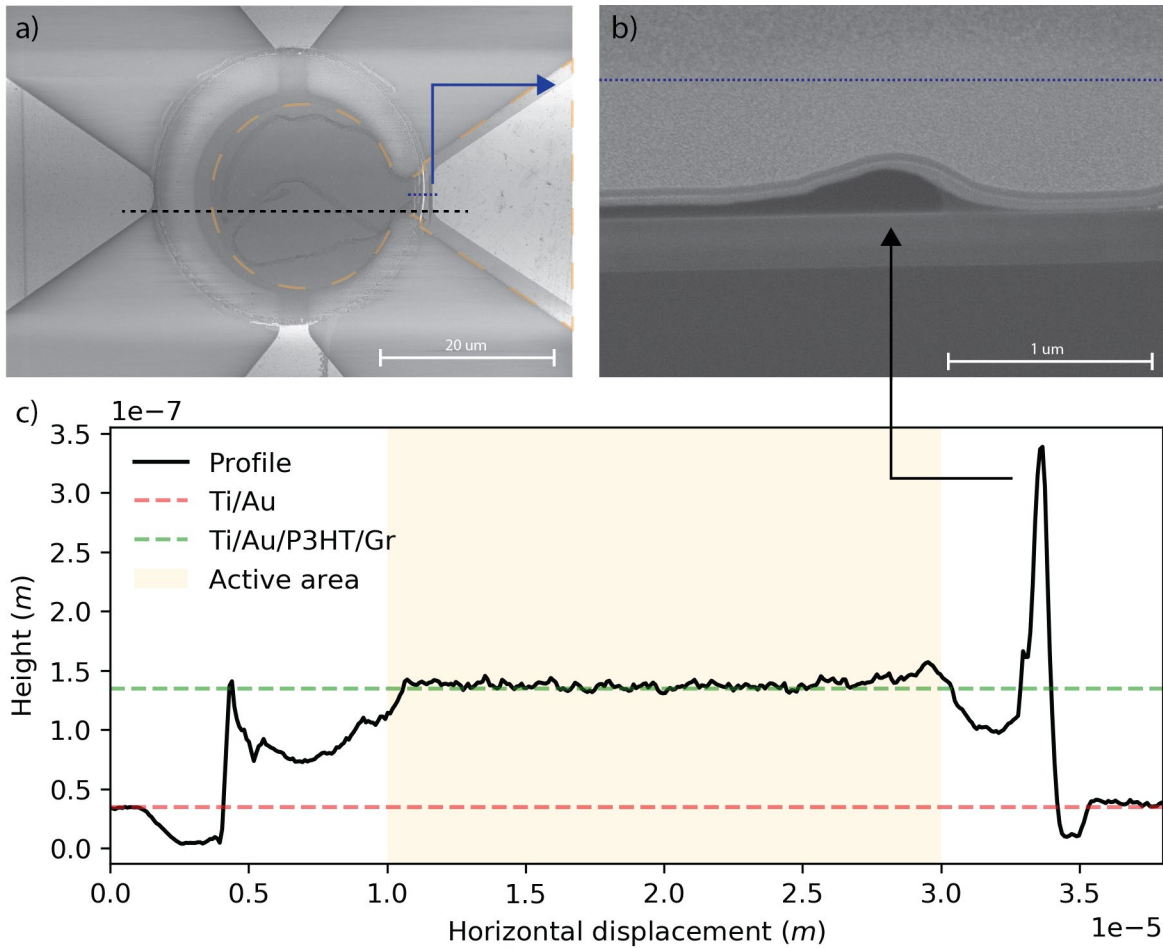


Figure S2. SEM images. (a) Top view of a representative device. The orange dashed line shows the contour of the graphene electrode. The blue dashed line shows the location of the cross-section of (b). (b) Cross-section showing the right edge of P3HT. (c) AFM height profile of the Au/P3HT/Gr stack. The red dashed line show the height of the Ti/Au electrodes, i.e. 35 nm. The green dashed line represent the height of the Tia/Au/P3HT/Gr stack, i.e. 135 nm. From this, the deduced thickness of the P3HT layer is roughly 100 nm.

Figure S2a shows the SEM image and of a representative device. The graphene electrode is clearly visible and contoured with an orange dashed line. Graphene bilayers are distinguishable on the Au side contact. Figure S2b and S2c shows the cross-section corresponding to the dotted blue and

dashed black line, respectively, in Figure S2a. The thickness of the P3HT film in the device center is uniform, while it is not on the device edge, where a higher ring possibly due to capillary/adhesion forces of the P3HT to resist prior to lift-off is observed. Although not desirable, the high edge does not affect the geometry of the device, which is entirely dictated by the region where the bottom and the top electrodes superimpose (active area shown in Figure S2c), and does represent an issue for the graphene electrode since it can easily adapt to the smooth shape of the P3HT edge (Figure S2b).

Electrical transport characterization

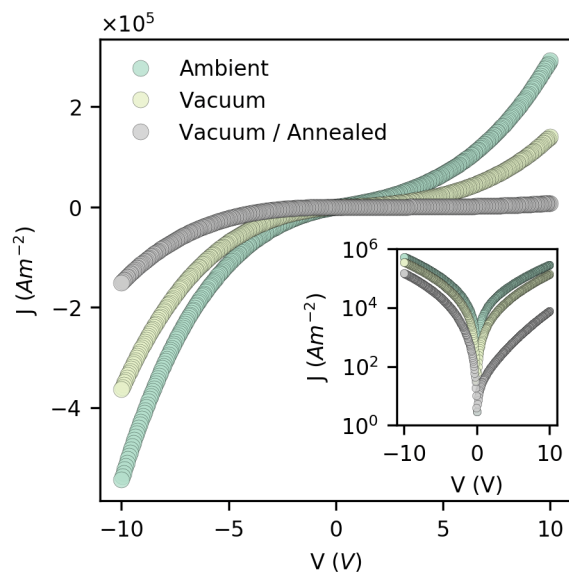


Figure S3. J-V traces of a $10 \mu\text{m}$ wide vertical Au/P3HT/Graphene device in ambient, in vacuum and in vacuum after annealing at 110°C for 12 h. The inset shows the same traces on log scale.

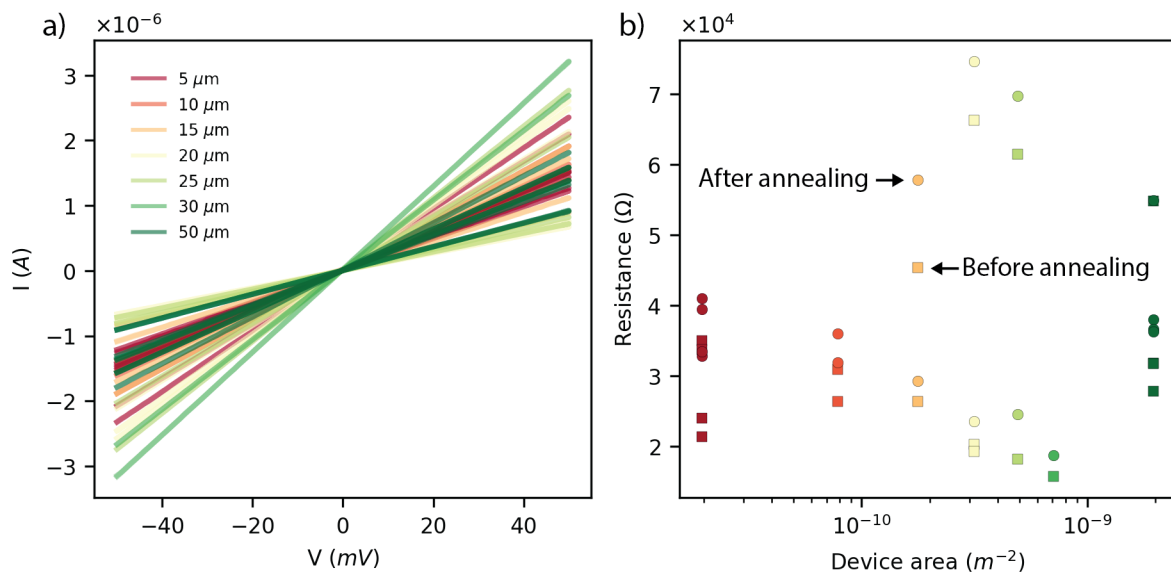


Figure S4. Graphene in-plane conductivity measurements. The total number of samples shown in the plot is 17. (a) Measured current vs. bias in the devices. Square symbols represent the devices measured in vacuum before annealing. Circles represent the devices measured after annealing. (b) Graphene resistance vs. device area.

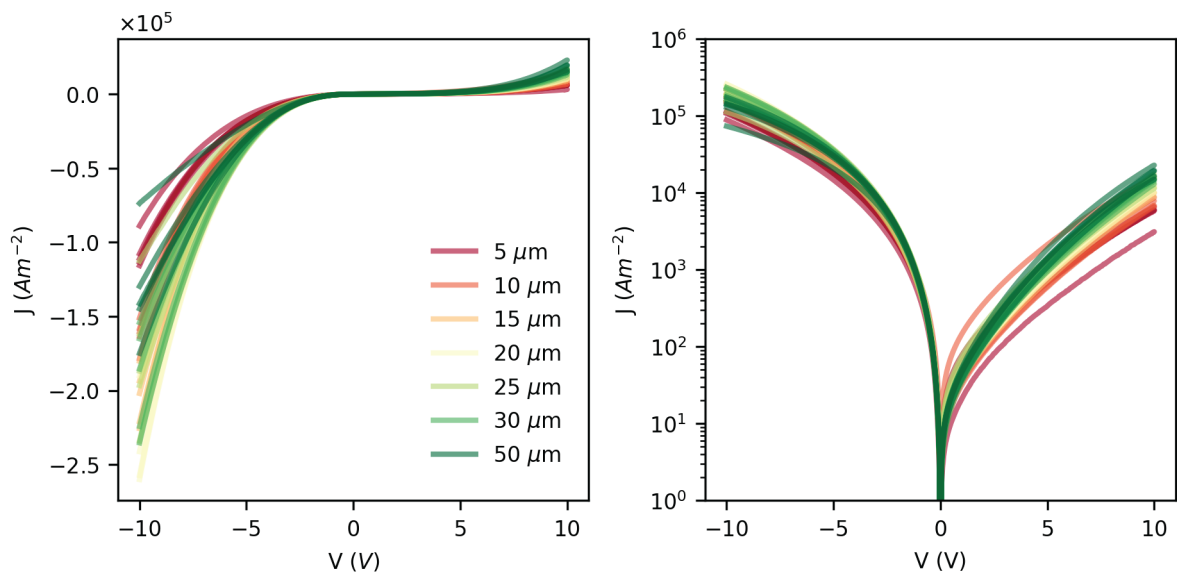


Figure S5. J-Vs of five devices per area of the vertical Au/P3HT/Gr devices measured in vacuum after annealing.

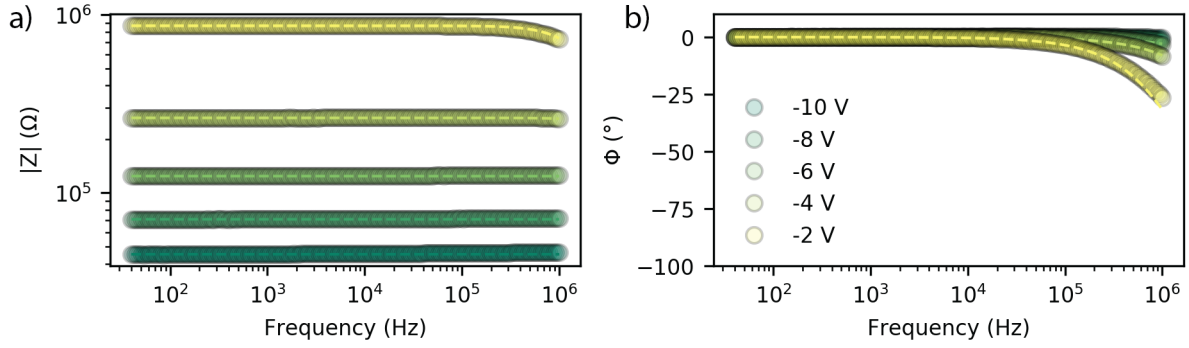


Figure S6. Impedance analysis. Modulus (a) and phase (b) of a representative 20 μm device for negative applied bias. The R||C system cut off frequency shifts above 1MHz for negative applied bias, where the resistance drops and becomes comparable to the graphene series resistance.

The dielectric constant ϵ_r of P3HT for different devices is calculated using the parallel plate capacitor equation (Eq. S1). The results are shown in Table 1.

$$C = \epsilon_0 \epsilon_r \frac{A}{t} \quad \text{Eq. S1}$$

Where ϵ_0 is the vacuum permittivity, A is the device area and t the device thickness. The propagation errors at first order is calculates as shown in Eq. S2.

$$\Delta\epsilon_r = \frac{1}{\epsilon_0} \sqrt{\left(\frac{t}{A} \Delta C\right)^2 + \left(\frac{C}{A} \Delta t\right)^2 + \left(\frac{Ct}{A^2} \Delta A\right)^2} \quad \text{Eq. S2}$$

Where ΔC is the fit error, $\Delta t = 30$ nm is the estimation of the thickness error and $\Delta A = \pi ((d_{Au} - d_{Gr})/2)^2$ is the estimation of the area error. Where d_{Au} and d_{Gr} are the diameter of the gold and graphene electrodes, respectively.

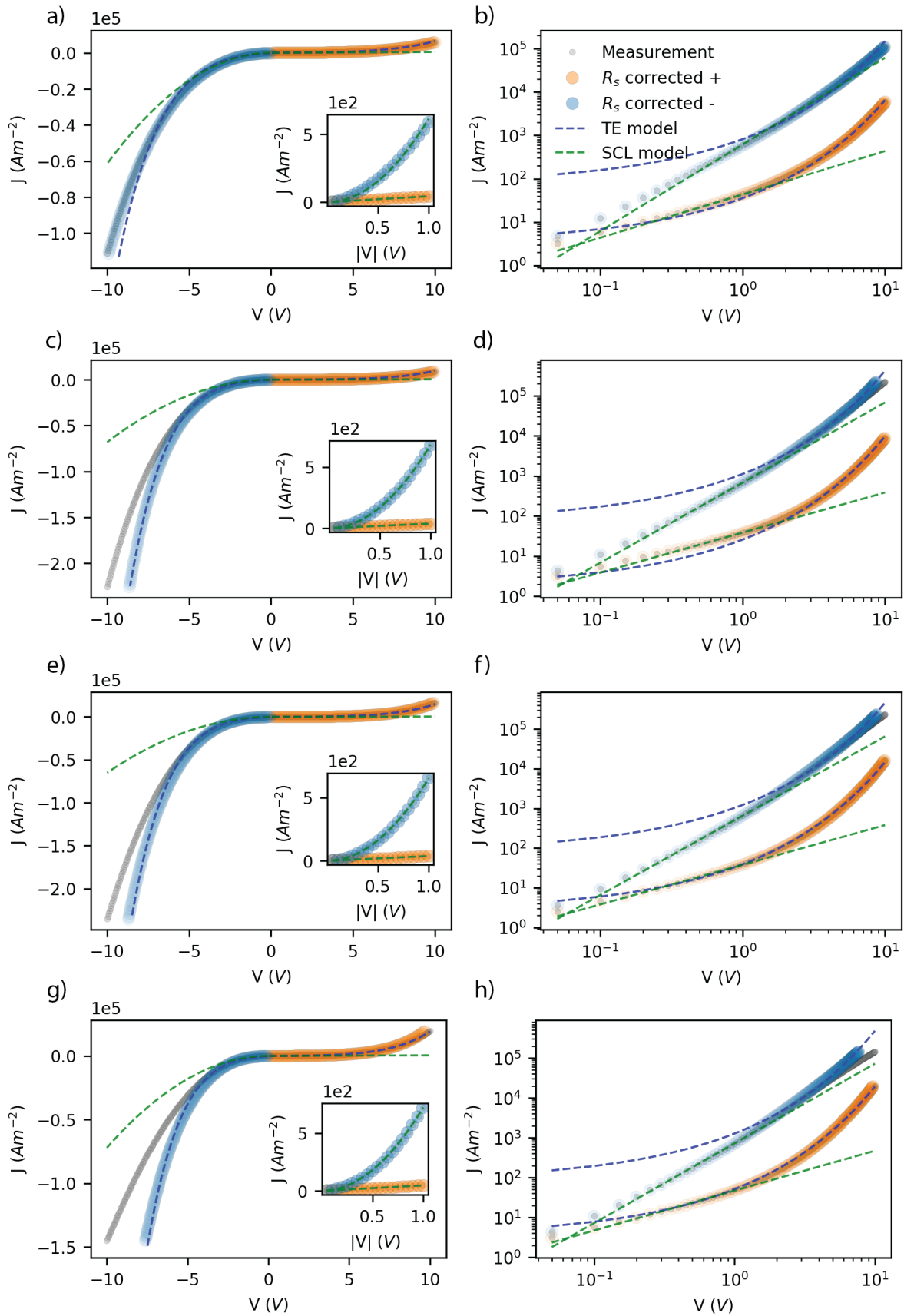


Figure S7. SCL and TE models fitting for different device with diameters: (a-b) 5 μm , (c-d) 15 μm , (e-f) 25 μm , and (g-h) 50 μm . Table 1 shows the statistic of fitting parameters. (a-b) In Fig. S2, one can observe a slightly thicker organic layer around the edge of the devices active area. The latter could have affect the actual average thickness of small devices. To take this effect into account, the thickness of the 5 μm and 10 μm device was set to 130 nm and 120 nm. For all the other devices, where the edge area can be neglected compared to the whole device area, the thickness was set to 100 nm.

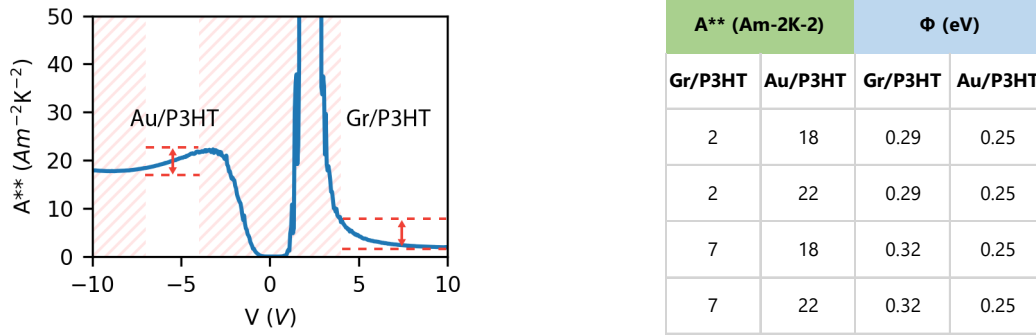


Figure S8. (Left) A^{**} as a function of voltage extracted from temperature dependent IV measurements on the representative 5 μm device. A^{**} in the range from -10 V to -7 V is neglected because of the graphene series resistance. Similarly, A^{**} in the range from -4 V to 4 V is also neglected because of instrumentation sensitivity. (Right) Potential barrier height calculated for A^{**} values spanning the whole range (ca. 18-22 $\text{Am}^{-2}\text{K}^{-2}$ for Au/P3HT and 2-7 $\text{Am}^{-2}\text{K}^{-2}$ for Gr/P3HT).

Kelvin Probe Force Microscopy (KPFM)

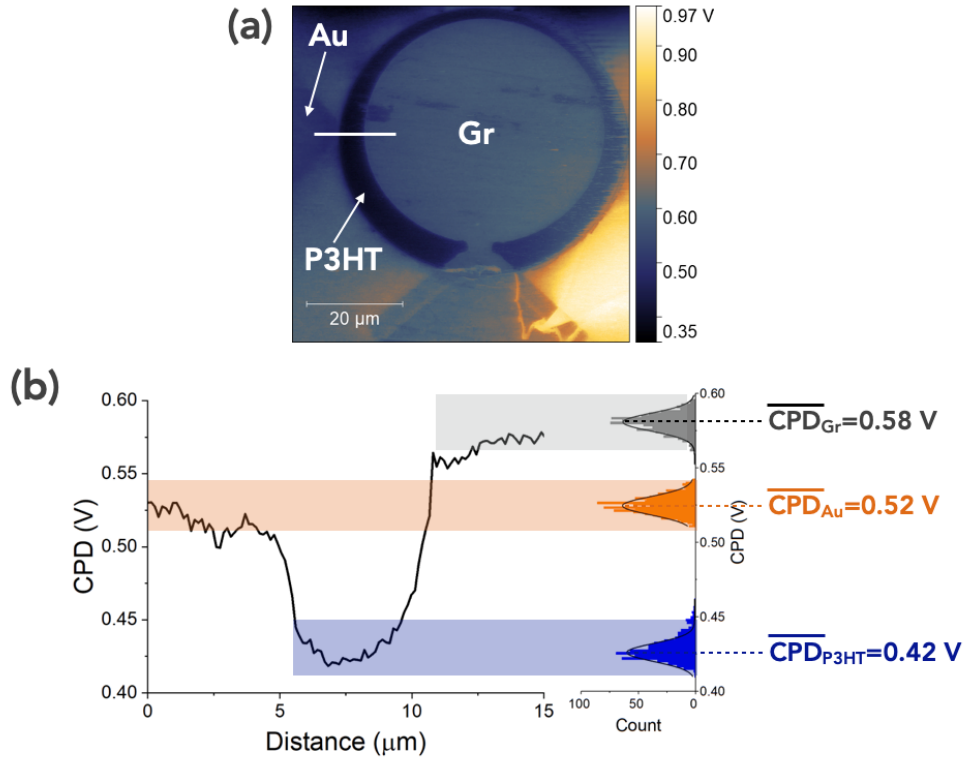


Figure S9. (a) CPD image of a 50 μm device with the different parts (bottom Au electrode, P3HT film and top graphene electrode) indicated. (b) CPD profile along the white line shown in (a) and histograms of the CPD values measured on Au, Gr and P3HT. The black lines are the fits with a Gaussian distribution, the mean CPD values are given in the figure (FWHM of 14 meV in all cases).

Figure S9a shows a Contact Potential Difference (CPD) image of a 50 μm device, where the top Gr electrode, the P3HT and the bottom Au electrode are clearly distinguishable. A CPD profile along the white line shown in Figure S9a reveals (Figure S6b) the variations of the CPD for the Au electrode, the P3HT film and the graphene electrode. CPD histograms recorded locally on the Au, P3HT and Gr are shown in the right panel of Figure S9b. Therefore, the deduced potential barrier at the interfaces are $\Phi_{B,Au/P3HT} = 0.10 \pm 0.013$ eV and $\Phi_{B,Gr/P3HT} = 0.16 \pm 0.013$ eV. These values show a similar trend as obtained from the I-V measurements ($\Phi_{B,Gr/P3HT} > \Phi_{B,Au/P3HT}$) with the same built-in potential (60 meV). However, the KPFM barrier heights are

smaller. This can be ascribed to the fact that the I-V measurements were done in vacuum after annealing. In this latter case, the obtained potential barriers at the interfaces are larger than the ones obtained from KPFM measurements done in air and ambient condition.

Chip overview

	A	B	C	D	E	F	G	H	I	J	K	GE diam.	ME diam.
A	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	5	7
B	BA	BB	BC	BD	BE	BF	BG	BH	BI	BJ	BK	5	7
C	CA	CB	CC	CD	CE	CF	CG	CH	CI	CJ	CK	5	7
D	DA	DB	DC	DD	DE	DF	DG	DH	DI	DJ	DK	10	12
E	EA	EB	EC	ED	EE	EF	EG	EH	EI	EJ	EK	10	12
F	FA	FB	FC	FD	FE	FF	FG	FH	FI	FJ	FK	15	17
G	GA	GB	GC	GD	GE	GF	GG	GH	GI	GJ	GK	15	17
H	HA	HB	HC	HD	HE	HF	HG	HH	HI	HJ	HK	20	22
I	IA	IB	IC	ID	IE	IF	IG	IH	II	IJ	IK	20	22
J	JA	JB	JC	JD	JE	JF	JG	JH	JI	JJ	JK	20	22
K	KA	KB	KC	KD	KE	KF	KG	KH	KI	KJ	KK	25	27
L	LA	LB	LC	LD	LE	LF	LG	LH	LI	LJ	LK	25	27
M	MA	MB	MC	MD	ME	MF	MG	MH	MI	MJ	MK	30	32
N	NA	NB	NC	ND	NE	NF	NG	NH	NI	NJ	NK	30	32
O	OA	OB	OC	OD	OE	OF	OG	OH	OI	OJ	OK	50	52
P	PA	PB	PC	PD	PE	PF	PG	PH	PI	PJ	PK	50	52
Q	QA	QB	QC	QD	QE	QF	QG	QH	QI	QJ	QK	50	52
Type	Open	Short	Stack	Stack	Stack.	Stack	Stack	Stack	Stack	Bridge	Bridge		

Table S1. Overview of the entire chip. Green cases show the working devices, while the red cases are the not working ones. Roughly, 50% of the chip devices are working and show the same J-V behavior of the device shown in Fig. 5.

Space-charge limited (SCL) current modeling

The analytical solution of the space-charge limited (SCL) current is here reported for convenience, as proposed in previous works.¹⁻⁴

1) From the continuity equation:

$$J = qn\mu E(x) + qD \frac{\partial n}{\partial x} \quad \text{Eq. S3}$$

and the Poisson equation:

$$\frac{\partial}{\partial x} E(x) = -\frac{q}{\epsilon} n(x) \quad \text{Eq. S4}$$

2) Assuming that the diffusion current is negligible³:

$$J = qn\mu E(x) = -\epsilon\mu E(x) \frac{\partial E(x)}{\partial x} \quad \text{Eq. S5}$$

3) Integrating Eq. S5:

$$\int_0^x J d\vartheta = J \int_0^x d\vartheta = \epsilon\mu \int_0^x E(\vartheta) \frac{\partial E(\vartheta)}{\partial \vartheta} d\vartheta$$

$$Jx + K = \frac{1}{2} \epsilon\mu E(x)^2 \quad \text{Eq. S6}$$

where K is a constant.

4) Solving Eq. S6 for the electrical field $E(x)$:

$$E(x) = \sqrt{\frac{2J}{\epsilon\mu} (x + K')} \quad \text{Eq. S7}$$

where $K' = \frac{K}{J}$.

5) K' is found using the boundary conditions at the injecting contact ($x = 0$). Defining $n|_{x=0} =$

N_0 and applying the Dirichlet boundary condition $\left. \frac{dE(x)}{dx} \right|_{x=0} = \frac{qN_0}{\epsilon}$, K' is

$$K' = \frac{J\epsilon}{2\mu N_0^2 q^2} \quad \text{Eq. S8}$$

6) Then, plugging K' in Eq. S7:

$$E(x) = \sqrt{\frac{2J}{\epsilon\mu} \left(x + \frac{J\epsilon}{2\mu N_0^2 q^2} \right)} \quad \text{Eq. S9}$$

$$E(0) = \sqrt{\frac{J^2}{\mu^2 N_0^2 q^2}} = \frac{J}{\mu N_0 q}$$

7) Finally, the voltage associated to the current J in the semiconductor of length L is given by:

$$V = - \int_0^L E(x) dx = \sqrt{\frac{8J}{9\epsilon\mu}} \left[(L + K')^{\frac{3}{2}} + K'^{\frac{3}{2}} \right] \quad \text{Eq. S10}$$

8) The current-voltage relation is found solving Eq. S10 for the current. Two solutions are found:

$$J = \frac{9}{8} \epsilon\mu \frac{V^2}{L^3} \quad \text{for } K' \ll L \quad \text{Eq. S11}$$

$$J = q\mu N_0 \frac{V}{L} \quad \text{for } K' \gg L \quad \text{Eq. S12}$$

J is the current density driven through the device by applying the bias V . The other parameters are defined by the semiconductor properties. N_0 , that is the charge carrier density at the interface, is defined by the density of states of the semiconductor N_{DOS} and by the potential barrier height Φ_B at the interface:

$$n|_{x=0} = N_0 = N_{DOS} e^{-\frac{E_{HOMO} - \Phi_M}{kT}} = N_{DOS} e^{-\frac{\Phi_B}{kT}} \quad \text{Eq. S13}$$

The case of a 20 μm representative device shown in Fig. 5 is considered. N_0 at the Gr/P3HT interface can be measured by (i) extracting the hole mobility of P3HT using Eq. S11 for negative biases and (ii) applying Eq. S12 in the linear region for positive biases. The obtained charge carrier density at the Gr/P3HT interface is $N_0 = 1.1 \times 10^{15} \text{ cm}^{-3}$.

Then, using the potential barrier height (0.31 eV, extracted from TE model) and N_0 at the Gr/P3HT interface, N_{DOS} of P3HT can be calculated: $N_{DOS} = 2.4 \times 10^{20} \text{ cm}^{-3}$. Finally, N_0 at the Au/P3HT can be computed using Eq. S11 and the potential barrier height (0.25 eV). Obtained charge carrier density at the Au/P3HT interface is $N_0 = 1.2 \times 10^{16} \text{ cm}^{-3}$. It is worth observing that the image-charge induced lowering of potential barrier is not considered. N_0 may depend on the applied bias and be larger than the estimated value¹. Figure S10 shows K' vs. J , i.e. the charge carrier density and the electrical field across the stack for the two different boundary conditions.

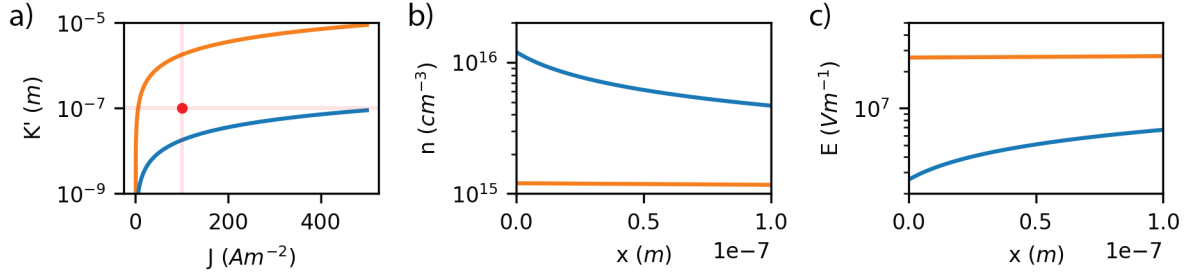


Figure S10. Space-charge limited current model calculated in the current density range of the measured devices. (a) K' vs. J showing the two different solution of the space-charge limited current model (Eq. S9 and S10). The horizontal red line shows $L = 100$ nm of Eq. S8. Orange line corresponds to $N_0 = 1.1 \times 10^{15} \text{ cm}^{-3}$ ($K' > L$) and blue line to $N_0 = 1.2 \times 10^{16} \text{ cm}^{-3}$ ($K' < L$). The vertical red line show the current density used to calculate $n(x)$ and $E(x)$ of plot (b) and (c). (b) Charge carrier density (b) and electrical field (c) across the across the vertical for a current density $J = 100 \text{ Am}^{-2}$.

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