



**HAL**  
open science

# Single-Carrier Phase-Disposition PWM Implementation for Multilevel Flying Capacitor Converters

A. M. Y. M Ghas, J. Pou, G. J. Capella, V. G. Agelidis, R. P. Aguilera,  
Thierry A. Meynard

► **To cite this version:**

A. M. Y. M Ghas, J. Pou, G. J. Capella, V. G. Agelidis, R. P. Aguilera, et al.. Single-Carrier Phase-Disposition PWM Implementation for Multilevel Flying Capacitor Converters. IEEE TRANSACTIONS ON POWER ELECTRONICS, 2015, 30 (10), pp.5376-5380. 10.1109/TPEL.2015.2427201 . hal-03796573

**HAL Id: hal-03796573**

**<https://hal.science/hal-03796573v1>**

Submitted on 5 Nov 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Single-Carrier Phase-Disposition PWM Implementation for Multilevel Flying Capacitor Converters

Amer M. Y. M. Ghias<sup>(1)</sup>    Josep Pou<sup>(1)(2)</sup>    Gabriel J. Capella<sup>(2)</sup>    Vassilios G. Agelidis<sup>(1)</sup>  
Ricardo P. Aguilera<sup>(1)</sup>    Thierry Meynard<sup>(3)</sup>

<sup>(1)</sup>Australian Energy Research Institute & School of Electrical Engineering and Telecommunications,  
The University of New South Wales, UNSW Sydney, NSW 2052, Australia.

<sup>(2)</sup>Terrassa Industrial Electronics Group & Department of Electronic Engineering,  
Technical University of Catalonia, Catalonia, Spain.

<sup>(3)</sup>The Laboratoire d'Electrotechnique et d'Electronique Industrielle (LEEI),  
Institut National Polytechnique de Toulouse, Toulouse 31000, France,  
and also with Cirtem SA, Toulouse 31047, France.

<b>Corresponding Author</b>	Amer M. Y. M. Ghias Australian Energy Research Institute, School of Electrical Engineering and Telecommunications, The University of New South Wales, SYDNEY NSW 2052 AUSTRALIA. Tel: +61-2-9385-4112. Mobile:+61-420-432-616. amer.ghias@unsw.edu.au or amer.ghias@hotmail.com.
---------------------------------	---

## Abstract

This letter proposes a new implementation of phase-disposition pulse-width modulation (PD-PWM) for multilevel flying capacitor (FC) converters using a single triangular carrier. The proposed implementation is much simpler than conventional PD-PWM techniques based on multiple trapezoidal shaped carriers, generates the same results as far as natural capacitor voltage balance is concerned and offers better quality line-to-line voltages when compared to phase-shifted PWM. The proposed algorithm is based on re-shaping the reference signal to fit within the range of a single carrier and assigning each crossing of the reference signal with the carrier to a particular pair of switches at any time. The proposed algorithm is suitable for digital implementation taking maximum benefit from the PWM units available in the processor. Simulation and experimental results are presented from the five-level FC Converter to verify the proposed PD-PWM implementation.

**Note:** This is not currently under review by any other journal for possible publication.

# Single-Carrier Phase-Disposition PWM Implementation for Multilevel Flying Capacitor Converters

## I. INTRODUCTION

Multilevel converters have attracted significant interest for medium/high power applications [1]–[3]. Among various multilevel converter topologies [4], the flying capacitor (FC) converter [5] offers some advantages over the neutral-point-clamped (NPC) converter [6], such as that capacitor voltage balance can be achieved without producing low frequency voltage ripples in the FCs, even in converters with a large number of levels.

Phase-shifted pulse-width modulation (PS-PWM) is a common technique applied to FC converters. PS-PWM provides natural capacitor voltage balance but the quality of line-to-line voltages is not the best. On the other hand, phase-disposition PWM (PD-PWM) produces better line-to-line voltages than PS-PWM, but it cannot be applied straightforward to the FC converter. Some solutions are based on modifying the shapes of the carriers to produce PD-PWM [7], [8]. However, each cell requires different carriers, which complicates its practical implementation, especially for FC converters with a large number of levels. The technique was simplified in [9], and the number of carriers was reduced from  $(n - 1)^2$  to  $(n - 1)$ , which is the standard number of carriers used in PD-PWM. The main drawback is that it requires a lot of digital signal power processing.

The property of natural capacitor voltage balance in FC converters can be boosted by the addition of *RLC* filters connected to the output of the converter [10]–[12]. Closed-loop voltage balancing methods have also been reported in the technical literature [13]–[19].

This letter proposes a new implementation of PD-PWM for the FC converter. Unlike in [7]–[10], the proposed PD-PWM implementation uses a single triangular carrier for the modulation. Tables or masks containing digital information are used to process the PWM pulses. It is very simple to apply and can be easily programmed in a digital processor requiring only a single PWM unit. The technique can be extended to FC converters with any number of levels.

The letter is organized as follows. Section II describes the operating principle of a FC converter and the PD-PWM technique. Section III introduces the proposed PD-PWM implementation. Section IV presents simulation and experimental results obtained from a three-phase five-level FC converter. Finally, the conclusions are summarized in Section V.

## II. FC CONVERTER AND PD-PWM

### A. Fundamentals

Fig. 1 shows a phase-leg of an  $n$ -level FC converter, which integrates  $n-2$  FCs. The subscript  $x$  is used for the phase identification  $x = \{a, b, c\}$ . The switch pairs in each phase-leg  $s_{x1} - \bar{s}_{x1}, s_{x2} - \bar{s}_{x2}, \dots$ , and  $s_{xn-1} - \bar{s}_{xn-1}$  operate in a complementary manner. During normal operation, the mean voltage values of the

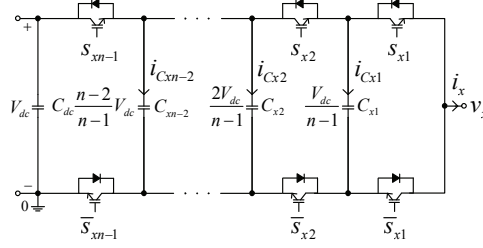


Fig. 1. Phase-leg of a five-level FC Converter.

FCs,  $C_{x1}$ ,  $C_{x2}$ , ..., and  $C_{xn-2}$ , should be maintained at  $V_{dc}/(n-1)$ ,  $2V_{dc}/(n-1)$ , ..., and  $(n-2)V_{dc}/(n-1)$ , respectively, where  $V_{dc}$  is the dc-bus voltage. Consequently, the voltage across each switch is only  $1/(n-1)$  of the dc-bus voltage. Each converter phase-leg can generate  $n-1$  output voltage levels, i.e.  $0$ ,  $V_{dc}/(n-1)$ ,  $2V_{dc}/(n-1)$ , ...,  $(n-2)/(n-1)V_{dc}$ , and  $V_{dc}$ , with respect to the dc negative rail "0".

### B. PD-PWM

In standard PD-PWM,  $n-1$  carriers of the same amplitude, frequency, and phase are arranged in a level shifted manner that occupy the linear modulation range. The reference signal is compared with the carriers to define the voltage levels that have to be generated at the output. This technique is spectrally superior to other carrier layouts because it produces large harmonic concentration at some specific frequencies that cancel in the line-to-line voltages, hence reducing their total harmonic distortion (THD) [10], [20]. However, when PD-PWM is applied to the FC converter, and each carrier should not be associated to a specific cell, otherwise capacitor voltage balance cannot be achieved. This is because the reference signal crosses a single carrier at any sampling period and hence only the cell associated to that carrier will switch. As a consequence, the FC voltages will keep on increasing or decreasing depending on the the direction of the output current  $i_x$ , thus deviating from their reference values.

In PS-PWM, natural capacitor voltage balance is achieved when the consecutive carriers are phase shifted by  $2\pi/(n-1)$ . Based on this idea, a carrier rotation technique was proposed using PD-PWM [7], [8]. This rotation implies that each specific carrier defines switching transitions to different converter cells. A similar rotation effect is achieved by re-shaping the carriers. Fig. 2 shows the carriers arrangement for a five-level FC converter. Different sets of carriers are required to achieve natural capacitor voltage balance. As it can be deduced from Fig. 2, this implementation of PD-PWM is complex, specially for converters with a high number of levels.

## III. PROPOSED PD-PWM IMPLEMENTATION

The PD-PWM method proposed in [7], [8] requires  $(n-1)^2$  carriers with different shapes and phase dispositions. Its implementation is complex and unpractical, especially for FC converters with a high number of levels. The proposed PD-PWM implementation is based on the same concept but it is radically simplified because a single triangular carrier is used instead. To achieve this, the reference signal  $v_{xref}$  needs to be level-shifted and re-scaled. The band where the reference signal is located (Fig. 2(b)) needs to be determined in order to know the adjustments required. The modified reference signal is compared with the triangular carrier (only

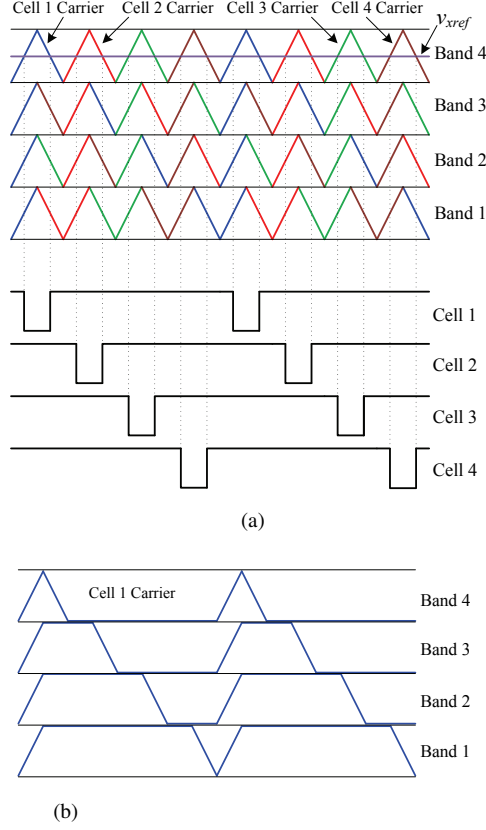


Fig. 2. PD-PWM in a five-level FC converter: (a) association of carrier segments to FC cells and final cell pulses, and (b) standard PD-PWM implementation using trapezoidal carriers (Cell 1).

one carrier). Look-up tables and some digital processing are needed to define the states of all the switches, including those that have to switch during a particular sampling period.

The value that has to be added to the reference signal  $v_{offsetx}$  depends on the band  $b_x$  within it is located ( $b_x = \{1, 2, \dots, n - 1\}$ ). In the general case of an  $n$ -level FC converter:

$$v_{offsetx} = \left(\frac{2}{n-1}\right)(n - b_x) - 1 = \frac{n - 2b_x + 1}{n - 1}. \quad (1)$$

When this offset is added to the reference signal, the operating range is within the interval  $[0, 2/(n - 1)]$ . In order to normalize this range into  $[0, 1]$ , the signal needs to be multiplied by  $(n - 1)/2$ , as follows:

$$v'_{xref} = (v_{xref} + v_{offset}) \frac{n - 1}{2}. \quad (2)$$

Fig. 3(a) shows an example of reference signal with the corresponding bands in the case of a five-level FC converter. From (1) and (2) considering  $n = 5$ , reshaping the reference signal is done using the following equation:

$$v'_{xref} = 3 + 2v_{xref} - b_x. \quad (3)$$

Modulation is performed by comparing the rescaled reference signal with the triangular carrier (Fig. 3(b)) producing the so-called raw PWM. The raw PWM needs to be processed to define the state of each FC converter cell. Digital processing is performed using masks that are allocated in look-up tables. The amount of intervals



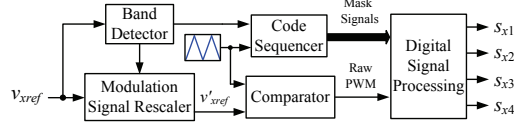


Fig. 5. Diagram of the proposed PD-PWM implementation.

TABLE I  
COMPARISON OF PD-PWM IMPLEMENTATIONS IN FC MULTILEVEL CONVERTERS

PD-PWM Implementations	Number of Carriers	Shape of Carriers	Implementation Difficulty
Proposed one	1	Triangular	Low
[7], [8], [10]	$(n - 1)^2$	Trapezoidal	High
[9]	$n - 1$	Triangular	Medium

transition is in the opposite direction, i.e. ‘0’-’1’. Such transitions are defined by the crossing of the reference signal with the triangular carrier, i.e. by the raw PWM.

Fig. 4 shows a possible implementation for the digital processing. The information included in the masks is designed according to this digital implementation. Coming back to the example in Fig. 3, when the counter indicates Intervals 1 or 4, the raw PWM should be applied to Cell 1. To achieve this, the information provided by the Mask A is ‘1’ (Mask A1 signal) and it leads the raw PWM to the output of the AND gate associated to Cell 1 (Fig. 4(b)). During those intervals, the Mask B should provide a ‘0’ (Mask B1 signal) to let the raw PWM reach the output  $s_{x1}$  through the OR gate. When the counter indicates Intervals 2 or 3, the Mask A1 signal is ‘0’, imposing the output of the AND gate to be ‘0’ and therefore preventing the raw PWM to go to the next stage. The final output for Cell 1 is defined by the state of mask B (signal Mask B1), which is ‘0’ in this case. Similarly, the output  $s_{x1}$  is imposed to be ‘1’ by the signal Mask B1 during the Intervals 5-8. Using this simple two-signal masks, the state of each cell is defined. Fig. 5 shows the block diagram for the proposed implementation. Table II shows the masks for all the cells and bands in the case of a five-level FC converter.

The generation of the masking codes is done off-line and, given a specific  $n$ -level FC converter, the masks are always the same. The mask pointer needs to be synchronized with the carrier signal and it increases whenever the slope of the carrier changes. The number of the interval is odd/even when the carrier signal has a positive/negative slope, respectively. Table I shows the comparison of the proposed PD-PWM implementation with the methods presented in [7]–[10].

#### IV. SIMULATIONS AND EXPERIMENTAL RESULTS

Simulations and Experimental tests are performed on a low power grid-connected five-level FC converter. The proposed PD-PWM implementation has been programmed in a DSPACE 1006 controller with integrated DS 5203 FPGA board. The parameters of the converter are given in table III.

The performance of the proposed PD-PWM implementation is used with a closed-loop grid-connected converter, as shown in Fig. 6. A voltage balancing booster is connected to the converter output [7]–[9]. A

TABLE II  
MASKS USED IN A FIVE-LEVEL FC CONVERTER

Single Carrier Waveform Band 1									
1	2	3	4	5	6	7	8	Counter	
1	0	0	0	0	0	0	1	Mask A1	Cell 1
0	0	0	0	0	0	0	0	Mask B1	
0	1	1	0	0	0	0	0	Mask A2	Cell 2
0	0	0	0	0	0	0	0	Mask B2	
0	0	0	1	1	0	0	0	Mask A3	Cell 3
0	0	0	0	0	0	0	0	Mask B3	
0	0	0	0	1	1	0	0	Mask A4	Cell 4
0	0	0	0	0	0	0	0	Mask B4	

Single Carrier Waveform Band 2									
1	2	3	4	5	6	7	8	Counter	
1	0	0	0	0	1	0	0	Mask A1	Cell 1
0	0	0	0	0	0	1	1	Mask B1	
0	0	1	0	0	0	0	1	Mask A2	Cell 2
1	1	0	0	0	0	0	0	Mask B2	
0	1	0	0	1	0	0	0	Mask A3	Cell 3
0	0	1	1	0	0	0	0	Mask B3	
0	0	0	1	0	0	1	0	Mask A4	Cell 4
0	0	0	0	1	1	0	0	Mask B4	

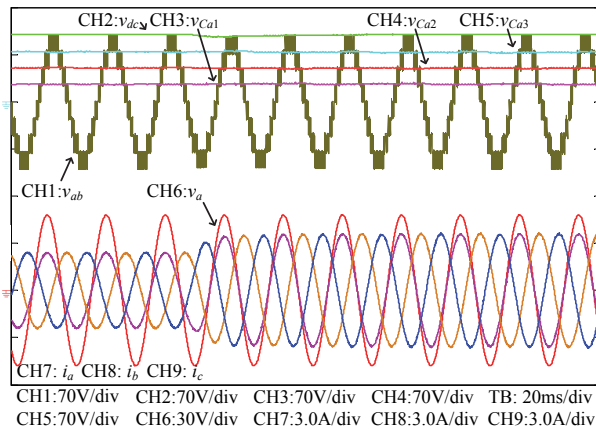
Single Carrier Waveform Band 3									
1	2	3	4	5	6	7	8	Counter	
1	0	0	1	0	0	0	0	Mask A1	Cell 1
0	0	0	0	1	1	1	1	Mask B1	
0	0	1	0	0	1	0	0	Mask A2	Cell 2
1	1	0	0	0	0	1	1	Mask B2	
0	0	0	0	1	0	0	1	Mask A3	Cell 3
1	1	1	1	0	0	0	0	Mask B3	
0	1	0	0	0	0	1	0	Mask A4	Cell 4
0	0	1	1	1	1	0	0	Mask B4	

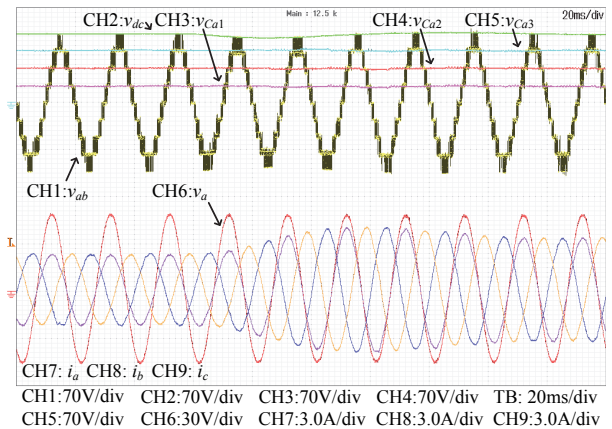
Single Carrier Waveform Band 4									
1	2	3	4	5	6	7	8	Counter	
1	1	0	0	0	0	0	0	Mask A1	Cell 1
0	0	1	1	1	1	1	1	Mask B1	
0	0	1	1	0	0	0	0	Mask A2	Cell 2
1	1	0	0	1	1	1	1	Mask B2	
0	0	0	0	1	1	0	0	Mask A3	Cell 3
1	1	1	1	0	0	1	1	Mask B3	
0	0	0	0	0	0	1	1	Mask A4	Cell 4
1	1	1	1	1	1	0	0	Mask B4	

TABLE III  
PARAMETERS OF GRID CONNECTED FC CONVERTER

Circuit Parameter	Value
RMS Grid Voltage, $E$	60 V
Dc-Bus Voltage, $V_{dc}$	100 V
Dc-Bus Capacitor, $C_{dc}$	2 mF
Flying Capacitors, $C_1, C_2, C_3$	220 $\mu$ F
Grid Inductance, $L$	10 mH
Carrier Frequency, $f_s$	4.1 kHz
Fundamental Frequency, $f$	50 Hz



(a) Simulation



(b) Experimental

Fig. 6. Closed-loop grid-connected FC converter operating with the proposed modulation technique. The load changes from  $R=66\Omega$  to  $R=44\Omega$  at  $t=60$ ms. Top waveforms: line-to-line output voltage, dc-bus and FC voltages. Bottom waveforms: grid voltage and output currents. (a) Simulation and (b) experimental results.



traditional voltage oriented control classical is used for the grid connection [21]. The FCs are charged using the precharging method proposed in [22]. The line-to-line voltage  $v_{ab}$ , dc-bus voltage  $v_{dc}$  and FC voltages ( $v_{Ca1}$ ,  $v_{Ca2}$ , and  $v_{Ca3}$ ) are shown in Fig. 6(a). The converter maintains the FC voltages at the reference values ( $V_{C1}^* = 25\text{V}$ ,  $V_{C2}^* = 50\text{V}$ ,  $V_{C3}^* = 75\text{V}$ ). At  $t=60\text{ms}$ , the load changes from  $R=66\Omega$  to  $R=44\Omega$ . It can be observed that the voltages in the FCs remain unaffected during this transient. Similar results are obtained experimentally from the laboratory prototype, as shown in Fig. 6(b).

## V. CONCLUSION

In this letter, a new implementation of PD-PWM for a FC converter using just a single carrier has been presented. The modulation signals have been properly level-shifted and rescaled to operate in the range of a single triangular carrier. The PWM pulses have been digitally processed to achieve the same effect as in the case of other complex implementations based on using several trapezoidal carriers. The proposed PD-PWM implementation has been presented in a general way so that it could be applied to FC converters with any number of levels. It is easy to apply and very suitable to be processed in a digital processor. In this letter, the proposed PD-PWM implementation has been tested on a five-level FC converter together with an *RLC* voltage balancing booster and it has shown excellent results.

## REFERENCES

- [1] V. Yaramasu, B. Wu, and J. Chen, "Model-predictive control of grid-tied four-level diode-clamped inverters for high-power wind energy conversion," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2861-2873, Jun. 2014.
- [2] T. Freddy, N. A. Rahim, W. P. Hew, and H. S. Che, "Comparison and analysis of single-phase transformerless grid-connected PV inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5358-5369, Oct. 2014.
- [3] V. Yaramasu and B. Wu, "Predictive control of a three-level boost converter and an NPC inverter for high-power PMSG-based medium voltage wind energy conversion systems," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5308-5322, Oct. 2014.
- [4] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Fraquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial application of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553-2580, Jun. 2010.
- [5] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE PESC*, 29 Jun.-3 Jul. 1992, vol. 1, pp. 397-403.
- [6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981.
- [7] S. Lee, D. Kang, Y. Lee, and D. Hyun, "The carrier-based PWM method for voltage balance of flying capacitor multilevel converter," in *IEEE PESC*, Jun. 2001, vol.1, pp. 126-131.
- [8] D. W. Kang, B. K. Lee, J. H. Jeon, T. J. Kim, and D. S. Hyun, "A symmetric carrier technique of CRPWM for voltage balance method of flying-capacitor multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 879-888, Jun. 2005.
- [9] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682-1693, Jun. 2011.
- [10] B. P. Mcgrath and D. G. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase (PD) modulation," *IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933-1942, Jul. 2011.
- [11] B.P. Mcgrath and D. G. Holmes, "Analytical determination of the capacitor voltage balancing dynamics for three phase flying capacitor converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 4, pp. 1425-1433, Jul. 2009.
- [12] B.P. Mcgrath and D. G. Holmes, "Natural capacitor voltage balancing for a flying capacitor converter induction motor drive," *IEEE Trans. Power Electron.*, vol. 24, pp. 1554-1561, Jun. 2009.
- [13] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five-level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658-1667, Apr. 2012.
- [14] G. Gateau, M. Fadel, P. Maussion, R. Bensaid, and T. A. Meynard, "Multicell converters: Active control and observation of flying capacitor voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no.5, pp. 998-1008, Oct. 2002.

- [15] C. Feng, J. Liang, and V. G. Agelidis, "Modified phase-shifted PWM control for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 22, pp. 178–185, Jan. 2007.
- [16] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. Power Del.*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.
- [17] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, Feb. 2012.
- [18] A. M. Y. M. Ghias, J. Pou, M. Ciobotaru, and V. G. Agelidis, "Voltage balancing method using phase-shifted PWM for the flying capacitor multilevel converter," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4521–4531, Sep. 2014.
- [19] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Optimal switching transition-based voltage balancing method for flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1804–1817, Apr. 2015.
- [20] V. G. Agelidis and M. Calais, "Application specific harmonic performance evaluation of multicarrier PWM techniques," in *Proc. IEEE PESC*, 17–22 May 1998, vol. 1, pp. 172–178.
- [21] L. Chen, A. Amirahmadi, Q. Zhang, N. Kutkut, and I. Batarseh, "Design and implementation of three-phase two-stage grid-connected module integrated converter," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3881–3892, Aug. 2014.
- [22] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Initial capacitor charging in grid-connected flying capacitor multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3245–3249, Jul. 2014.