New Multi-Level Multiplexed Power Converter Topology for Medium-Voltage Power Drives

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Abstract

This paper proposes a three-phase multilevel converter topology based on the multiplexed concept which is especially intended for medium-voltage power drives applications. The main potential application are four-quadrant 4.16 kV and 6.6 kV power drives. The proposed topology allows pushing efficiency, switching frequency and cost to values that could not be obtained with HV semiconductors which are expensive and have poor switching performances. This paper will describe the topology, its modulation and control strategy, its main waveforms, the overall efficiency and a comparison with a 5LANPC inverter.

1 Introduction

Multilevel converters have found a great interest and have been widely studied in industry and academia during the last decades. Multilevel topologies development associated to the growth of voltage and current ratings of fast power semiconductors, such as IGBT, have allowed the evolution of medium-voltage (MV) and high-power solutions [1]–[6]. The cost of semiconductor devices, the reliability, the power density and the efficiency are the main criteria used for MV power drives [7], [8].

However, one of the main problems is still the limited switching performance of high voltage (HV) semiconductors (IGBT and diodes) rated between 3.3 kV and 6.5 kV. Figure 1 shows a switching performance degradation and cost elevation as rated voltage increases for the same current (here 450 A). The direct consequence is a severe limitation of the switching frequency or a low efficiency if the application requires a high output frequency to drive the machine. This drop in performance is also reflected in a high cost of these systems.

As cost, efficiency and power density are essential characteristics targeted for MV drives and to get around the limited switching performance of HV semiconductors, a new architecture is proposed for the inverter and rectifier stages (Fig. 2).

The conversion stage topologies and the structure of this Multi-Level Multiplexed (xPlexed) topology will be described in Section 2. Section 3 presents the principle of control and a more in-depth chopper and inverter modulation strategy for the proposed architecture. Comparisons with ANPC-5L (5LANPC) are presented in Section. IV. Finally, the conclusions are given in Section. V.

2 Multiplexed topology for power drives

2.1 Power Converter Structure

The proposed power conversion architecture is mainly composed by three parts: The DC bus voltage, two symmetric DC-DC step-down converters (choppers) and a three phase DC-AC inverter. Proposed solution uses a 3-level NPC inverter associated to a 3-level flying capacitor chopper for 4.16 kV solution (Fig. 2) and a 4-level flying capacitor for the 6.6 kV solution. In a power drive application with four-quadrant operation, an AFE (Active Front End) and inverter are connected in back-to-back configuration (Fig. 3).

The control strategy that will be described in Section 3 shows that it is possible to place most of the switching effort on the chopper stage. The concentration of the switching effort in a single stage combined to an inverter performing only a

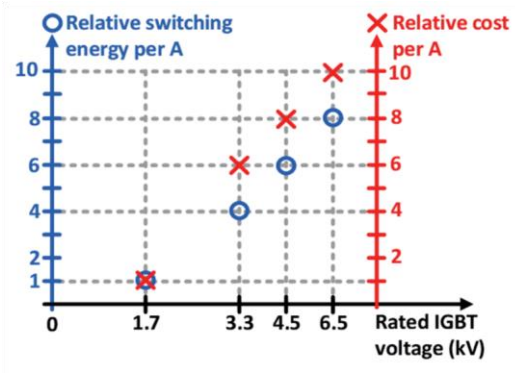

Fig. 1: Relative switching energy and relative cost per rated ampere normalized by 1.7 kV IGBTs.

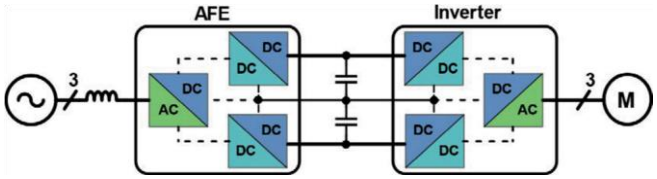

Fig. 2: Power drive application conversion architecture using xPlexed topology.

few switchings could lead to a WideBandGap/Si combination. However, today, even with WBG devices only in the chopper stage, the cost is not compatible with market expectations. But, in this paper we will show that a realistic option is to build such a MV converter using only low-cost silicon devices.

The chopper switches are highly stressed because they switch high currents and switch all the time, so it is interesting to use series connected IGBTs with a lower voltage rating rather than HV semiconductors. Doing so will reduce switching losses and allow higher switching frequency. In addition, using series connected 1.7 kV IGBTs to replace 3.3 kV IGBTs on the flying capacitor converter fits also the main objective of this solution: reduction of overall semiconductors cost.

3 Control strategy for xPlexed converters

In the multiplexed topology the output voltage results of the combined action of the two conversion stages that are interlinked. Consequently, unlike conventional three-phase topologies, this topology does not have independent phase legs [9], [10]. The top and bottom choppers generate, respectively, the highest (in green)(Fig. 4) and lowest (in blue)

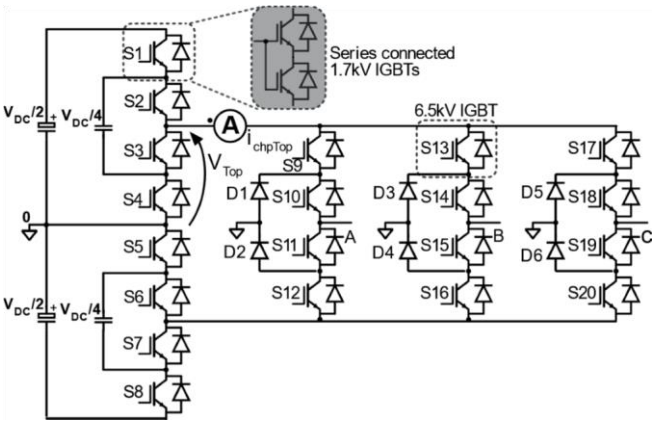

Fig. 3: Proposed Multiplexed DC-AC Inverter with 3level-Flying Capacitor Chopper topology and 3level-NPC Inverter topology for 4.16 kV power drive.

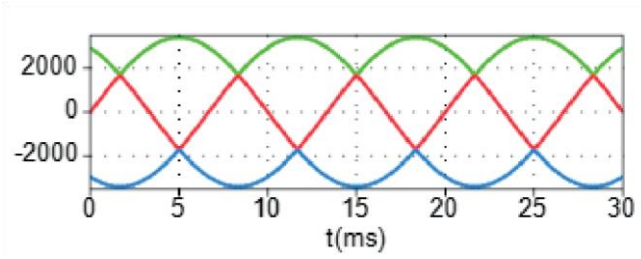

Fig. 4: Three-phase voltage reference signals for chopper and inverter stage for multiplexed architecture. green: Top chopper; red: Inverter; blue: Bot chopper.

voltage of the three-phases reference and the corresponding inverter legs are saturated to a 100 % and a 0 % duty cycle, witch means they are not switching. The remaining inverter arm will generate the intermediate voltage (in red) by switching the square voltage produced by the chopper.

In the next sections chopper and inverter frequency refer to the switching frequency of the switching device, which, in the FC stage, is different from the frequency of the chopped voltage.

3.1 Chopper modulation

The main purpose of the control of the DC-DC choppers is to generate the highest and lowest voltages of the three-phase reference. In addition, because of the DC-DC chosen topology, it must maintain the average current in the flying capacitors at zero [9].

Unlike proposed by [9], where the chopper switches at half of the frequency of the inverter, in this case the chopper switches at the same frequency as the

inverter. As a result, the chopper output frequency will be the product of the inverter switching frequency and the number of switching cells in the chopper.

This is possible because of the switching energies of the 1.7 kV are almost negligible compared to those of HV devices, and it contributes to reduce the flying capacitors size. Consequently, stored energy, volume and even cost can be reduced.

The current supplied by the top (resp. bottom) can take two values: can be equal to the current in the phase with the highest of the three voltages or to this current plus the current in the phase with the mid voltage. In this way, the current supplied by the chopper has a switched shape with a frequency equal to that of the inverter (Fig. 6(b) and Fig. 7(c)). If a frequency ratio like the one described by [9] was used, an almost zero current in each flying capacitor would be guaranteed because the charging and discharging phases of the flying capacitor would occur with almost the same value. So, it would be possible to take advantage of FCs self-balancing property using Phase Shifted (PS) modulation [11],
[12].

However, using the switching frequency for the chopper and inverter, the charge and discharge current of the flying capacitors is no longer symmetrical, because the charge and discharge occur within the same period of the inverter. Therefore, the chopper modulation chosen is based on Phase Disposition (PD) by means of state machines [13]–[15] giving the necessary degree of freedom to balance FC voltages even though this may cost some extra commutations.

Next section will explain how the inverter duty cycle calculation is done respecting the unitary switching frequency ratio between chopper and inverter

3.2 Inverter modulation

For this topology, where the inverter stage is composed by a 3L NPC (Fig. 3), each phase can be seen as two decoupled blocks where each one is responsible to produce, respectively, a positive and negative average output voltage. For example, the positive part of the voltage in phase A will be built by the top chopper and the top NPC switching cell (S9 and S11). These two blocks are symmetric so the analysis that will be done bellow is valid for the positive and negative average voltage.

In order to reduce the inverter switched voltage, the maximum voltage and the switching energy, one of the inverters switching edges will be aligned to the middle of the lower voltage level produced by the chopper on the inverter period. Figure 5(a) shows in red how the inverter re-chops the square voltage generated by the chopper for a rising sawtooth carrier. In this case, the inverter rising edge will be always aligned with the beginning of the first period of chopper voltage and the corresponding inverter commutation is guaranteed to occur at lowest voltage; on the other hand, depending on the value of the inverter duty cycle, the falling edge will create a commutation of the inverter at a voltage that can be low or high. Figure 5(b) shows a similar analysis for a falling sawtooth. As a conclusion of these two figures, a rising (resp. falling) sawtooth carrier can guarantee an inverter voltage rising (resp. falling) edge at lower chopper voltage and the voltage at the falling (resp. rising) edge depends on the inverter duty cycle. However, it should be noted that the corresponding between rising/falling edge and IGBT turn-on/turn-off depends on the sign of the current.

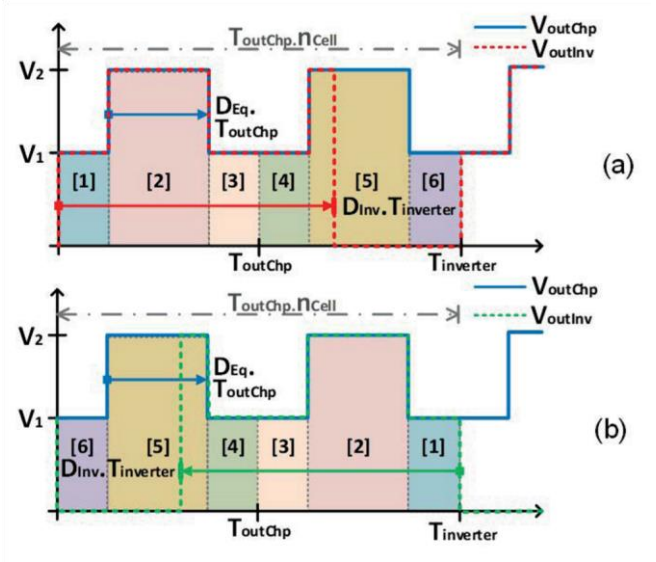

Fig. 5: Duty cycle evolution for rising (a)(red) and falling (b)(green) sawtooth carrier in function of chopper output voltage (blue) and number of chopper cells n_{cell}.

To develop the equations that link the inverter average output voltage V_{Inv} to the inverter duty cycle D_{Inv}, the chopper average output voltage V_{Chp}, its output voltage

levels V_1 and V_2, the chopper equivalent duty cycle D_{Eq} and the number of flying capacitor cells n_{cell} an example with 2 cells, i.e., a three-level flying capacitor, will be used. Developing those equations, the inverter duty cycle can be calculated for a generic case, no matter how many cells compose the flying capacitor. Inverter duty cycle is the same for either a rising or a falling sawtooth carrier.

$$V_{Inv} = \begin{cases} [1]\ D_{Inv} \cdot V_1 \\ \text{for} \quad 0 \le D_{Inv} \le \dfrac{1 - D_{Eq}}{2n_{cell}} \\ \\ [2]\ D_{Inv} \cdot V_2 + \dfrac{1 - D_{Eq}}{2n_{cell}} \cdot (V_1 - V_2) \\ \text{for} \quad \dfrac{1 - D_{Eq}}{2n_{cell}} < D_{Inv} < \dfrac{1 + D_{Eq}}{2n_{cell}} \\ \\ [3]\ D_{Inv} \cdot V_1 + \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) \\ \text{for} \quad \dfrac{1 + D_{Eq}}{2n_{cell}} \le D_{Inv} < \dfrac{1}{n_{cell}} \\ \\ [4]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_1 \\ \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} < D_{Inv} < \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \\ \\ [5]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_2 + \dfrac{1 - D_{Eq}}{2n_{cell}} \cdot (V_1 - V_2) \\ \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} < D_{Inv} < \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \\ \\ [6]\ \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{1}{n_{cell}} \right) \cdot V_1 + \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) \\ \text{for} \quad \dfrac{1}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \le D_{Inv} < \dfrac{2}{n_{cell}} \end{cases} \tag{1}$$

Equation (1)[1] corresponds to its respective zone on figure 3, i.e., to the zone where the inverter ontime is lower than half the equivalent off-time of the chopper on its first period. When the inverter on time exceeds it but is lower than one chopper period minus half the equivalent off-time of the chopper, i.e., it enters the zone 2, Eq. (1)[2] gives the corresponding output voltage. Furthermore, when the inverter on time exceeds the previous condition but is lower than one chopper equivalent period Eq. (1)[3] gives the output voltage. Additionally, if the inverter on-time exceeds one chopper period but is lower than one chopper period plus half the equivalent chopper off-time it enters the zone 4 where the equation Eq. (1)[4] gives the output voltage. The logic continues for an inverter on-time that evolves over the upcoming zones.

One should note that a term like the one given by Eq. (2) appears in the average output voltage equation when the inverter on-time exceeds one chopper period. It represents the contribution of the entire period of the chopper voltage on the inverter average voltage. The *lvl* variable gives the information of how much chopper entire periods are included in the inverter on time. *lvl* goes from zero to the number of choppers switching cells minus one and its mathematical definition is given by Eq. (3).

$$lvl \cdot \frac{V_{Chp}}{n_{cell}} \tag{2}$$

$$lvl = floor\left(\frac{V_{Inv}}{V_{Chp}} \cdot n \right) \cdot \frac{1}{n} \tag{3}$$

$$V_{Inv} = \begin{cases} [1]\ lvl \cdot \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_1 \\ \text{for} \quad \dfrac{lvl}{n_{cell}} \le D_{Inv} \le \dfrac{lvl}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} \\ \\ [2]\ lvl \cdot \dfrac{V_{Chp}}{n_{cell}} + \left(D_{Inv} - \dfrac{lvl}{n_{cell}} \right) \cdot V_2 + \\ \dfrac{D_{Eq}}{n_{cell}} \cdot (V_2 - V_1) \\ \begin{cases} \dfrac{1 - D_{Eq}}{2n_{cell}} * (V_1 - V_2) \\ \text{for} \quad \dfrac{lvl}{n_{cell}} + \dfrac{1 - D_{Eq}}{2n_{cell}} < D_{Inv} < \dfrac{lvl}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \end{cases} \\ \\ \text{for} \quad \dfrac{lvl}{n_{cell}} + \dfrac{1 + D_{Eq}}{2n_{cell}} \le D_{Inv} < \dfrac{lvl + 1}{n_{cell}} \end{cases}$$

(4)

Applying Eq. (3) on Eq. (1) it becomes generic for any number of chopper cells. Inverter duty cycle for any number of chopper cells is given by Eq. (4).

Figure 6(a) presents the result of the previous modulation when a falling sawtooth carrier is used. One can observe that the falling edge of switch $S9$ always occurs at a reduced voltage.

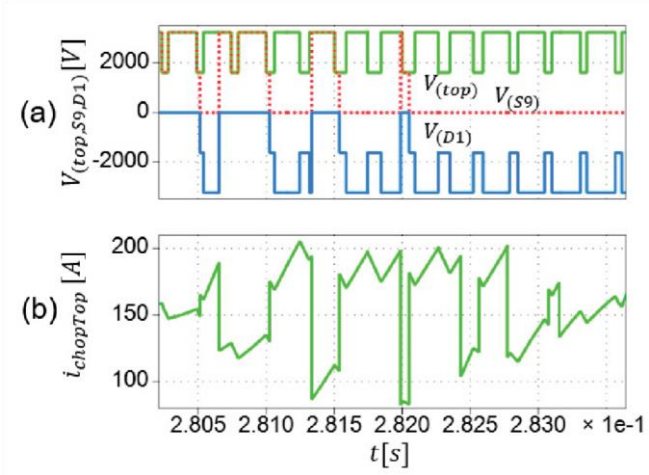

Fig. 6: Simulation waveforms of the 4.16 kV multiplexed converter operating with a DC-link voltage of 6.47 kV, a 1950 Hz switching frequency, an output frequency of 50 Hz, a rated output power of 0.67 kW and a RLE load (R=1%, L=15%). (a): Chopper output voltages, Vtop in green, $S9$ and $D1$ voltages in red and blue; (b): Top chopper output current.

3.3 Topology advantages

This topology characteristic, associated to its modulation, presents some advantages to face the limitation related to the HV semiconductors performance. First, the chopper semiconductors need to withstand only half of the bus voltage reducing their voltage ratings. Switching losses can be further reduced by using series connected IGBTs with a lower voltage rating; a higher chopper switching frequency can thus be used. On the other hand, the switching losses in the inverter can be significantly reduced because each semiconductor switches only during one sixth of the period (Fig. 7). Besides that, for a close to unity power factor, they switch only low current values (Fig. 7(g)). This allows a higher switching frequency for inverter semiconductors reducing their losses and increasing the efficiency.

Finally, even if the inverter legs need to withstand the entire bus voltage, they can do at least one of the commutations (turn-on or turn-off) at a reduced voltage. This is possible using a dedicated inverter modulation strategy that is a key factor for this topology. Figure 6(a) shows the semiconductor voltages where it is possible to observe that the IGBT turn-on commutations are done at reduced voltage.

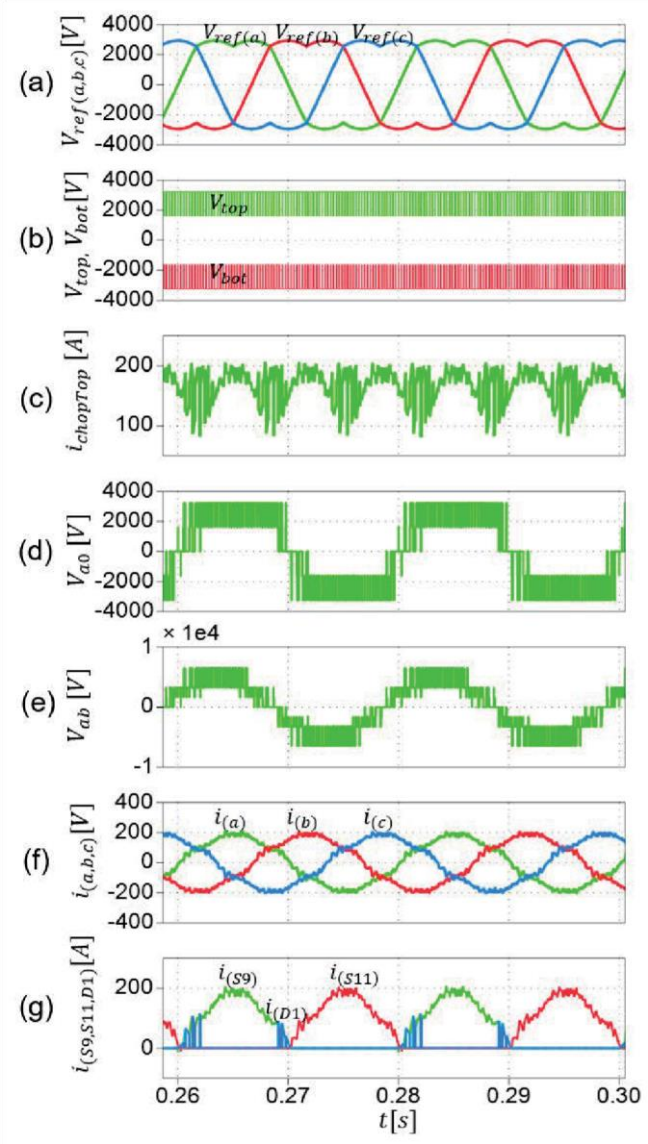

Fig. 7: Simulation waveforms of the 4.16 kV multiplexed inverter operating with a DC-link voltage of 6.47 kV, a 1950 Hz switching frequency, an output frequency of 50 Hz, a rated output power of 0.67 kW and a RLE load (R=1%, L=15%). (a): Grid reference voltages;

(b): Reference voltages; (c): Chopper output voltages, VTOP in green,

VBOT in red; (d): Multi-level voltage of the node A to the DC-link midpoint; (e): Multi-level voltage of the node A to the node B; (f): Output phase currents; (g): Current on semiconductors S9 (green), S11 (red) and D1 (blue).

4 Multiplexed Inverter and 5LANPC

This section will present a comparison between two inverter topologies for a 4.16 kV output voltage: the multiplexed inverter topology and the 5LANPC [6], one of the references in the market. For a fair comparison of the topologies, power switches with similar characteristics have been used whenever possible. To this extent ABB modules have been a good option because, their loss/thermal models are available and the 800 A current rating exist with different voltage rating. This is convenient when combining different voltage ratings within the same converter. For this comparison multiplexed inverter uses 4.16 kV IGBTs series-connected in the chopper and 6.5 kV semiconductors for the NPC. 5LANPC is composed by 3.3 kV IGBTs.

As seen in the previous section, multiplexed topology does concentrate switching losses on its chopper stage due to its operation principle. Therefore, for this comparison the 1.7 kV IGBTs have been associated in parallel to reduce overload of these switches and underused HV inverter semiconductors. Likewise, for a fair comparison, the most overloaded switches from the 5LANPC, i.e., the 4 switches of the FC chopper, are associated in parallel (Fig. 8).

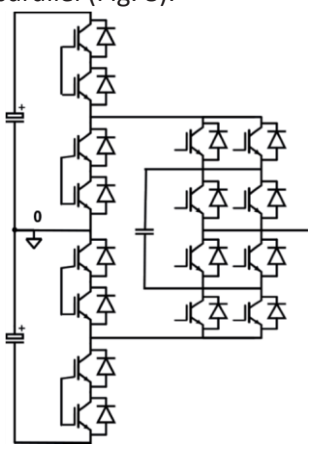

Fig. 8: ANPC-5L arm configuration used for comparison with multiplexed inverter for 4.16 kV output voltage . All IGBTs are rated at 3.3 kV and 800 A.

For each design and switching frequency the maximum power that can be delivered has been determined with PLECS® software simulations (Fig. 9(a)). Therefore, a temperature loop that acts over the output power is used [7], [16]. The heatsink temperature is set at 75°C and the highest of the average junction temperature is regulated at 105°C by the temperature loop. At the maximum output power point semiconductors efficiency has also been simulated and the results are presented in
Fig. 9(b).

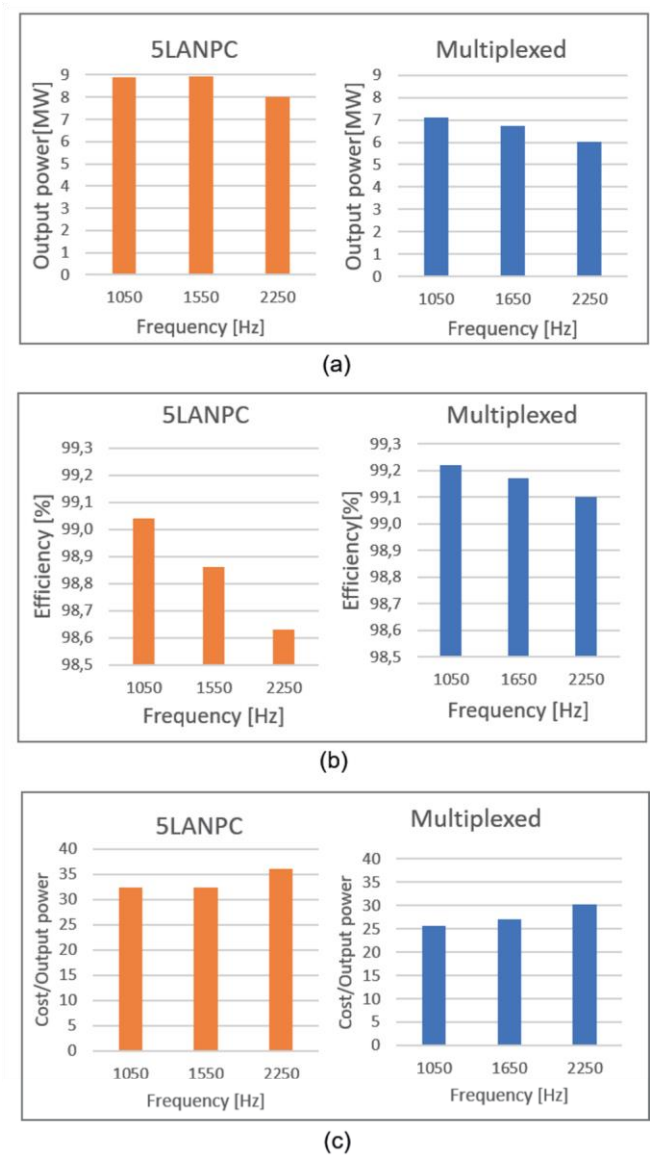

Fig. 9: Comparison between 4.16 kV (LANPC and multiplexed inverters: (a) Maximum output power in function of switching frequency for 800 A rated IGBTs; (b) Efficiency in function of switching frequency at maximum output power; (c) Cost per maximum

output power in function of switching frequency using relative price values from Table 1.

Another interesting comparison that can be realized is the semiconductors cost, main criteria of this study. For this comparison the relative cost per rated ampere (Fig. 1) has been used. The number of switches used for the maximum output power comparison are weighted by their relative cost and the results are presented on Table 1. Diode price is considered half of the IGBT price. For the 6.6 kV inverter either the 5LANPC and the NPC uses 4.5kV IGBTs. In the multiplexed converter those IGBTs are series connected. Figure 9(c) presents the cost per output power in function of switching frequency using the cost values from Table 1.

Figure 9 shows that multiplexed topology is less affected in terms of output power and efficiency by switching frequency increase than 5LANPC and presents a better overall semiconductors efficiency. However, one can observe that the multiplexed maximum power is inferior that the 5LANPC one for the same current rating of semiconductors. Nevertheless, if the price of semiconductors enters the comparison, even though with a lower output maximum power, the multiplexed topology presents a lower cost per output power.

Tab. 1: Component relative cost comparison between 5LANPC and multiplexed topology for 4.16 kV and 6.6 kV power drive.

	ANPC-5L		**Multiplexed**	
SC	4.16 kV	6.6 kV	4.16 kV	6.6 kV
1.7 kV	0	0	32	48
3.3 kV	288	384	0	0
6.5 kV	0	0	150	240
Total	**288**	**384**	**182**	**288**

5 Conclusion

In this paper, a new multilevel converter topology for power drives was proposed. This topology can reduce high-voltage semiconductors requirements due to its cascaded stages, where the inverters semiconductors switch only one sixth of the time. Most of the switching efforts are concentrated on the choppers that need to with stand only half of the bus voltage and are composed by low voltage IGBTs that have much better switching performances. Moreover, the fact of cascading inverter and choppers without intermediate filtering associated to a dedicated modulation leads to a reduction of the voltage switched by the inverter, thus reducing the switching losses. For low modulation depth zero voltage commutation is even possible. These features enable a relatively higher switching frequency increasing efficiency and overall semiconductors cost when compared to 5LANPC. An appropriate control strategy and modulation for this new topology dedicated to power drives has been presented. Simulations realized on PLECS® software have presented good results showing the topology performance that should be reflected on a future prototype.

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