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# Distributed Control for the Current Balancing of a Multiphase Converter using a Single Voltage Sensor

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## Abstract

This article presents a method of current balancing for a multiphase converter using a single voltage sensor. This control approach uses the ripple measurement of the input voltage to determine the current unbalance. It uses local controllers associated with each switching-cell and allows current balancing to be performed in a distributed manner by implementing simple and identical computations in each one of them. The results obtained on a 3-phase 300V/60A converter demonstrate the robustness of the control. This approach can be generalized to any multiphase converter using a large number of phases.

## 1 Introduction

Nowadays, DCDC multiphase converters are widely used in several applications and power ranges because of their advantages. The interleaving PWM modulation generates the effect of multiplying the apparent switching frequency by the number of cells ( $N$ ) both at the input and output of the converter. The increase in ripple frequency and the resulting reduction in amplitude minimize the input and output filter requirements and also contribute to reduce the switching losses. Consequently, higher efficiency and higher power density are obtained. Moreover, the shrink of the passive filters improves the dynamical performance of the converters. Multiphase converters present further advantages such as redundancy, reconfigurability, fault tolerance and the capability of phase shedding, i.e. individual cells can be enabled or disabled depending on the load power demand reducing losses and increasing system lifespan.

However, in terms of control complexity, these multiphase converters present more signals to be

measured and manipulated. An important drawback is the need of guarantying the power sharing between the different converter legs in

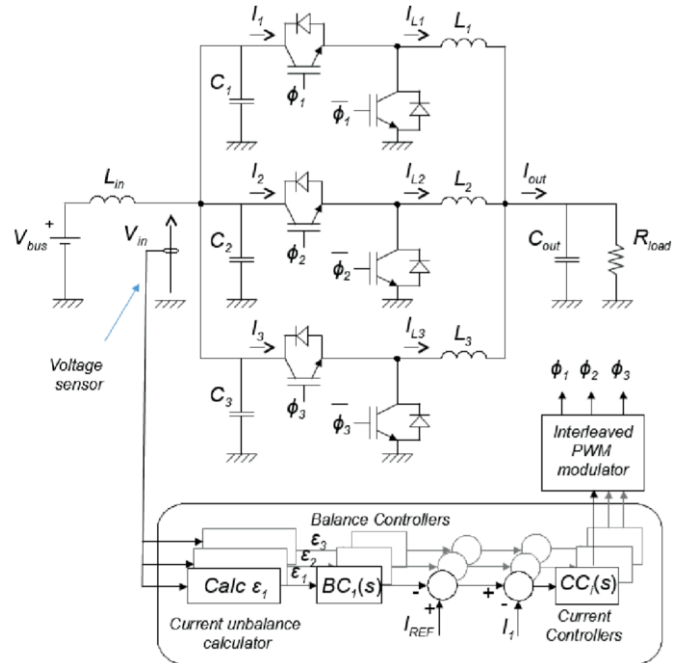


Fig. 1: Multiphase DC-DC buck converter ( $N=3$ )

order to maintain the components under secure operating conditions in what concerns thermal, mechanical and electrical stresses. In other terms, the currents of the converter legs must be balanced. This study focuses on  $N$ -leg multiphase parallel buck converters as the one presented in Fig. 1. The balance in the individual leg currents can be affected by even small variations in the pulses sent to switches or electrical parameters. If individual current sensors are used in the converter legs to measure the inductor's currents, offset or sensibility mismatches may affect the accuracy of the control and leads to a current unbalance also.

Several balancing methods have been already presented in the literature such as the standard centralized balancing using a central controller and one current sensor per leg [1], or a distributed balancing using local controllers and one current sensor per leg

[2-6] or even a balancing method using a single current-sensor [7,8]. All of them require at least one current sensor which is either inaccurate for low DC current level or an intrusive, expensive sensor presenting a limited bandwidth. It should be noted also similar distributed balancing strategies are implemented to insure the power sharing in serial multilevel converters [9-11].

This study presents a strategy to simplifying the active current balance control in a parallel  $N$ -leg buck converter. The originality of our approach consists in using the information contained in the ripple of the input voltage of the converter to determine the current imbalance to be corrected. Although this balancing approach could be used in classical centralized control, a distributed algorithm has been prioritized due to its modularity potential. This means that  $N$  local controllers (LC) are responsible for current regulation

and each LC receives its own relative reference correction to allow the system to balance all of its leg currents. This type of distributed control obtained makes it possible to simplify the implementation of the control using only one single large-bandwidth voltage sensor, allows to easily add or remove active phases thanks to the distributed approach and to manage any large number of converter legs.

## 2 Distributed Current Balancing Method

By considering the circuit schematic of a multiphase converter shown in Fig. 1, it is observed that the collector currents of the high-side switches  $I_1$ ,  $I_2$  and  $I_3$  all sum up at the same node to make a current called  $I_{in}$  (not shown in the figure).

$$I_{in}(t) = \sum_{i=1}^N I_i(t) \quad (1)$$

Capacitors  $C_1$  to  $C_3$ , dedicated to the local decoupling of each switching-cell, are placed in parallel as seen from the input node and constitute an equivalent input capacitance called  $C_{in}$ . Basically, the DC component of the current

$I_{in}$  is supplied by the inductor  $L_{in}$  while the AC component of this current flows through the capacitor  $C_{in}$ . Fig. 2a) shows the waveforms of the signals  $V_{in}$  and  $I_{in}$  in the case of a balanced interleaved

system. It is observed that the signal  $I_{in}$  is made up of high and low current levels whose values depend on the currents  $I_1$  to  $I_3$  or a linear combination of these currents according to the value of the duty-cycle  $D$ .

When this duty-cycle is less than  $T_{sw}/N$ , with  $T_{sw}$  the switching period, the signal  $I_{in}$  is similar to the one shown in Fig. 2a) and each level represents the value of a leg current. It is important to note that in order to simplify the description of the control method, the leg current ripple is considered negligible. This is not true in practice and the average value of the leg current is reached at the middle of the control signal pulse (see times  $t_1$  to  $t_3$ ). Usually, the duty-cycle can be expressed as:

$$D = D_{root} \bmod k/N \quad (2)$$

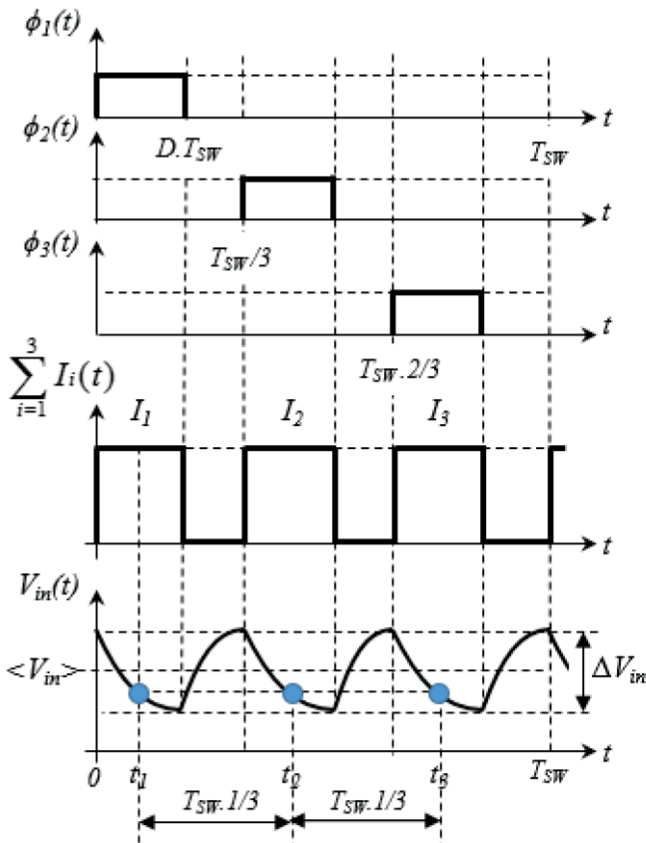
where  $k = 0 \dots N - 1$  and  $0 \leq D_{root} < 1/N$ .

Considering  $k \geq 1$ , several cases must be considered depending the value of the levels reached for  $I_{in}$ . In this article, and for the sake of clarity, only the case  $k = 0$  is considered.

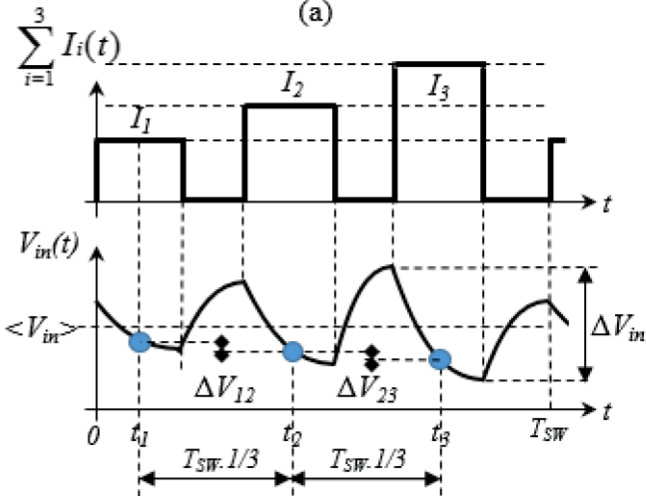
### 2.1 Time-delayed measurement

Fig. 2a) shows the waveform of the input signal  $V_{in}$  in the case of a balanced system. This

signal consists of a DC component imposed by the bus voltage  $V_{bus}$ , and an AC component  $V_{inAC}$  depending on the AC component of the current  $I_{in}$ . It can be assumed:



(a)



(b)

Fig. 2: a) Balanced b)Unbalanced leg currents principle of the

LC considers as a time reference the middle of the pulse of its own PWM control signal.

$$V_{in}(t) = V_{bus} + V_{inAC}(t) \quad (3)$$

with

$$V_{inAC}(t) = -\frac{1}{C_{in}} \int I_{inAC}(t)dt - R_{ESR} \cdot I_{inAC}(t) \quad (4)$$

where  $R_{ESR}$  is the equivalent serial resistance of the equivalent capacity  $C_{in}$ , i.e. taking into account the ESR of the capacitors  $C_1$  to  $C_3$ .  $R_{ESR}$  will be considered negligible at first.

It should be noted the signal is symmetrical with a frequency equal to  $N * f_{sw}$ , with  $f_{sw} = 1/T_{sw}$  the switching frequency and  $N = 3$ . If  $N$  samples, all spaced apart by a duration  $T_{sw}/N$ , are taken,

whatever the starting time considered, the level of these samples will be equal. On the other hand, this is not the case if one considers an unbalanced system. Indeed, Fig. 2b) shows the case of a multiphase with  $I_1 < I_2 < I_3$ . Because the current levels reached are different, the AC component of the signal  $V_{in}$  now shows peaks and valleys

with different levels. The harmonic frequency  $f_{sw}$  appears. Therefore, if  $N$  samples are taken, all spaced apart by a duration  $T_{sw}/N$ , their values will be different and the differences obtained will depend on the current imbalance.

## 2.2 Control algorithm

In order to set up a distributed control system, it is proposed to involve with each leg of the converter a specific LC. Each LC consists of a current unbalance calculator (obtained from the input voltage measurement), a balance controller (BC) and a current controller (CC). All LCs are identical and implement the same calculation algorithm. The

distributed balancing consists of ensuring that each LC takes  $N$  samples from the signal  $V_{in}$  as follows:

- Each LC considers the signal  $V_{in}$  in a relative manner with respect to its own phase, i.e. each

- E
- a
- c

$$\epsilon_i = \sum_{k=1}^{N-1} [V_{in}^*(t_i) - V_{in}^*(t_i + \frac{k}{N}T_{sw})] \quad (5)$$

where  $\epsilon_i$  is the local error of the  $i^{th}$  LC,  $t_i$  is the time reference of the LC considered,  $k$  is the sample rank and  $V_{in}^*(t_i)$  is the sample at time  $t_i$ .

In order to cancel out the calculated errors, each LC implements a corrector through the BC that makes the necessary changes in the current reference ( $I_{REF}$ ) in order to minimize the voltage ripple variation, that is the current unbalance. Both BC and CC are proportional-integral controllers. Finally, by the use of an interleaved PWM modulator, the control signals  $\phi_1$  to  $\phi_N$  of the switching-cells are generated.

Fig. 3 shows the simulation results obtained. A 50% balancing error is introduced producing the currents  $I_1 = 60A$ ,  $I_2 = 120A$  and  $I_3 = 140A$ . The waveform of the  $V_{in}$  signal is periodic, it involves the fundamental frequency  $f_{sw}$  and its peaks and valleys present different levels. After enabling the distributed balancing control, the currents are perfectly balanced and the fundamental frequency  $f_{sw}$  on signal  $V_{in}$  is canceled out.

### 3 Experimental validation

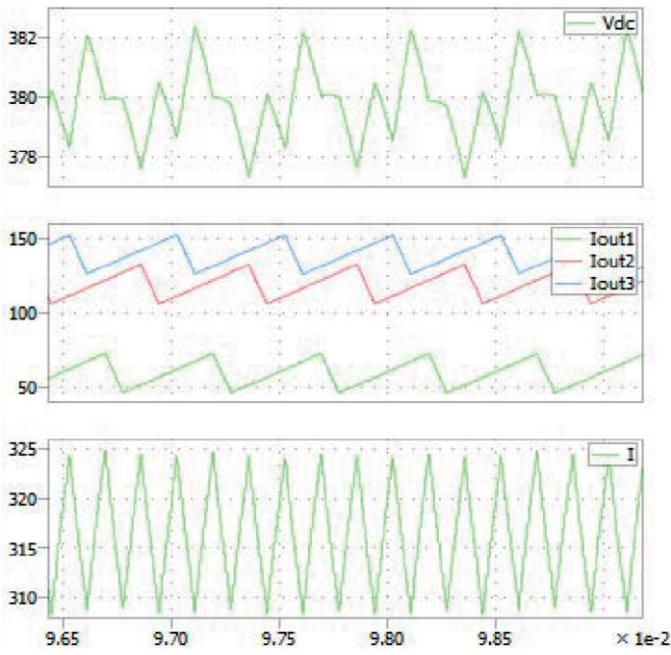
In order to confirm the relevance of the proposed current balancing algorithm, the control strategy has been implemented in a 3-leg multiphase DCDC buck converter. Fig. 4 shows a photo of the prototype used in the laboratory.

The converter is made of IGBT modules 2MBI300VB-060-50 from Fuji Electronics. Main converter parameters are summarized in Table 1. In order to generate the control laws of the converter cells, the platform RT-box 1 coupled to the PLECS simulation tool is used.

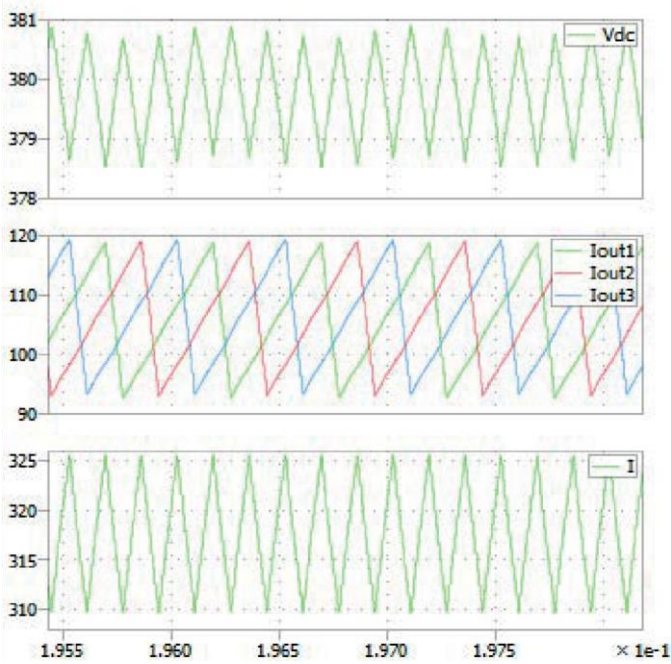
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N  
.

Therefore, each LC will be able to calculate its own local error to cancel by performing the following calculation:

correction is applied. The test of the algorithm was accomplished by forcing an imbalance of the



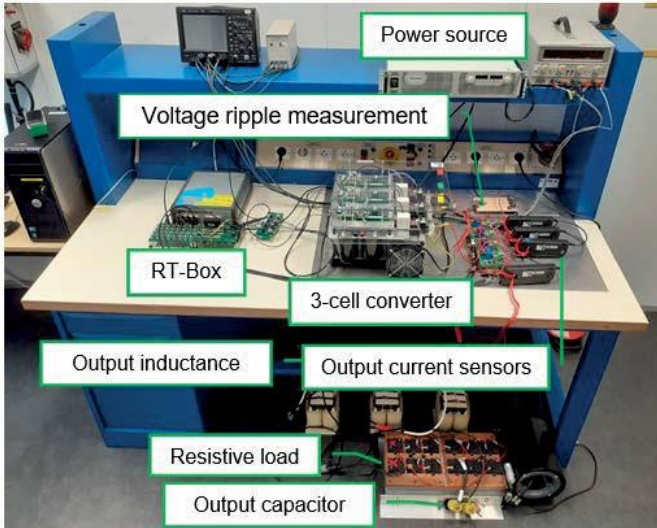
(a)



(b)

**Fig. 3:** Simulation of the input voltage, the converter leg currents and the output current under 50% current unbalance with a) the balancing control disabled and b) enabled

Fig. 5 illustrate the control method performance showing a unbalanced system before and after the



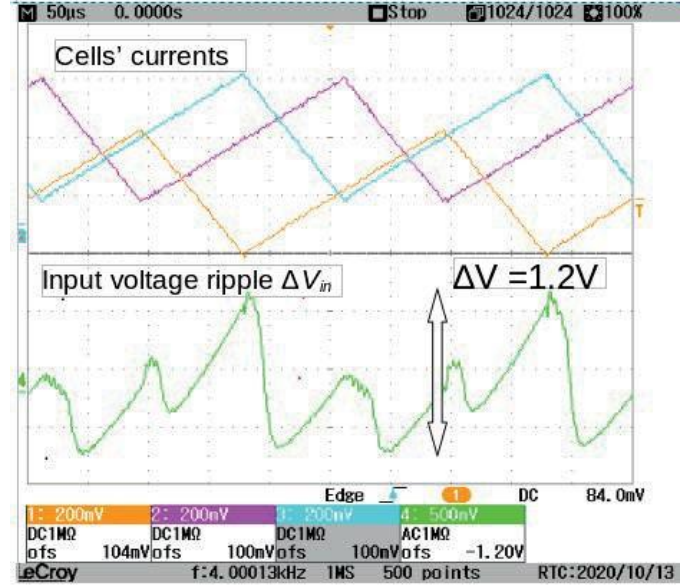
**Fig. 4:** Prototype of a 3-leg multiphase DC-DC buck converter

**Tab. 1:** Test bench parameters

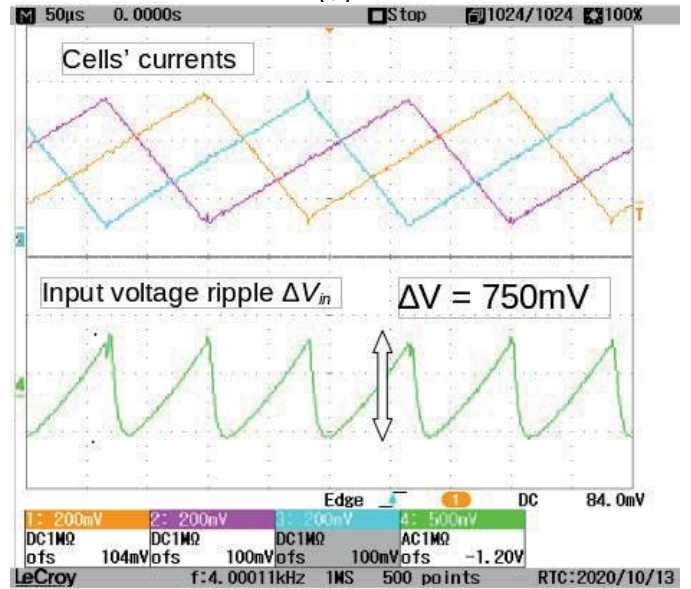
Input Voltage ( $V_{in}$ )	100 V
DC-link capacitance ( $C_{1-3}$ )	13.2mF
Output filter inductance ( $L_{1-3}$ )	650uH
Output filter capacitance ( $C_{out}$ )	2.5uF
Load resistance ( $R_{load}$ )	5 Ohm
Current sensor	LA 55-P (LEM)
Switching frequency ( $f_{sw}$ )	4 kHz
ADC conversion	12 kHz

the legs, while the two others were kept with correct currents by a deliberate variation of the gain of an analog-to-digital conversion (ADC) ( $K_{adc}$ ) in one of

values. For instance, in Fig. 5a) an intentional error of +20% has been added in the measurement of the current  $I_1$ . The unbalance is reflected in the asymmetrical and relatively high ripple of 1.2V on  $V_{in}$ . Activating the balancing control algorithm, each LC takes three samples  $T_{sw}/3$  apart on signal  $V_{in}$ , and computes the local error to compensate. Local duty-cycle corrections are obtained and current errors are cancelled out. The result is presented in Fig. 5b) where an error of 20% in  $K_{adc}$  for the first current measurement has been imposed. As shown in the figure, the LCs adjust their current references in order to eliminate the asymmetry on the DC-link ripple.



(a)



(b)

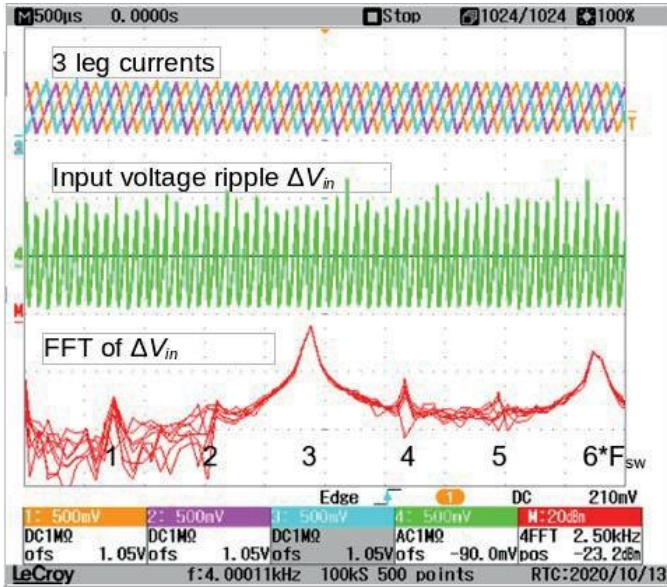
Consequently, the currents are balanced and the ripple is significantly reduced to 0.75V for the same operation condition.

**Fig. 5:** Converter leg currents and input voltage under 20% current unbalance with a) the balancing control disabled and b) enabled

It is also important to notice the useful information included in the harmonic spectrum of  $V_{in}$ . Under unbalanced current conditions, during a full period of switching, the input capacitor voltage waveform with



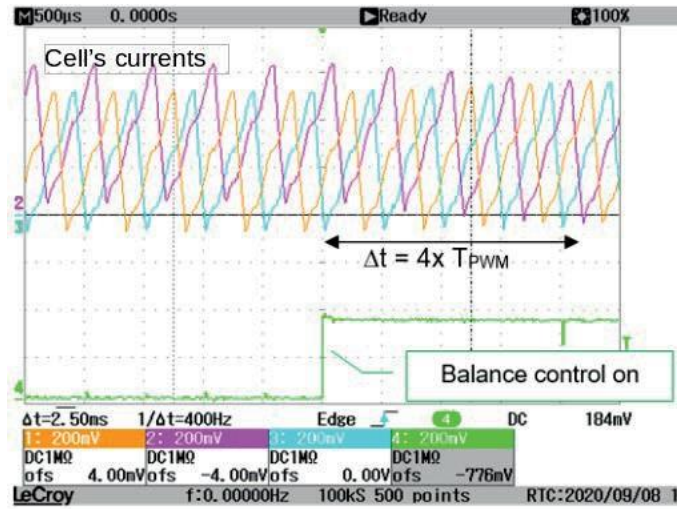
$N$ -times  $f_{sw}$  is always present, the fundamental at the switching frequency  $f_{sw}$  only appears for cases of current imbalance. However, under balanced current condition, all the turn-off event transitions will present a identical level for  $V_{in}$ , so its waveform will present  $N$  identical valleys during a full period of switching. The fundamental spectral line at  $f_{sw}$  no longer exist and is cancelled out.



different charge and discharge rates presents different slopes. The negative slope will be more aggressive if the current related to the ON-state switch is higher. This means that the voltage  $V_{in}$  will present the lowest value during the turn-off of this particular switch. If the apparent frequency at

**Fig. 6:** Leg currents,  $V_{in}$  and FFT of  $V_{in}$  with an measurement error of -10% in  $K_{ADC}$  with the BC enabled.

The harmonic spectrum of the signal  $V_{in}$  is presented in Fig. 6. The leg currents and the input voltage are shown for a system with an initial unbalance condition of 20% and an enabled balancing control (BC) algorithm. The leg currents are all equal and interleaved. The FFT of the  $V_{in}$  waveform is plotted with an frequency span from 0 to the sixth harmonic of  $f_{sw}$ . It is remarkable to consider the low contribution of  $f_{sw}$  in the harmonic spectrum: its value is 25 dB lower than the third harmonic, which is the apparent switching frequency ( $N \times f_{sw}$ ). The fact that only the harmonic at the apparent frequency ( $3 \times 4kHz = 12kHz$ ) presents a preponderant contribution in the FFT of the signal  $V_{in}$ , indicates the good performance of the proposed algorithm.



**Fig. 7:** Dynamical response of the leg currents during the BC startup.

possible to achieve a fast dynamic response, i.e. only few periods of switching. The BC is enabled with a condition of -10% of current unbalance in  $K_{adc}$  of current  $I_1$ . After 4-times the PWM period ( $4 \times T_{sw}$ ) the system is able to converge towards the appropriate steady state achieving the balancing of the 3 leg currents.

Finally, Fig. 7 presents the dynamic response of the BC. It is important to mention that the dynamic analysis of the proposed algorithm is not the object of this article. Nevertheless, Fig. 7 shows it is

## 4 Conclusion

A control method dedicated to balancing the leg currents of a multiphase converter has been presented. The main advantage of this method is that it requires a single voltage sensor to calculate the current imbalance for any number of converter legs. Indeed, the input voltage ripple signal contains all the necessary useful information. With samples taken from this voltage signal, local leg controllers are able to compute in a distributed manner the appropriate local duty-cycle corrections to balance the currents.

A 3-leg 300V/60A multiphase prototype has been carried out to demonstrate the relevance and the robustness of the proposed control method.

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