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# Design Aspects for Achieving High Bandwidth Series and Parallel Multicell Converters

Victor Flores Mendes, *Member, IEEE*, Guilherme Monteiro de Rezende, Tiago de Sá Ferreira, *Member, IEEE*, João Lucas da Silva, Jérémi Régnier, *Member, IEEE*, and Thierry A. Meynard, *Fellow, IEEE*

**Abstract**—Series and parallel multicell converters (SMCs and PMCs) have been conventionally used in high-voltage and high power applications. Recently, due to the improved efficiency with the increase of the number of cells, they are also applied in small power converters with high power density. The higher the number of cells, the higher the apparent switching frequency, so the filter requirements are reduced, which means less energy is stored in the passive components. This potentially allows for faster dynamic responses in closed-loop operation, i.e., higher bandwidth of the converters. This article highlights the filter design and the importance of using an appropriate modulator for SMCs in order to reach high bandwidths, mainly when the number of cells increases. It is underlined, through a comparison with PMC, that SMC topologies are more sensitive to the modulation strategy. SMC and PMC performances of 2-kW converters are evaluated and compared through simulations implemented in software PLECS and validated using an experimental test bench.

**Index Terms**—Fast control, flying capacitors, high bandwidth converters, modulation, multilevel converters.

## I. INTRODUCTION

The multilevel converter is not a recent technology, but its industry application has grown mainly in the last decade. There is a wide range of applications, as electrical drives in general, reactive power compensators, high-voltage direct current transmission, wind energy conversion systems, energy storage

systems, and several high-power high-voltage applications [1]. Different topologies of multilevel have been proposed in the literature: neutral point clamped (NPC) and flying capacitor (FC) with their variations; cascaded topologies as cascade H-bridge (CHB) and modular multilevel converters (MMC) [2], [3].

Among the multilevel converters, of particular interest, are the ones that present a multicell structure, i.e., a modular topology in which the cells with smaller power can be combined to form higher converter power. FC, CHB, and MMC are examples of multicell converters.

Instead of using the multicell converters to reach higher powers, it is possible to combine the cells in order to have faster dynamics of current and voltage. Increasing the number of cells ( $n_{\text{cell}}$ ) means increasing the number of voltage levels of the converter output and, consequently reducing the filter requirements (smaller inductance and capacitance) in comparison to a two-level counterpart [4]. Therefore, converters with higher bandwidth may be expected and applied to systems that need fast responses [5].

Another way of increasing the system bandwidth is using interleaved converters, also known as multiphase or parallel

multicell converters (PMCs). In this case, the voltage levels are the same whatever the number of cells, but with the proper phase shifted modulation between the cells, the perceived switching frequency in the output of the converter increases with the number of cells. Therefore, the filter requirements are also reduced, and higher bandwidths can be attained [6].

High bandwidth interleaved converters were initially employed as dc/dc voltage regulators to supply microprocessors that present high current demands under low voltage and fast dynamics [7]. Recently, other applications have been taking advantage of their fast response, as radio frequency power amplifiers [8], aeronautical applications [9], automotive converters, battery chargers [10], among others.

Multilevel converters can be connected in parallel with their control interleaved in order to take advantage of both principles and to increase even further the system bandwidth. For example, Gleissner and Bakran [11] and Konstantinou *et al.* [12] present the interleaved operation of FC and NPC converters, respectively.

Another obvious way of decreasing the filter requirements and expanding the converter bandwidth is the utilization of high switching frequencies ( $f_{\text{sw}}$ ). Nowadays, frequencies of hundreds of kilohertz can be used, employing wide bandgap devices (WBD), commonly SiC and GaN transistors [13].

Several applications can benefit from the high switching frequency as low-inductance motors and high-speed motors drives [14].

By employing WBD in multilevel interleaved converters with the proper filter design, it is possible to reach high power density and ultra-high bandwidths. In [15], the project of an interleaved FC converter with GaN devices for automotive application with the purpose of high efficiency and power density is proposed. In [16], an interleaved FC converter is designed to have a high bandwidth converter (HBC). An impressive apparent switching frequency of 4.8 MHz is employed with the converter being designed for a bandwidth of 100 kHz.

An important point for HBC is the modulation technique. New modulation strategies have been developed for years, but the carrier-based modulations are still the most employed [17]. The symmetrically sampled PWM (SSPWM) and the asymmetrically sampled PWM (AS-PWM) are widely employed. In such PWM schemes, the cell duty cycles are computed and updated once (top OR bottom of the carrier) or twice (top AND bottom of the carrier) per switching period. In multicell converters, in order to take advantage of the higher output apparent switching frequency ( $n_{\text{cell}} \cdot f_{\text{sw}}$ ), the cell duty cycles can be computed by the control at this apparent

frequency. This concept is known as multisampling technique and, theoretically, the control can be faster and the higher the  $n_{\text{cell}}$ . However, the sampling is generally synchronized with the carriers of the cells, as in the SS and AS-PWMs [18]. Therefore, each cell duty cycle is updated only twice per switching period in the best case. This sampling process decreases the modulator gain and introduces delays that hinder the control action [4], [19]–[21].

In a naturally sampled PWM (NS-PWM), the converter duty cycles are updated immediately, i.e., they are not synchronized with the carriers. Therefore, the response of the modulator is enhanced, making it suitable for multicell converters [19]. The drawback of the NS-PWM is the overswitching, i.e., the semiconductor may switch ON/OFF more than once per switching period, which can increase the converter losses and even damage the semiconductors. Yang *et al.* [20] apply the NS-PWM combined with the multisampling technique in such a way that the duty cycles of all cells are updated at the same time. The authors named the concept as multirate technique and the overswitching is avoided using an FPGA to modify the converters pulses after the PWM generation.

Using a similar approach, de Sá Ferreira *et al.* [21] propose a multirate modulator that is easily implemented digitally. The article demonstrates for PMCs the superior dynamic performance of the multirate modulator compared to the SS- and AS-PWMs with the multisampling technique presented in [18]. The multirate presents a similar behavior when compared to NS-PWM, proposed by [20], with the advantage of avoiding overswitching in the algorithm implemented in the control platform, i.e., no extra equipment as an FPGA is needed. Furthermore, the algorithm is generalized for any number of converter cells combined in series and/or parallel.

The present article intends to extend the analysis presented in [21], evaluating the response of series multicell converter (SMC) based on FC when the multirate modulator is employed. It is demonstrated that the improvement in the SMC response with the multirate modulator can be significantly higher than in PMC. Furthermore, a comparison between bandwidth (rapidity of response) of SMCs and PMCs with various numbers of cells is presented. The analysis is carried out through simulations using the software PLECS and validated using a 2 kW dc/dc SMC prototype.

The main contribution of this article is the analysis of the modulator and output filter characteristics in PMC and SMC with the objective of design HBCs. It is shown that, for the same design restraints (current and voltage ripples, size, etc.), the intrinsic differences of the output filters of the PMC and the SMC lead to completely different dynamic behavior. It is also shown that this, in conjunction with the utilization of the multirate modulator in combination with a state space feedback control, increases the converter bandwidth considerably. Unlike usual approaches that employ small signal analysis, this article focuses on large signal performances of the converters (voltage step from 10% to 90% of input voltage), which means that saturation is implicitly involved. The design filter, the multirate

modulator, and the large signal analysis present a different investigation of the design of HBC that does not necessarily involve the most common approaches, such as using WBD or raising the switching frequency.

The rest of this article is organized as follows. Section II presents details of the filter designed for PMC and SMC. Section III describes the control strategy and the multirate modulator employed in this article. Section IV presents the results of the multirate modulator applied to SMC. Section V compares the responses of PMC and SMC. Finally, Section VI concludes this article.

## II. MULTICELL CONVERTERS FILTER CHARACTERISTICS

Fig. 1(a) and (b) depicts the structure of generic  $n_{\text{cell}}$  PMC and SMC based on FC, respectively. Fig. 1(c) shows the parallel combination of two three-cell SMCs. These figures represent the connection of dc/dc converters, but it is possible to have dc/ac converters connecting the load (point B) to the dc-link middle point (point A), instead of the negative part of dc link. This possibility allied with variation of series–parallel cells makes the multicell structure very versatile.

Another important aspect of SMC and PMC is their duality [22]. For the same number of cells, if the equivalent output filter is the same, the current and voltage output behavior is the same. Nevertheless, the filter design rules may be different in these converters. The filter is a key point in the project of HBC; thus, this section presents the aspects of the filter design adopted.

### A. Filter Design

de Sá Ferreira *et al.* [21] present a generalized equation of the total output current ripple of multicell series–parallel converters using an interleaved modulation

$$\Delta I_{pkpk}^{\text{total}} = V_{\text{HV}} / (4 \cdot L_f \cdot f_{\text{Sw}} \cdot n_{\text{cell}}^2) \quad (1)$$

$$L_f = L_{\text{LV}} / n_p \quad (2)$$

$$n_{\text{cell}} = n_s \cdot n_p \quad (3)$$

where  $L_{\text{LV}}$  is the cell filter inductor,  $L_f$  is the equivalent filter inductor (low-voltage side),  $V_{\text{HV}}$  is the voltage in the high-voltage side of the converter (input),  $f_{\text{Sw}}$  is the switching frequency, and  $n_p$  and  $n_s$  are the number of cells in parallel and series, respectively. It is defined here the apparent switching frequency  $f_{\text{sa}} = n_{\text{cell}} \cdot f_{\text{Sw}}$ .

One of the objectives of the use of multicell converters maybe the reduction of the size, cost, and losses of the inductors. Furthermore, in order to design HBC, a low value of the equivalent inductance is required. Obviously, a high value of inductance results in bulky inductors, but it is also true that very small inductance means very high current ripple, which would also lead to inductors of great volume [23], [24].

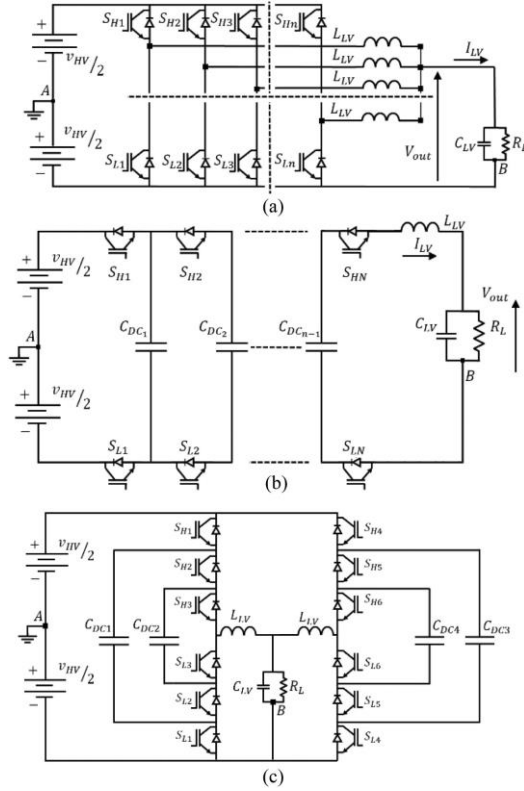


Fig. 1. (a) Generic  $n_{cell}$  parallel multicell converter. (b) Generic  $n_{cell}$  series multicell converter. (c) Series-parallel multicell converter (two parallel, three series).

Equation (1) shows that the current ripple in the output of the converter is the same when the cells are connected in series and/or parallel. If the equivalent filter inductor  $L_f$  is the same in the SMC and PMC, the output dynamic behavior of voltage and current are the same in both converters. Nevertheless, since the cell inductor current ripple in the parallel case is  $\Delta I_{pkpk}^N = n_p \cdot \Delta I_{pkpk}^{total}$ , if the same  $L_f$  is used in the SMC and PMC, the inductor current ripple for the latter may be much higher, consequently the inductors volume would be higher. Therefore, one can conclude that it is not interesting to design the same  $L_f$  for PMC and SMC with the same number of cells.

Defining the maximum inductor current ripple ( $\Delta I_{pkpk}^N$ ), the inductance per cell can be calculated as [21]

$$L_{LV} = \left( \frac{n_p}{n_s^2} \right) \cdot V_{HV} / (4 \cdot \Delta I_{pkpk}^N \cdot I_{LV} \cdot f_{sw}) \quad (4)$$

where  $I_{LV}$  is the converter total output current. One can see that the inductance is directly proportional to the number of cells in parallel and inversely proportional to the square of the cells in series. This means that the equivalent inductance for the PMC is constant whatever the number of cells, (2) and (4), while it drops quadratically with the number of cells in SMC.

TABLE I

FILTER PARAMETERS:  $V_{HV} = 100V$ ,  $I_{LV} = 20A$ ,  $f_{sw} = 20kHz$ .

$n_{cell}$		1	2	3	4	5	6	7
$C_{LV}$ ( $\mu F$ )	PMC	75	9.3	2.8	1.17	0.6	0.35	0.2
	SMC	75	37.5	25	18.8	15	12.5	10.7
$L_{LV}$ ( $\mu H$ )	PMC	208	416	625	833	1041	1250	1458
	SMC	208	52	23.1	13	8.3	5.8	4.2

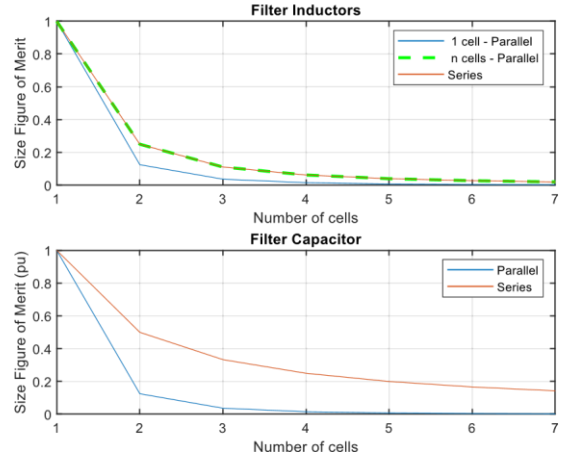


Fig. 2. Estimation of inductor and capacitor filter sizes.

With this design rule, the ripple of the output converter voltage ( $\Delta V_{pkpk}^N$ ) is restricted by the filter capacitor  $C_{LV}$ , which can be calculated as [21]

$$C_{LV} = \left( \frac{1}{n_s \cdot n_p^3} \right) \left( \frac{I_{LV}}{V_{HV}} \right) \cdot \left( \frac{\Delta I_{pkpk}^N}{\Delta V_{pkpk}^N} \right) \cdot \frac{1}{8 \cdot f_{sw}} \quad (5)$$

In this article, the maximum ripples are defined as  $\Delta I_{pkpk}^N = 30\%$  and  $\Delta V_{pkpk}^N = 0.5\%$ . Table I gives the filter parameters calculated for both topologies and considering a converter input voltage  $V_{HV} = 100 V$ , maximum output current  $I_{LV} = 20 A$  ( $R_L = 5 \Omega$ ), and switching frequency  $f_{sw} = 20 kHz$ . These parameters are used throughout this article.

### B. Filter Size Analysis

An idea of the filter size can be approximated by two figures of merits:  $L \cdot I_{pk} \cdot I_{rms}$  for the inductor and the stored energy  $0.5 \cdot C \cdot V_{out}^2$  for the capacitor [23], [24]. Considering the values of these figures of merits for a single cell converter as the base values, Fig. 2 shows the estimated relation between the sizes for the filters in Table I. One can see that, although the equivalent output inductance is different, the relation between the inductor

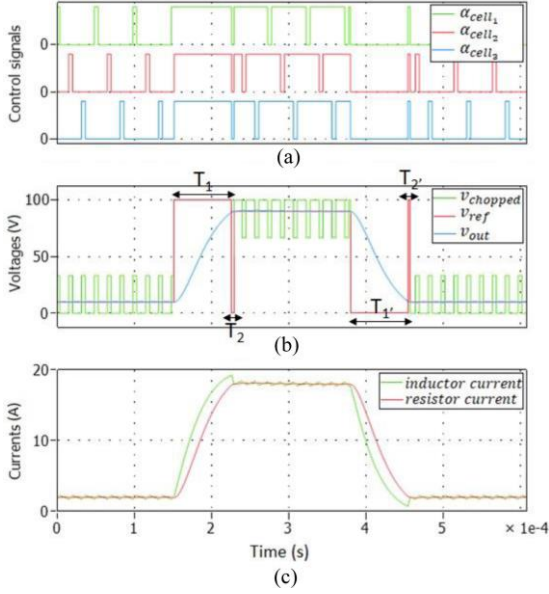


Fig. 3. Optimal response of the output filter for a three-cell parallel converter with  $R_L = 5\Omega$ : (a) command signals, (b) reference voltage, cell voltage, output voltage, and (c) cell current (inductor) and output current (load) [21].

size in PMC and SMC tends to be equal. As the output converter current ripple is smaller in PMC, its capacitance and consequent volume tend to be much smaller than the SMC. Of course, this is a rough approximation, but as the inductors generally are bigger and heavier than the capacitors, the filter volume and weight tend to be similar in both topologies.

A deeper analysis of filter sizing/construction is out of the scope of the present article. The aim of this discussion is to establish general design rules to allow a fair comparison between PMC and SMC in terms of bandwidth.

### C. Physical Limits for Filter Dynamic Response

It is easy to understand that the fastest converter response occurs when the power flowing from the dc link to the load is maximized. This is mainly limited by the input voltage ( $V_{HV}$ ) and the output filter characteristics. Therefore, an ideal control of the converter delivers the maximum output voltage (100%) for a first time interval  $T_1$ , then 0% for a time interval  $T_2$  to avoid voltage overshoot and, finally the final voltage is applied to keep the output voltage at the targeted value. Fig. 3 shows an example for the target voltage varying from 10% to 90%.

de Sá Ferreira *et al.* [21] demonstrate how to calculate numerically the values of  $T_1$  and  $T_2$ , consequently a “optimal time response” ( $t_{opt}$ ) of the filter. Nevertheless, this calculation is not trivial and hard to implement in a microprocessor to control a multicell converter. Furthermore, this  $t_{opt}$  does not consider real control, neither the modulation. Therefore, in the present article, the results of  $t_{opt}$ , calculated as in [21], are used for the sake of comparison with the responses of the SMC and PMC.

## III. CONTROL AND MODULATION OF MULTICELL CONVERTERS

### A. Control Strategy

In the highest level, the bandwidth of the converter depends on the control strategy. Several linear and nonlinear control strategies have been proposed in the literature with the objective of fast responses and/or robustness to parameters uncertainties, as predictive control [25]–[27], adaptive control [28], [29], geometric control [30], and variations of classical controls [31].

For multicell converters, the digital control performance can be enhanced with a multisample technique, i.e., the control and its variables are sampled at  $f_{sa}$  or  $2f_{sa}$  [18]. Even with today’s powerful microprocessors, the implementation of complex control strategies become unfeasible with increased number of cells and/or high switching frequencies. Therefore, in this article, the control is kept as simple as possible.

It is employed a state-space feedback control (SSFC), which is simple and well established [30]. It is easy to develop the state-space model of the equivalent filter as

$$\begin{bmatrix} \dot{I}_L \\ \dot{V}_{out} \end{bmatrix} = \begin{bmatrix} -\frac{R_L}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_{LV}} & \frac{1}{R_L C_{LV}} \end{bmatrix} \begin{bmatrix} I_{LV} \\ V_{out} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} V_{CM}, A_s C_s B_s y_{out} = [0, 1] \begin{bmatrix} I_{LV} \\ V_{out} \end{bmatrix} \quad (6)$$

and the common voltage imposed by the combination of the voltage cells is

$$V_{CM}(t) \approx \frac{V_{HV}}{n_{cell}} \sum_i^{n_{cell}} \alpha_{cell_i}(t) = V_{HV} \cdot \alpha_{CM} \quad (7)$$

where  $\alpha_{cell_i}(t)$  is the instantaneous cell duty cycle of the  $i$ th cell and  $\alpha_{CM}$  is the mean common mode duty cycle. Equation (7) applies to  $n_{cell}$  series–parallel converters, considering the input voltage constant and the FCs balanced, i.e., the cells capacitance are not taken into account in the model.

To be suitable for a closed-loop control, (6) is discretized at the control sampling time ( $t_{sample}$ ) using a zero-order holder approximation. The state-space model and its matrices are given by

$$x^{[k+1]} = A_d x^{[k]} + B_d V_{cm}^{[k]} y^{[k]} = C_d x^{[k]} \quad (8)$$

$$A_d = e^{A_s t_{sample}} \quad B_d = \left( \int_0^{t_{sample}} e^{A_s \tau} d\tau \right) B_s \quad C_d = C_s \quad (9)$$

$$\frac{t_{sample}}{t_{sample}} = \frac{1}{f_{sa}} \quad \text{for single sampled PWM} \\ \frac{t_{sample}}{t_{sample}} = 1/(2f_{sa}) \quad \text{for double sampled PWM} \quad (10)$$

The control sampling time is a function of the apparent switching frequency  $f_{sa} = n_{cell} \cdot f_{sw}$  in order to take advantage of the cell’s phase-shifted PWMs [6].

Due to the output feedback and integral action, there is a state augmentation. In this article, the bilinear integration (Tustin method) is used for the control discretization and the state-space model is described as follows:

$$x_I^{[k+1]} = x_I^{[k]} + [t_{\text{sample}}] e^{[k]} \quad y_I^{[k]} = x_I^{[k]} + \left[ \frac{t_{\text{sample}}}{2} \right] e^{[k]} \quad (11)$$

where  $x_I^{[k]}$  is the augmented state,  $e^{[k]}$  is the output error, and  $y_I^{[k]}$  is the result of Tustin integration method. The discrete control

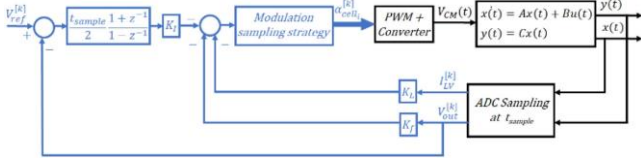


Fig. 4. State-space feedback control.

law is given in (12) and the SSFC structure is shown in Fig. 4:

$$\alpha_{\text{CM}}^{[k]} = - [K_L \ K_f \ K_I] \begin{bmatrix} I_{\text{LV}}^{[k]} \\ V_{\text{out}}^{[k]} \\ y_I^{[k]} \end{bmatrix} \quad (12)$$

where  $\alpha_{\text{CM}}^{[k]}$  is the mean duty cycle in the discretized  $k$  instant and  $K_L$ ,  $K_f$ , and  $K_I$  are the gains of the SSFC. The augmented model is presented as follows:

$$\begin{bmatrix} x_s^{[k+1]} \\ x_I^{[k+1]} \end{bmatrix} = \begin{bmatrix} A_d & 0 \\ -t_{\text{sample}} C_d & I \end{bmatrix} \begin{bmatrix} x_s^{[k]} \\ x_I^{[k]} \end{bmatrix} + \begin{bmatrix} B_d \\ 0 \end{bmatrix} V_{\text{cm}}^{[k]} + \begin{bmatrix} 0 \\ t_{\text{sample}} \end{bmatrix} y_{\text{ref}}^{[k]} \quad y^{[k]} = [C_d \ 0] \begin{bmatrix} x_s^{[k]} \\ x_I^{[k]} \end{bmatrix}. \quad (13)$$

Equation (7) is an approximation that allows to write (6) as a linear model suitable for the control design. In fact, as shown in Fig. 4, the  $\alpha_{\text{cm}}^{[k]}$  calculated by the control is sampled and compared to the carriers of each cell to determine the real cell duty cycles  $\alpha_{\text{cell}_i}^{[k]}$ . Consequently, the real mean voltage applied to the output filter  $V_{\text{cm}}^{[k]} \cdot \alpha_{\text{cm}}^{[k]}$  is not strictly . For slow bandwidth controls, this sampling process is negligible, but when fast controls are required, as in the HBCs, the modulator plays an important role in the control performance.

### B. Modulators

In this article, the main carrier based modulators for multicell converters presented in the literature are compared for HBC: the symmetrical and asymmetrical sampled modulators with the multisampling technique proposed in [18], named here simply SS- and AS-PWMs; natural sampled modulator with multirate technique presented in [20], called NS-PWM; and multirate modulator proposed by [21].

The article focuses the multirate modulator due to the easy implementation for generalized  $n_{\text{cell}}$  converters and its comparison with SS- and AS-PWMs, since avoiding the extra pulses in the NS-PWM is more complex, and the overswitching is undesired. Therefore, multirate modulator is briefly described in this section.

The sampling process in the multirate modulator is similar to the classical modulators SS- or AS-PWMs, i.e.,  $\alpha_{\text{CM}k}$  is updated on the minimum or on the minimum and maximum of the cell carriers, respectively. If the update is done once per carrier period (single sampled), the modulator is named MSS-PWM (multirate symmetrical sampled) and twice (double sampled), it is named MAS-PWM (multirate asymmetrical sampled).

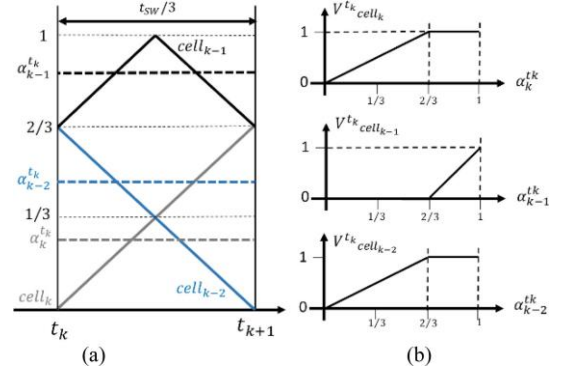


Fig. 5. Hypothetical three-cell converter: (a) PWM carriers during one subcycle sampling period and (b) possible voltage contributions of each cell [21].

In order to obtain the mean values of the converter output current and voltage, they are sampled with  $t_{\text{sample}}$ , given in (10), and the control algorithm runs at this frequency. Nevertheless, in the classical modulators, to avoid overswitching, the duty cycle of each cell is updated according to its own carrier, i.e., the period of update of each cell is  $t_{\text{sw}}$  for single sampled PWMs and  $t_{\text{sw}}/2$  for double sampled.

In the multirate modulator, when an event of one cell is detected (minimum and/or maximum of the carrier), the duty cycles of all cells can be updated if the cell has not changed its state twice (turned ON/OFF) during its switching period. So the update can be done at the same frequency of the control  $t_{\text{sample}}$ . Furthermore, an algorithm is developed to take advantage of the nonlinear relation between mean voltage of each cell ( $V_{\text{cell}_k}^{t_k}$ ) during one sample period and the cell duty cycle  $\alpha_k^{t_k}$ .

Fig. 5 illustrates this nonlinearity for a three-cell converter.

For converters with the control much slower than the carrier frequency, this non-linearity can be neglected [32]. For HBC, this constitutes a key point to improve the ability of the converter to provide the voltage required at the output as soon as possible. The multirate modulator, described in [21], calculates at each instant  $t_k$ , the duty cycles  $[\alpha_k^{t_k}, \alpha_{k-1}^{t_k}, \dots]$  to apply during the next period  $t_{\text{sample}}$ , guaranteeing, if possible, the required output voltage  $V_{\text{OUT}t_k}$ .

To accomplish this, an algorithm is implemented that first determines at each sampling instant which cells have already

switched previously within their own carrier cycles in order to avoid overswitching. Since an iteration of the algorithm is fully executed at each sampling period, this information is simple to obtain and to store in the controller's memory. Those cells that have already switched will contribute with 0 V or  $V_{HV}$  to the output, and the average contribution of the other ones will depend on the duty cycle that will be assigned to them.

The average voltage at the output of the converter is the sum of the output voltage of each cell divided by the number of cells. Therefore, this information allows calculating the incremental voltage that must be synthesized by the cells that are still able to switch. If the voltage demanded is greater than the voltage that can be synthesized by the enabled cells, there is a saturation of the duty cycle. Finally, the algorithm updates the command of all cells that are enabled to switch, keeping unchanged the

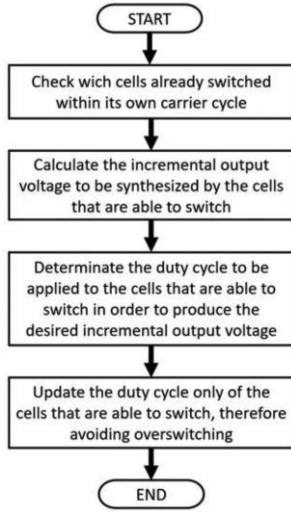


Fig. 6. Simplified flowchart of the multirate modulator algorithm.

command of the others ones. The algorithm flow chart is shown in Fig. 6 and a more in-depth description is presented in [21].

### C. Control Tuning

For the calculation of the gains of the SSFC, (12) and (13) can be used. Nevertheless, this is a linear approximation that neglects the modulator nonlinearity. Mouton and Putzeys [32], Corradini and Mattavelli [33], and Mouton *et al.* [34] show ways of modeling different modulators, but the models are complex and/or consider small-signal analysis.

In the present article, the focus is on the response of large-scale voltage variations in the converter's output, where the modulator's nonlinearity is important. In this case, a complete modeling for control purposes is not trivial. Therefore, to determine the fastest response, the control tuning is based on the closed-loop form of the linear discretized equations (12) and (13) combined with an iterative process using the complete model of the converter simulated in the software PLECS.

The state-space feedback gains are computed by choosing the desired time of first peak ( $t_{peak}$ ), the damping ratio ( $\xi$ ), and

placing the dominant closed-loop discrete poles defined as follows:

$$z_{1,2} = e^{t_{sample} \left( -\xi\pi / (t_{peak} \sqrt{1-\xi^2}) \pm j\pi / t_{peak} \right)}. \quad (14)$$

The integral pole is placed to disturb as less as possible the previous pole placement (one decade separation). The damping ratio is chosen as  $\xi = 0.7$  to avoid high overshoots (<5%). The  $t_{peak}$  is varied iteratively, starting with small value ( $\approx t_{opt}$ ).

- 1) The  $t_{peak}$  is defined, the poles are placed, and the gains calculated.
- 2) A voltage reference step from 10% to 90% of the dc-link voltage is simulated.
- 3) If the duty cycle saturates during the transient, i.e.,  $\alpha_{CM} > 1$ ,  $t_{peak}$  is increased and the process restarts.
- 4) If the duty cycle does not saturate, the effective  $t_{peak}$  obtained in the simulation is measured and this is defined as “the fastest response.”

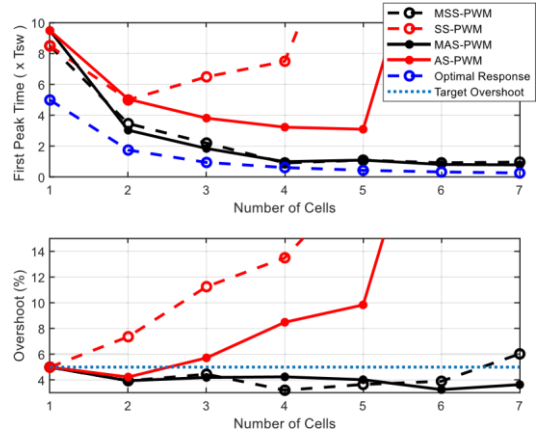


Fig. 7. Closed-loop system response of  $n_{cell}$  series converters with rated load.

The concept of “the fastest response” is relative and is valid only for the considered step amplitude, but it gives an idea of the converter performance for large-scale voltage variations. Avoiding the control saturation ( $\alpha_{CM} \in [0, 1]$ ) makes possible to guarantee the control stability without high oscillations and overshoots, thus, it is the criterion adopted in this article.

It is important to highlight that the SSFC gains are always calculated for each specific case in order to have the fastest possible response, i.e., it changes with  $n_{cell}$ , modulation strategy, load, filter parameters, etc. This guarantees that the best control within the criteria is always obtained.

## IV. RESULTS—SERIES MULTICELL CONVERTERS

### A. Simulation

Computational simulation models were developed in the software PLECS considering ideal multicell converters, as depicted in Fig. 1(a) and (b), with the following characteristics.

- 1)  $V_{HV} = 100$  V,  $I_{LV_{rated}} = 20$  A, and  $f_{Sw} = 20$  kHz .
- 2) Filter parameters presented in Table I.

- 3) The input voltage and the FCs are constant voltage sources.
- 4) Ideal semiconductor models are implemented.
- 5) SSFC is tuned and the results obtained as described in Section III-C.

Fig. 7 shows the time of first peak of the output voltage (as multiples of the switching period  $T_{sw}$ ) and the overshoot for the closed loop, as a function of the number of cells and employing different modulators in SMC. For the SS- and AS-PWMs, increasing the number of cells increases the voltage overshoot and, consequently, the control tends to saturate, violating the criterion of non-saturation. To have a response with small overshoot and oscillations, it is necessary to slow down the control excessively [to choose high values of  $t_{peak}$  in (14)], thus, these results are not shown in the graph. The double sampling process (ASPWM) gives better responses, but the overshoot is still high for increased  $n_{cell}$ .

The multirate modulator results show improved voltage responses when compared with the classical modulators independently of the  $n_{cell}$ . This happens because the effective

TABLE II  
CONVERTER AND FILTER PARAMETERS OF THE TEST SETUP

Input Voltage ( $V_{HV}$ )	100V		
Output Current ( $I_{LV}$ )	20A		
Switching Frequency ( $f_{sw}$ )	20kHz		
Semiconductors	Mosfet Infineon IPB025N10N3		
Flying Capacitors	60 $\mu$ F		
Dead Time	1 $\mu$ s		
$n_{cell}$	3	5	6
$C_{LV}$ ( $\mu$ F)	27.5	18.33	13.75
$L_{LV}$ ( $\mu$ H)	25	10	5

voltage imposed by the converter with multirate is closer to the voltage demanded by the control and, consequently, the control is more effective, allowing faster responses.

Comparing the single (MSS-PWM) and the double (MASPWM) sampling in the multirate, an insignificant difference can be observed. Therefore, the use of MSS-PWM is advantageous since it has less computational burden when compared to the MAS-PWM.

In Fig. 7, it is also shown the theoretical optimal response, as demonstrated in Section II-D. The multirate modulator approximates, with small overshoot, the ideal response. For the designed converter, for  $n_{cell} > 4$ , the increase of the number of cells does not accelerate the response (similar bandwidth).

The increase of the filter bandwidth does not always result in a real increase of the system bandwidth in closed loop due to the limitation imposed by PWM-based modulators. As demonstrated in [4], the higher the ratio between modulating signal frequency to the carrier frequency ( $f_{sw}$ ), the higher is the voltage attenuation for SS-PWM and NS-PWM with avoided overswitching. Therefore, even if the sampling is increased

with higher  $n_{cell}$  ( $t_{sample}$  decreases), the control bandwidth is limited by  $f_{sw}$ .

## B. Experiment

The experimental setup utilizes a 12-cell series converter from CIRTEM, which the parameters and filters are described in Table II. Due to component availability, the filter's inductors and capacitors are slightly different from the design and just parts of the cells are employed. Fig. 8 depicts the test bench.

The control and modulator are implemented in a PLECS RTBox. The inherent time delay between duty cycle computation and analog to digital conversion of the measurements makes the implementation of a fast control in this platform a difficult task. Therefore, an open-loop state-space estimator [41] based on (8) is implemented to estimate the voltage and current used in the control. Since the objective is to demonstrate the behavior of the different modulators, not of the control, the details of this estimator are omitted. Nevertheless, the results presented are from voltage and current measurements using an oscilloscope.

Fig. 9(a) shows the open-loop voltage response of the three cell converter for a duty cycle step from 0.1 to 0.9. It is seen that the SS-PWM presents the slower response and the MSS-PWM is an intermediary response when compared with NS-PWM. The same test is done using six cells, as shown in Fig. 9(b). In this case, the slower response of the SS-PWM is more noticeable since it has longer rising time and time to first peak, and the MSS-PWM can respond almost as fast as the NS-PWM.

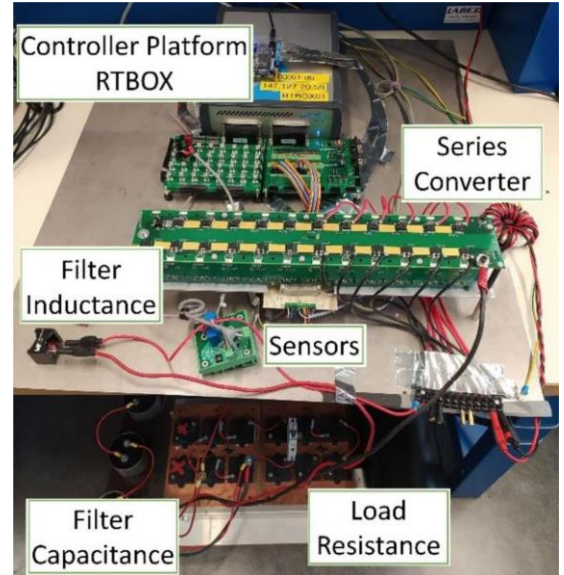


Fig. 8. Experimental setup: dc/dc 12-cell series converter.



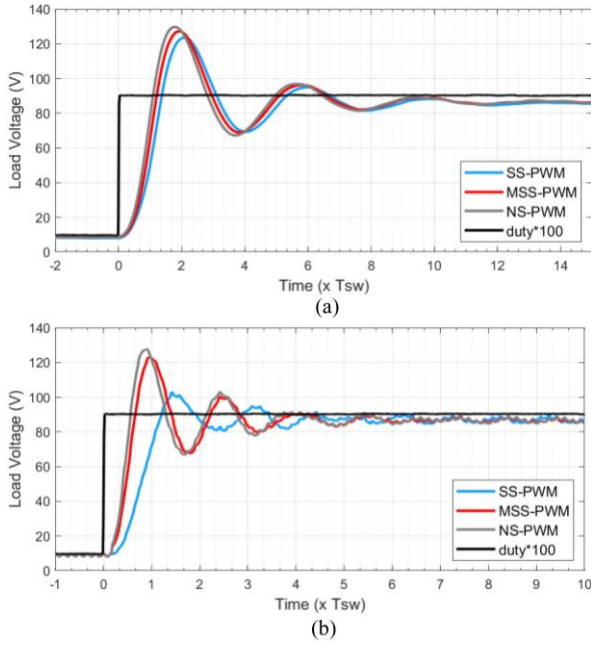


Fig. 9. Experimental results series converter in open loop with rated load. Measured load voltages with (a)  $n_{cell} = 3$  and (b)  $n_{cell} = 6$ .

With high inductances, the converter current variation is slow and, consequently, the difference in the output voltages between two sampling instants is small. In this situation, the nonlinearity of the modulator is negligible. The smaller the inductance, the faster the current and voltage variations, thus, the nonlinearity in a sampling period becomes important to guarantee a fast response. One can conclude that when  $n_{cell}$  increases (smaller filter inductances), it becomes more important to use a modulator with a small delay.

Even a small difference in the open loop response with the different modulators can represent a significant improvement in closed loop, as shown in Fig. 10(a) for the three-cell converter. Due to converter current limitation, the test considers a voltage step from 20% to 80%. In this case, the duty cycles do not reach the limit ( $\alpha_{CM} = 1$ ), as demonstrated in Fig. 10(b), but the control is adjusted in such a way that the fastest possible response is obtained without high overshoots. It is seen that MSS-PWM is much faster than SS-PWM and nearly equivalent to NS-PWM. It is important to highlight that NS-PWM is prone to overswitching, since the extra pulse blocking is not implemented in this article.

Fig. 10(c) shows that fast response means high current overshoot ; for the MSS- and NS-PWM, the current reaches more than two times the rated current of the converter (20 A). It is clear that the converter must be designed to support this transitory peak current in order to have the fast response desired of HBC.

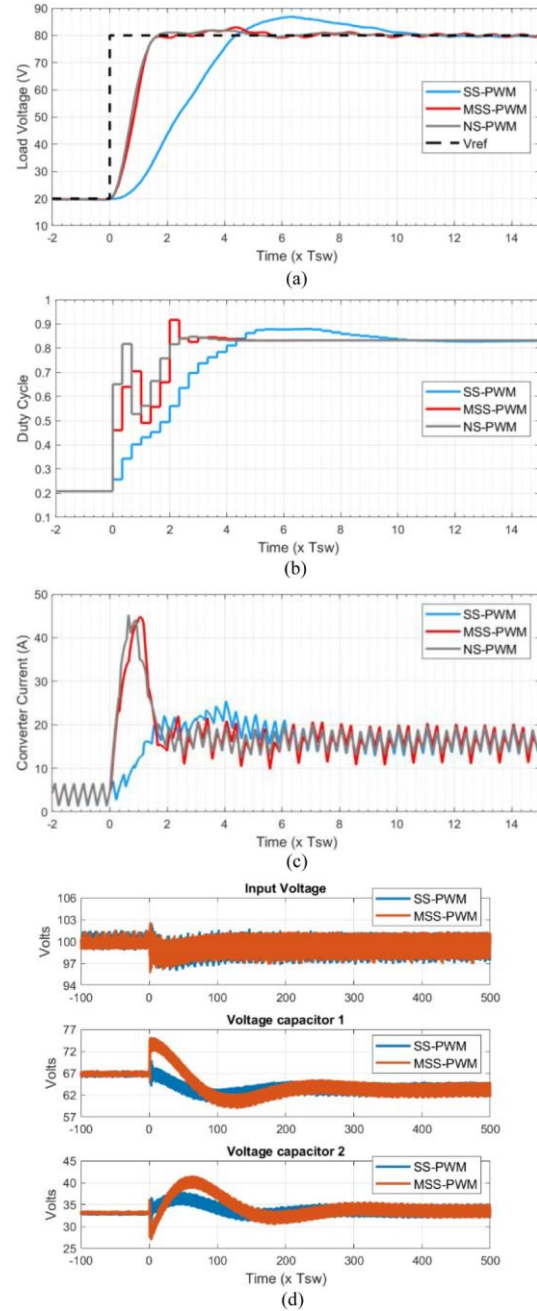


Fig. 10. Experimental results of three-cell series converter in closed loop with rated load: (a) load voltage, (b) duty cycle (control command), (c) converter current, and (d) flying capacitors voltage.

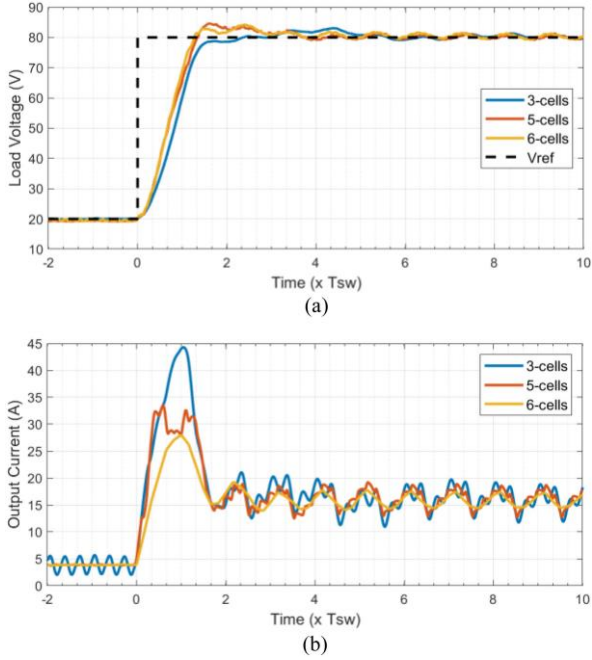


Fig. 11. Experimental results series converter with different  $n_{cell}$  in closed loop with MSS-PWM and rated load: (a) load voltage and (b) converter current.

Another important point is the balance of the FC voltages. One can see in Fig. 10(d) that, because of the high current transient, the FC voltages vary significantly which can be dangerous for the semiconductors and may increase the output voltage ripple. The benefit is that the use of the MSS-PWM does not affect the natural FC voltage balancing, but this is a relatively slow process, as shown in Fig. 10(d). The problem can be reduced if the FC capacitances are increased, increasing the energy stored, or using passive [36] or active [37] balancing strategies, as presented in the next subsection.

Comparing the results of converters with different number of cells using the MSS-PWM, Fig. 11(a) shows that the higher the number of cells the fastest the response, as the three-cell has the slower response and six-cell the fastest, although extremely close to the five-cell one. These results confirm the behavior shown in Fig. 7, but the differences between the responses are not as significant as expected between  $n_{cell} = 3$  and  $n_{cell} = [5,6]$ . In fact, the nonlinearities of the test bench, the variation of the FC voltages, and the limitations of the control platform make it hard to push the converter to its limits. Therefore, with increased number of cells, the control is tuned slower than the speed theoretically possible, i.e., the speed obtained in simulation.

Even with similar voltage responses, it is interesting to note in Fig. 11(b) that when the number of cells increases, the peak current is reduced. Since the filter inductance and capacitance reduces with the increase of  $n_{cell}$ , less energy (current) is necessary to change the voltage output. This observation gives an important remark: for a desired bandwidth, it is possible to increase the number of cells in order to reduce the peak current.

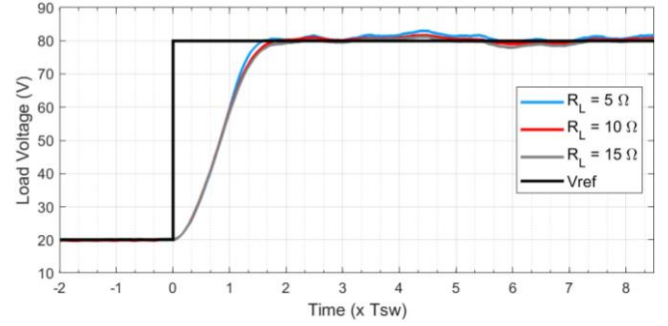


Fig. 12. Experimental result of three-cell series converter in closed loop with MSS-PWM for different loads.

This means that even if a desired bandwidth can be reached with a specific number of cells, it is possible to choose a higher number of cells to reduce the current transient and, e.g., reduce the semiconductors current requirements. The quantification of number of cells versus peak current is out of the scope of this article.

The results shown until here considered the operation with rated load resistance ( $R_L = 5 \Omega$ ). Fig. 12 presents the voltage response of the three-cell converter employing the MSS-PWM under different loads. It is seen that the load resistance does not affect the voltage time response, as it has little influence on the filter bandwidth. Instead, the load resistance affects the resonant peak of the filter, as it changes the filter damping and, consequently, the current transient peak.

Since the variation on the FCs' voltages and consequent unbalance can be a problem when fast responses are desired in the SMC, an active FC balancing control (FBC) is implemented. This strategy is based on the correction of the duty cycles according to the measured voltage unbalance, as described in [37]. A PI controller was used with gains adjusted in a conservative way, applying  $K_p = 1/V_{HV}$  and  $K_i = 1$ .

Fig. 13(a) shows that a fast voltage balancing is possible, but the FC voltage's variation in the transient is almost not affected. Nevertheless, as demonstrated in Fig. 13(b), the behavior of the output voltage is almost not affected, and the fast response is still guaranteed. Therefore, it is seen the importance of using balancing strategies and the design of the capacitors to avoid huge voltage variation.

A deeper analysis of FBC is out of the scope of the article, but it is proved that it can be used without affecting the behavior of the MSS-PWM and its fast response with SSFC.

## V. SERIES VERSUS PARALLEL MULTICELL CONVERTERS

The goal of the comparison here is to highlight the bandwidth characteristics of SMC and PMC. Details of the converters design, as components count, efficiency, fault tolerance, etc.,

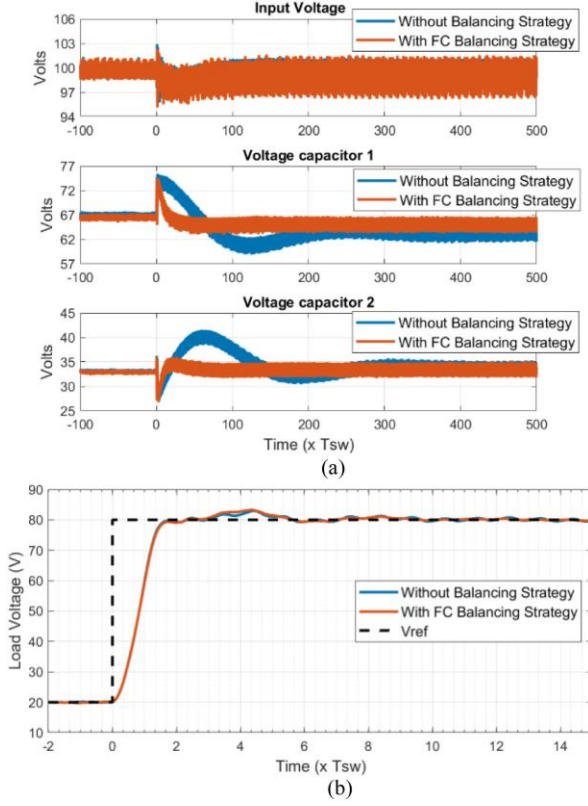


Fig. 13. Experimental results of three-cell SMC in closed loop with MSSPWM and rated load, with and without FC active balancing strategy: (a) flying capacitors voltages and (b) load voltage.

TABLE III

TIME TO FIRST PEAK (MULTIPLE OF  $t_{sw}$ ) FOR  $n_{cell}$  PARALLEL CONVERTERS WITH DIFFERENT MODULATORS

		$n_{cell}$					
		2	3	4	5	6	7
Modulator	SS, PWM	4.95	3.81	3.25	3.5	3.8	3.9
	MSS, PWM	3.48	2.83	3	3.28	3.32	3.62
	AS, PWM	4	3.5	3.25	3.5	3.8	3.8
	MAS, PWM	3	2.2	3	3.28	3.4	3.48

are not evaluated. Gleißner and Bakran [38] briefly discuss these points.

#### A. Time Response Comparison

Simulating the parallel converters with different modulators using the filter parameters of Table I and considering a voltage step from 10% to 90%, the first peak times are presented in Table III. Fig. 14 shows the graphical comparison of the responses using the MSS-PWM for the SMC and PMC, and the optimal expected values, calculated as in Section II-D. The percentages of how much the PMC response is higher in relation to the SMC are also shown.

One can see in Table III that for the PMC, the improvement in the response using the multirate modulator is more significant for two and three cells and tends to be constant with more cells. This happens because the equivalent inductor is independent of  $n_p$ , but the capacitance decreases with  $n_p^3$ . Therefore, the filter

bandwidth that is affected only by the capacitance varies more for small number of cells.

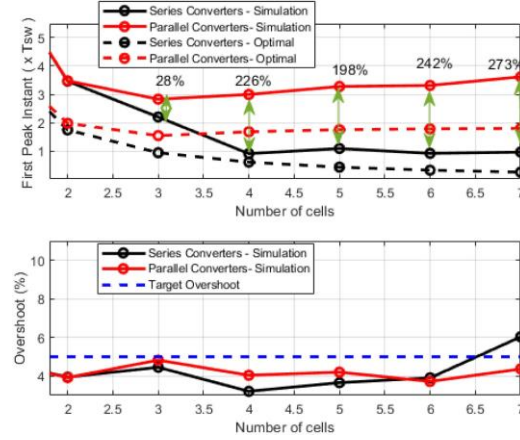


Fig. 14. Optimal response vs simulation results of closed-loop system response of  $n_{cell}$  series and parallel converters employing MSS-PWM with rated load.

For the SMC, the higher  $n_s$ , the higher the filter bandwidth, since the filter's inductance and capacitance diminish and, consequently it is possible, theoretically, to have faster control. Nevertheless, in order to have an effective fast control, it is necessary to use an appropriate modulator. Therefore, as presented previously in Fig. 7, the improvement provided by the multirate is more important with increased  $n_s$ . One of the conclusions is that having a modulator with a small delay is crucial when the filter cutoff frequency is high.

From these results, it is concluded that in order to have HBC, it is necessary to reduce the modulator delay and this applies both to PMC and SMC, i.e., the multirate modulator is always recommended. However, as SMC filters have greater cutoff frequencies, for the design rules adopted, their overall response time is more sensitive to the modulator's response time. For this reason, the principle of multirate control introduced in [21] brings a significant improvement in SMC.

It is clearly seen in Fig. 14 the SMC advantage for increased  $n_{cell}$ , as the responses are closer to the optimal responses than the PMC. For the latter, the responses become a bit slower as the filter bandwidth decreases for  $n_{cell} > 3$ . Similar behavior is seen in the optimal response. For the SMC, the response becomes almost constant for  $n_{cell} > 4$ , as already discussed. In both cases, the overshoot is kept under acceptable values.

As already discussed in Section IV-A, the increase of the number of cells has a limit in the increase of the system bandwidth due to the PWM. In the case of study, one can see that the use of more than three cells for the PMC does not bring advantages in terms of response, and that for the SMC this limit is four cells. Therefore, these are the number of cells to be chosen if the main criterion is bandwidth. It is important to highlight that these results are for the filter design rules and converter characteristics chosen. Analysis, as presented in this article, should be carried out for different HBC projects.

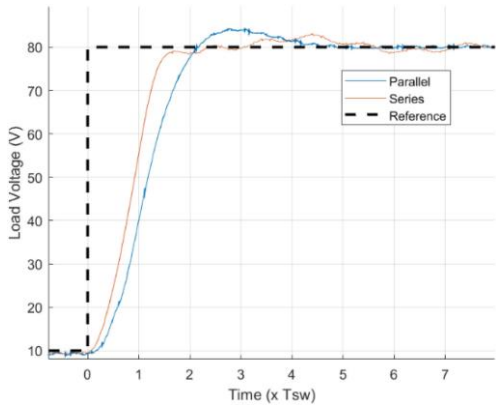


Fig. 15. Experimental results comparing load voltage response of closed-loop system for three-cell PMC and SMC employing MSS-PWM with rated load.

TABLE IV

TIME TO FIRST PEAK (MULTIPLE OF  $t_{sw}$ ) FOR  $n_{cell}=3$ , SERIES AND PARALLEL CONVERTERS WITH MSS-PWM AND DIFFERENT LOADS

$R_L$ ( $\Omega$ )	5	6.5	8	9.5	11	20
PMC	2.83	2.5	2.17	1.83	1.83	1.83
SMC	2.22	2.24	2.17	2.17	2.17	2.17

Fig. 15 presents the experimental results comparison for three-cell PMC and SMC. The filter parameters of PMC are similar to the ones presented in Table I and the prototype is described in [21]. One can see that the series is a bit faster than parallel, and the results are in good agreement with Fig. 14. As previously mentioned, the superior performance of the SMC is more pronounced for higher number of cells.

Another difference between the SMC and PMC is the behavior under different loads. As presented in the experimental results, the SMC is almost unaffected by the variation of the load resistance. This behavior is also seen in the simulation results presented in Table IV for the three-cells case. The PMC is more affected by the load resistance since the bandwidth of the filter varies with this value. One can see that, in this case, depending on the load, the PMC can be faster than the SMC. However, the control must deal with this “plant variation” (here the control is readjusted for each simulation).

The SMC is affected by FC voltage unbalances for fast voltage transients, as well as the PMC counterpart is the current unbalance between the cells. Nevertheless, the converter current transient peak in the PMC is generally much smaller than the SMC. For example, in the three-cell case for a step from 10% to 90% with rated load, in the SMC, the peak current reaches almost three times (60 A) the load rated current, while in the PMC the peak is under 20 A. As already discussed, the PMC equivalent inductance does not reduce with the increase of  $n_{cell}$ . It is clear that, for taking advantage of the reduced filter in the SMC, it is necessary to pay the price of high current overshoot or increased number of cells.

### B. Frequency Response

Until now, the converter behavior for a step response was analyzed. The equations presented in Section III-A are

simplifications that neglects the nonlinearity of the modulator that is very important to HBC. As fast the control, which is the case for

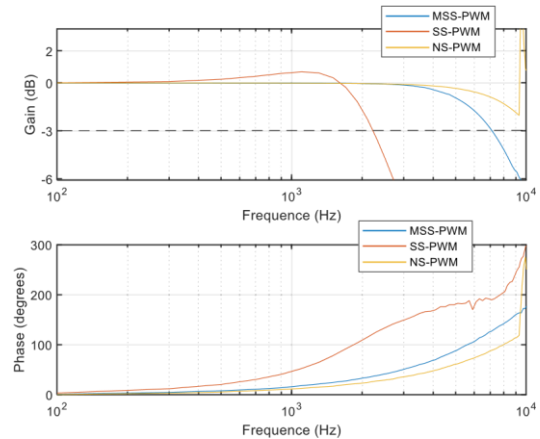


Fig. 16. Closed-loop frequency response for three-cell series converter using different modulators.

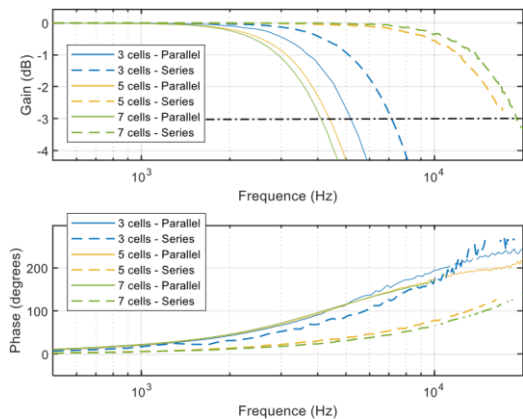


Fig. 17. Closed-loop frequency response for  $n$ -cell series and parallel converters using MSS-PWM.

higher number of cells, more the simplified model diverges from the real response. Therefore, the frequency response analysis proposed here is based on simulation results.

As the objective is to evaluate the high signal response, a sinusoidal voltage reference with amplitude from 10% to 90% (dc component in 50%) is applied to the control and the frequency is varied from 100 to 20 000 Hz. The closed-loop amplitude and phase responses are evaluated. The same procedure based on step responses was used to set the control gains, i.e., the same gains used to plot Figs. 7 and 14 were used to investigate the frequency response.

Fig. 16 shows the results for a three-cell SMC for the single sampled modulators. One can see that the use of MSS-PWM allows the increase of the bandwidth to 7 kHz when compared to SS-PWM (2 kHz). Using the NS-PWM with permitted overshooting, the bandwidth can be extended, but for frequencies above 9 kHz the control does not respond properly. As already discussed, the closer the switching frequency, higher is the modulator attenuation and phase delay.

The frequency responses comparison between  $n_{\text{cell}}$  SMC and PMC are shown in Fig. 17. Due to the design filter characteristics, PMC bandwidths do not change very much with the number of cells and in this case are restricted between 2 and 5 kHz.

For the SMC, the range of variation with the number of cells is higher, varying from 7 to around 19 kHz. There is a greater difference between three and five cells, confirming the result of Fig. 14, and for higher number of cells the difference becomes negligible. For frequencies close to  $f_{\text{sw}}$  (20 kHz), the control does not work properly due to the modulator limitations.

The frequency responses highlights the main conclusions of this article: the multirate modulator is recommended when a fast control is desired, SMC have advantages in terms of dynamic behavior compared to PMC and the increase of the number of cells contributes for higher bandwidths, but there is a limitation to the response improvement (in this case of study, four cells).

## VI. CONCLUSION

In this article, a multirate modulator was applied for high bandwidth SMCs. This modulator takes into account the nonlinearity between the mean voltage of each cell during one sample period and the cell duty cycle. The cells duty cycles are modified in order to have the output voltage as close as possible to the reference, avoiding overswitching. This means a modulator with a small delay and, consequently the possibility of having a fast control (high bandwidth) with large-signal voltage changes.

Simulation and experimental results for various numbers of cells and employing different modulators were presented. The multirate modulator always shows superior performance when compared with classical SS-PWM and AS-PWM, approximating the response of the NS-PWM. Since the multirate modulator is of simple digital implementation and intrinsically avoids overswitching, it is always recommended for HBC.

The drawback of fast response is the high converter current during the transients. This has direct impact in the HBC semiconductor design and in the unbalance between the FC's voltages. Nevertheless, the experimental results show that a simple voltage balancing strategy can be employed without affecting the converter voltage response.

The proper filter design, as presented in the article, permits the improvement of the filter bandwidth with a higher number of cells, but it does not necessarily represent an increase in the converter bandwidth. The use of PWM modulators limits the response of the system according to the switching frequency. Even if the bandwidth is limited, using more cells in series permits the reduction of the current peak during voltage transients.

This article also presents a comparison between the use of series or parallel cells in terms of response speed. This comparison is based on filter design rules that have been

clarified and systematically applied to the series and parallel converters studied in this article. The simulation results demonstrate that, in both cases, the multirate modulator presents superior performance. In the series case, the design rules result in a filter with a cutoff frequency that is higher than for the parallel case; as a consequence, the improvement in the response is more noticeable in the series case and this difference between the series and the parallel configuration increases with increasing numbers of cells.

The principle of the multirate modulator is quite general and can be applied to several other multilevel topologies. As soon as the chopped voltage can be expressed as the sum of the square voltages produced by several commutation cell voltages, which is for example the case of MMC and CHB, the multirate algorithm used in this article can be applied to optimize the position of the different voltage steps in the chopped voltage. The design of the filters of such converters is also very similar to the case of the FC converter described in this article, and therefore these topologies will not suffer from the limitations of the parallel multilevel converters briefly explained in Section II of this article.

However, it must be understood that fast action of the multirate control causes asymmetrical cell control patterns, which might result in unbalanced voltages. The control loop needed to compensate for these voltage imbalances depends on the current path associated to each state of the converter and consequently a specific voltage balance control should be developed for each topology (e.g., MMC, CHB, etc.). The application of multirate for other multilevel topologies is part of the continuation of this article.

Finally, from the results, we can list the main factors that will affect the performances of HBCs: modulator with small delay, proper filter design for SMC and PMC, number of cells, maximum transient current supported by the semiconductors, and FCs voltage balance in the series case. Obviously, the control design also plays an important role, but it is always limited by the modulator. The study of other control strategies combined with multirate modulator is also a proposal of work continuity.

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