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ABSTRACT

This paper demonstrates the use of numerical simulation data, depending on the behavior of a low voltage dropout regulator, for reliability performance estimation based on the accelerated degradation test data. The regulator was designed using Cadence Virtuoso software in 180 nm AMS CMOS technology, and simulated to evaluate its output voltage variations to both temperature and input voltage. The output voltage degradation data were generated according to environmental parameters (input voltage and temperature) constraints, which makes it possible to define failure thresholds under accelerated conditions, making use of the numerical simulation model along with the proposed degradation model. Degradation path model has been adopted to determine the pseudo failure time under the specified failure criterion (5 %). Acceleration law model has then been derived to estimate the reliability model parameters by performing maximum likelihood estimation method not only to analyse but also to predict lifetime data distribution of the regulator under different voltage and temperature stress conditions.

1. Introduction

Reliability prediction of integrated circuits (ICs) embedded in electronic components is essential for manufacturers to estimate the functionality and probability of failure while operating under extreme external operational conditions (e.g. high or low temperature, humidity, voltage or current stress). Moreover, advanced reliability model (i.e. M-STORM) needs to be developed and integrated with conducted immunity model (ICIM-CI) for predicting long-term evolution of electromagnetic compatibility (EMC) on CMOS ICs operating at external environmental constraints [1].

Study of reliability modelling is generally proposed based on traditional standards available in MIL-HDBK-217F [2] and FIDES [3]. HTOL (high temperature operating life test) and LTOL standard ageing measurements are usually conducted on ICs to induce and accelerate different types of intrinsic degradation mechanisms [1]. Depending on the ageing stress types (high or low temperature, voltage, etc.), different failure degradation mechanisms are activated in CMOS circuits, which vary mobility and threshold voltage (V_{th}) parameters of MOS transistors in deep submicron CMOS technology depending on ageing stress magnitude and duration [4].

Negative bias temperature instability (NBTI) and hot carrier injection (HCI) degradation mechanisms are activated when HTOL test is conducted on MOS devices under high temperature, electric field and high negative gate bias voltage, while time-dependent dielectric breakdown (TDDB) is observed due to applying low temperature and low drain – source voltage on MOS transistors during LTOL test [5]. In [6], NBTI degradation on VDMOSFET was investigated under external magnetic field that identified formation of paramagnetic defects at the interface between silicon and the oxide layer. In [7], stress-induced NBTI effect was characterized in p-channel power VDMOSFET to investigate V_{th} drift at high temperature stress conditions for predicting the device lifetime reliability by applying different linear extrapolation models to fit experimental degradation data.

Previous studies on extracting accurate reliability modelling for ICs have considered multiple failure mechanisms by conducting multiple temperature operating lifetime (MTOL) method under multiple simultaneous stress conditions [8]. Multi-stress predictive reliability model (M-STORM) is developed considering different combinations of temperature and voltage stresses applied on FPGA circuits to accurately evaluate and predict the IC failure rate and time to failure (TTF) under any specified operating conditions [1,9]. Depending on the multiple

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stress conditions, the MTOL method enables to distinguish and identify different failure degradation mechanisms inducing on the CMOS circuits during accelerated ageing tests [10,11].

In [12], the usage of MTOL testing method was demonstrated to predict probability of failure (PoF) and calculate the failure in time (FIT) of multiple failure mechanisms for reliability prediction of FPGA devices fabricated on 45 nm and 28 nm CMOS technology. In [13], degradation data generated during measurements was used to develop accurate predictive reliability model by combining FIT of multiple failure mechanisms. The reliability matrix method, which involves predicting failure rates of each different failure mechanisms using corresponding mathematical models, followed by evaluation of accelerated factors were adopted for each failure types based on ageing test data [8]. Hence, the system reliability predicted accurately by the matrix solution method at any operational conditions that were not specified during the ageing test [8,12].

Failure threshold is generally required for an IC to define the time to failure under nominal conditions. However, this criterion is indeed essential for defined accelerated life test conditions. The goal of this paper involves conducting reliability study solely based on the development of electrical design model follows by the use of reliability software tools to estimate reliability model parameters.

The paper outlined as follows. Section 2 describes the voltage regulator circuit design in Cadence Virtuoso software using 180 nm CMOS technology as well as discussing the simulation results to analyse both temperature and voltage sensitivity. That section also includes mathematical and curve fitting simulation model of the output voltage (V_{out}) for varying combinations of temperature and input voltage variations before degradation. Section 3 summarizes methods to produce degradation path model based on generated aged degradation data to compute pseudo-lifetime for specified failure threshold criterion. This section also provides the reliability modelling and estimation analysis taking into account the degradation data and pseudo-lifetime based on the developed simulation model for accurate prediction of its lifetime parameters under different ageing stress conditions. Concluding contributions of the reliability study are provided in Section 4.

2. Circuit design and simulation

Fig. 1 shows the internal structure of the designed low dropout voltage regulator using Cadence Virtuoso software in AMS 180 nm technology. It consists of the operational amplifier (error amplifier), power MOSFET, voltage divider and load. A two-stage cascaded transconductance operational amplifier was designed using both p- and n-type MOSFETs with the required aspect ratio width (w)/length (l) to obtain desirable output voltage and current. Power MOSFET was designed as a pass element with large aspect ratio (w/l) to drive a high current into the voltage regulator circuit block. The series connected resistive voltage divider circuit acts as a negative feedback for the amplifier to compare the output voltage of the amplifier with the 1.2 V bandgap voltage reference (V_{ref}) value provided at the negative input terminal of the amplifier. The difference between these two voltages is adjusted to obtain V_{out} of the regulator.

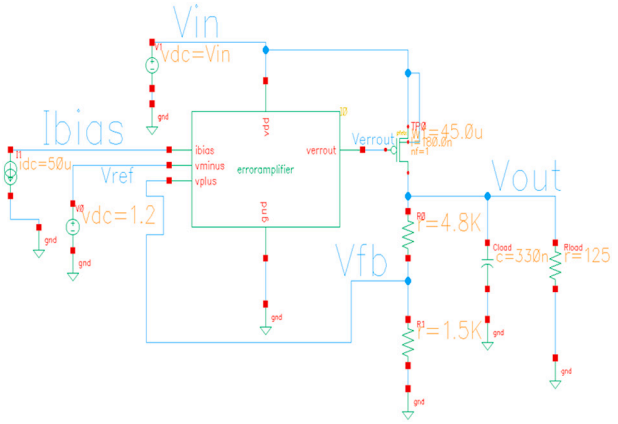

Fig. 1. Circuit design schematic of the studied regulator.

2.1. Simulation results: temperature and voltage sensitivity analysis

The designed circuit was simulated in Spectre to analyse both temperature and voltage sensitivity. The V_{out} variations were monitored for operating temperature between −40 °C and +120 °C, while keeping the input voltage (V_{in}) unchanged at a nominal value of 7 V. The output voltage increased the non-linearly at lower temperature and vice versa. Hence, the regulator was found to be sensitive to temperature variations, with minimal temperature sensitivity of 0.000406 V/°C (Fig. 2). Voltage sensitivity simulation was conducted by varying V_{in} within a range of 6.5 V to 7 V at constant nominal temperature of 27 °C. Results demonstrated the linear variation of V_{out} for changing V_{in}, with a relatively higher sensitivity of 0.64.

Both the V_{in} and operating temperature were varied simultaneously to observe the combined impact of these parameters on the overall V_{out}. The effect of varying both temperature and V_{in} on the V_{out} is shown in Fig. 2.

2.2. Simulation model

Based on the circuit design model developed in Cadence software, simulation data obtained from the set of curves in Fig. 2, the output voltage dependency of the regulator on temperature and V_{in} can be modelled mathematically. Non-linear relationship between V_{out} and temperature was observed at constant V_{in}, which can be modelled separately in terms of polynomial function. On the other hand, V_{out} behaves linearly due to changing V_{in} for a fixed temperature, which can also be expressed mathematically.

Overall, those two mathematical functions can be combined (Eq. (1)) forming a single mathematical simulation model for V_{out} as a function of both dependent variables (temperature and V_{in}), where T and V_{in} represent temperature and input voltage applied to the regulator, respectively. The output characteristics of the proposed electrical simulation model for the regulator was investigated at low input voltage range (6.5 V–8.5 V) along with varying operating temperature between −40 °C and +120 °C for developing the mathematical simulation model (Eq. (1)) at degradation time (t = 0), prior to applying accelerated degradation for high ageing voltage (12 V and 18 V) and high temperature stress conditions.

$$V_{out} = \left(aT^2 + bT + c\right)\left(dV_{in} + e\right) \tag{1}$$

Results in Fig. 2 were used to demonstrate the best curve fitting polynomial model to determine the constant values of the unknown

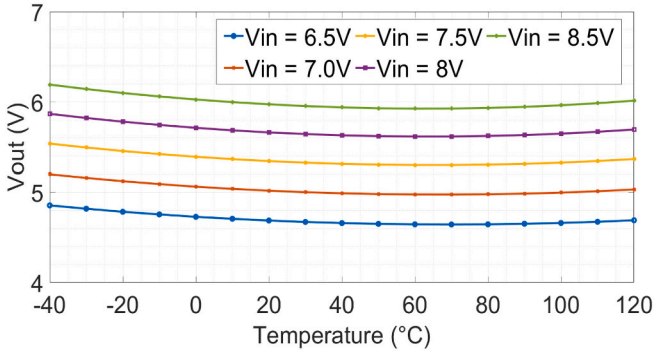

Fig. 2. Output voltage as a function of temperature and input voltage variation.

variables (i.e., a, b, c, d and e). Fig. 3 illustrates graphically the developed simulation model. The graph in Fig. 3 displays distribution of simulated data points close to the surface of the polynomial due to applying the best suitable curve fitting modelling technique. As observed, it is possible to obtain the V_{out} at any operating temperature and corresponding V_{in} by substituting known values of curve fitting constants substituted in Eq. (1). It is worth mentioning that the proposed model is likely to be appropriate for other types of technologies, where the electrical simulation model for the design kit could be developed in other CMOS technology.

3. Degradation path and accelerated life test model

Electrical simulation model for the regulator developed with the aid of schematic design in cadence allowed to obtain simulation data before the ageing degradation time. Simulated test data were used to demonstrate the purpose of this methodological approach. The V_{out} degradation data was considered for the total ageing duration of 1000 h with a span of every 200 h.

Degradation data was generated for the specified ageing stress conditions, which include combination of both different ageing input voltage and temperature stress level at 12 V and 18 V for corresponding temperature stress of 80 °C and 120 °C, respectively.

A methodological approach was applied to obtain degradation data at different ageing stress time, based on some specific simulation procedures that have been mentioned as follows:

1. Obtain relevant reliability parameters (i.e. π_{th}) for the IC regulator using the FIDES [3] predictive reliability analysis standard to compute failure rates (λ) corresponding to different failure modes.
2. Apply FIDES [3] standard to separately compute the acceleration factors (A_{FT}) due to temperature stress by defining the Arrhenius law model and A_{FV} due to voltage stress using the model according to the standard defined for the regulator.
3. Generate failure times at different ageing stress time for different combinations of voltage (12 V and 18 V) and temperature stress (80 °C and 120 °C), while considering A_{FT}, A_{FV} and the Weibull distribution for the degradation process.
4. Define the failure criterion for the regulator to determine the corresponding V_{th} drift from the nominal V_{out} data at specified ageing stress condition.
5. Propose and develop the degradation model in the simulation step and obtain the values of unknown parameters of the model for different combinations of stress levels defined at the initial stage of the simulation procedure. The unknown parameters (β and B) were evaluated using the simulation test data, while the unknown variable α was obtained using the computed failure time and V_{th} drift data.
6. Finally, V_{out} degradation data at different stress time intervals was generated from the proposed degradation model with known values of degradation model parameters.

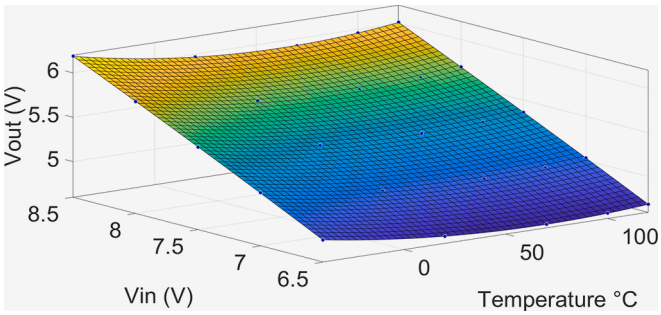

Fig. 3. Simulation curve fitting model of the output voltage.

3.1. Degradation model estimation

The output voltage as a function of ageing stress time for different temperature and voltage stress is plotted in Fig. 4. In order to fit sets of voltage degradation data for specified ageing stress conditions, the mathematical degradation model was proposed in Eq. (2), where V_{out} depends on stress time duration, stress magnitude (V_{in} and T), unknown parameters α and β are functions of V_{in} and temperature (T/°C) and unknown coefficient B is linear function of V_{in} and T. The expression in Eq. (2) demonstrate the degradation model for the regulator, indicating how V_{out} link to ageing stress time ($t > 0$) at any specified combination of V_{in} and T. Therefore, Eq. (2) provides an insight to understand the impact of t on V_{out}, with T and V_{in} applied simultaneously. The proposed degradation model might vary, and hence, the acceleration law model might differ for different technology because of different associated failure modes or degradation mechanisms.

$$V_{out}\,(t, V_{in}, T) = \mu t^{\Upsilon} + D \tag{2}$$

Fig. 4 illustrates four different V_{out} degradation paths were generated for each corresponding different stress level (12 V and 18 V) at different temperatures, which fits the V_{out} degradation data with greater accuracy. Plotting the best fits of the degradation model to the data indicates that the model is adequate for estimating the unknown parameters (μ, Υ and D) of the model.

The graph demonstrates that the degradation level increases with stress duration, with more pronounced V_{out} degradation observed for higher stress conditions (18 V and 120 °C). Considering a fixed failure criterion of 5 %, corresponding V_{th} was defined as the minimum degraded output voltage above the nominal voltage at which the regulator could be considered to fail.

Considering the regulator's performance ratings (maximum current and voltage) from the datasheet, a fixed failure criterion was chosen with an arbitrary value in order to ensure that the regulator would not undergo into permanent failure mode while assessing its performance degradation throughout the total specified stress duration of 1000 h.

Thus, the TTF was determined at the defined V_{th} for corresponding 5 % failure criterion at the specified ageing stress conditions. Interpolating the degradation curve to reach the minimum V_{th} (5 % higher than nominal V_{out}) value after degradation would lead to obtain the pseudo failure time. It is also possible to calculate the failure time using the Eq. (3), after determining unknown parameters of the degradation model. Table 1 summarizes the numerical values of the degradation model parameters and failure time computed for each unit of the regulator at different ageing stress conditions. The tabular data for highest applied stress voltage (18 V) and maximum temperature (120 °C) indicates least TTF in hours is needed to reach failure criterion compared to that of other lower ageing stress conditions.

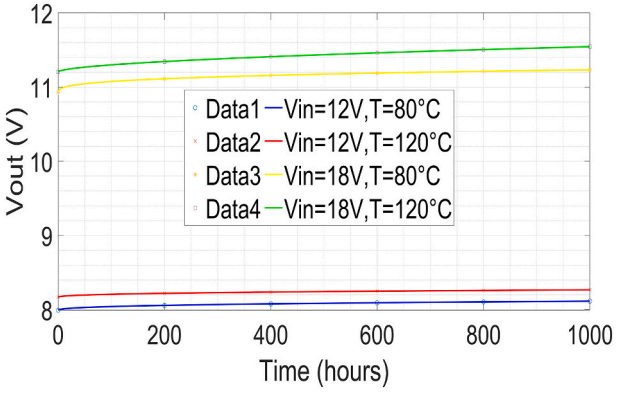

Fig. 4. Degradation path model fitted to the output voltage data of the regulator at different stress conditions.

Table 1
Degradation model parameters and TTF under different stress conditions.

Parameters	12 V, 80 °C	12 V, 120 °C	18 V, 80 °C	18 V, 120 °C
μ	0.01	0.045	0.007	0.008
ϒ	0.372	0.285	0.453	0.548
D	7.988	10.91	8.132	11.20
TTF/h	22,392	6846	13,536	2490

$$TTF = \left(\frac{V_{th} - D}{\mu}\right)^{1/\gamma} \tag{3}$$

3.2. Reliability estimation: life data analysis

Life data analysis was used to predict the lifetime distribution of the regulator and estimate the required reliability parameters at the applied stress conditions and defined threshold level. Stress parameters (e.g. voltage and temperature) were applied simultaneously to increase acceleration factor and performance degradation of the regulator. Hence, the life-time (L) relying on these stress parameters is modelled by combining Arrhenius relationship and inverse power law model for temperature and voltage stress respectively as provided in Eq. (4). The expression in Eq. (4) consist of several unknown parameters, where L is the nominal life that can be represented as characteristic life of the Weibull distribution, A, B and C are the stress dependent constants that depends on failure criterion and product design. Besides the activation energy (E_a) with a value of 0.75 eV is considered for the studied regulator, k corresponds to Boltzmann constant in J/K or eV/°C and T is temperature in kelvin (K). The relationship between L and both stress parameters (T and V_{in}) is expressed in Eq. (4), where the last term Cln (V_{in}) or Clog(V_{in}) inside the exponential has been provided to indicate that the interaction between T and V_{in} is strongly evident [14]. The resulting expression can be simplified by assuming that this last term is non-existent if significant effect of both T and V_{in} on L is not evident. Consequently, the simplified expression would account for the relationship between L and (T and V_{in}) to be modelled individually or independently by the Arrhenius and inverse power relationship.

$$L = A \Big/ {V_{in}}^{B} exp\left(\frac{E_a}{kT}\right) exp\left(\frac{Clog(V_{in})}{kT}\right) \tag{4}$$

The life data (probability of failure) expressed in percentile at corresponding failure time for different stress combinations is plotted in Fig. 5. The data plotted on the logarithmic graph corresponds to the pseudo lifetime (hours) failure on x-axis for different voltage and temperature stress level. Nominal condition refers to the nominal temperature at 25 °C. The parallel lines for the logarithmic fits produced by applying the Weibull distribution display shape parameter β is independent of voltage and temperature stress, while the scale parameter (η) is dependent on different stress levels at defined threshold criterion. Higher lifetime reliability of the regulator was predicted (around 9000 h at 12 V, 120 °C against 5000 h at 18 V and 120 °C) for 99 % failure probability. The Weibull distribution plot presented in Fig. 5 allows the linear interpolation of the plotted data to the specified degradation criterion (5 % voltage output drift from nominal value). Table 2 shows the value of the shape (β) parameter is constant and >1 (β > 1), which means that the regulator degraded with increasing non - constant failure rate (λ) in the wear - out phase of the bathtub curve.

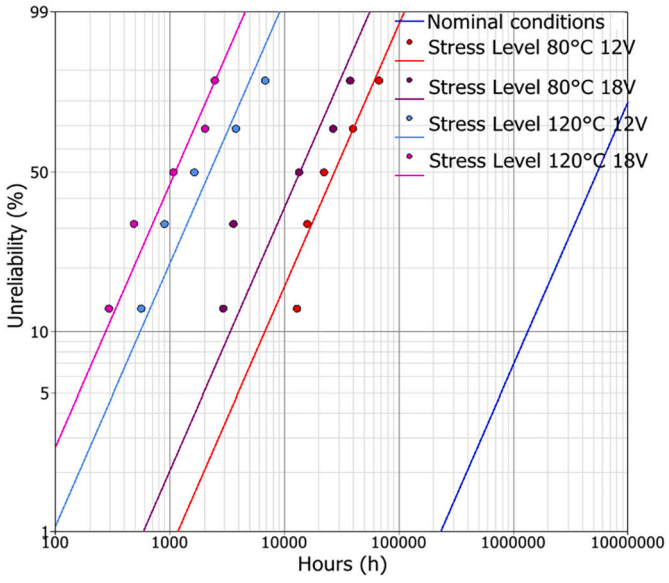

Fig. 5. Weibull distribution fits to pseudo failure time at different stress conditions.

The application of Weibull's distribution was found to more suitable for applying linear regression model to best fit the degradation data. The construction of reliability models based on Weibull's distribution has enabled to extract and estimate reliability parameters, including pseudo time-to-failure (TTF) for different stress conditions only in the wear - out stage of the regulator's bathtub curve. The Weibull's distribution was applied to the degradation behavior of the regulator due to being more suitable compared to other statistical distributions (i.e. exponential and log-normal) for characterizing both the useful life period and wear – out phase in the bathtub curve of this device. The shape parameter β of this distribution allows obtaining valuable information on failure modes or mechanisms at different phases of the bathtub curve. The shape parameter β value is <1, indicates that the device demonstrates random degradation with constant failure rate λ in the useful phase of the bathtub curve.

Data measurements from experiments are usually preferable prior to applying the Weibull distribution or log-normal distribution methods to evaluate or accurately predict reliability parameters, such as: failure in time, TTF from degradation data when subjected to specified stress conditions. However, the limitation or the weakest- link property of this type of distributions, lies mostly on the difficulty of computing accurate estimation of reliability parameters, i.e. the pseudo TTF, failure in time, probability of failure and so on, for any untested or undefined ageing stress operating conditions.

Maximum likelihood estimation (MLE) method, with the aid of Weibull distributions, was applied using the quantified sets of TTF data under specific threshold and stress conditions, enabled to obtain reliability estimation parameters using Weibull++ software [15]. Table 2 provides numerical values of the accelerated life test analysis. These estimated parameters would enable to determine lifetime data for failure under any operating conditions.

4. Conclusion

This paper demonstrated the interest of using a simulation model of the designed voltage regulator to assess the reliability estimation from the accelerated degradation data. The objective was achieved by developing the numerical model for extracting the output voltage as a function of temperature and input voltage. Moreover, a methodological

Table 2
Reliability model estimation parameters under different accelerated stress conditions.

Parameters	Data (value)
Shape (β)	1.34
Scale (η)	7.08E+06
A	5.02E−05
B	−1.13
C	−42.10

approach was proposed to generate the output voltage degradation data under accelerated conditions based on the knowledge of predictive reliability analysis for the regulator according to the FIDES standard. Failure threshold was extracted at two different voltage and temperature stress conditions to estimate the pseudo failure lifetime from the degradation data. With the use of simulated test data, a suitable acceleration law model was then adopted to predict the reliability parameters of the regulator under accelerated conditions.

It was shown that the estimated lifetime reliability of the regulator is significantly higher at lower accelerated ageing conditions (around 90,000 h at 12 V, 80 °C against 5000 h at 18 V, 120 °C) for 99 % failure probability. Hence, the regulator was found to have significantly higher pseudo TTF, depending on the magnitude of ageing stress type (voltage and temperature) conditions.

Future perspective of this ongoing research work would involve comparing the simulation and measurement ALT results to develop an accurate reliability model that would be integrated with the immunity model to predict EMC performance of the regulator.

CRediT authorship contribution statement

Jaber Al Rashid: Conceptualization, Methodology, Data curation, Formal analysis, Writing – Original draft.
Laurent Saintis: Software, Validation, Writing – Review and editing, Funding acquisition.
Mohsen Koohestani: Validation, Visualization, Writing – Review and editing.
Mihaela Barreau: Supervision, Project administration.

Declaration of competing interest

None.

Data availability

The data that has been used is confidential.

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