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Frédéric Richardeau, Yazan Barazi. Predictive gate ageing-laws of SiC MOSFET under repetitive short-circuit stress. *Microelectronics Reliability*, 2022, pp.114706. <10.1016/j.microrel.2022.114706>. <hal-03791964v2>

HAL Id: hal-03791964

<https://hal.science/hal-03791964v2>

Submitted on 29 Sep 2022

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Predictive gate ageing-laws of SiC MOSFET under repetitive short-circuit stress

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Abstract This paper proposes SiC MOSFET gate ageing-laws under repetitive short-circuit stress. Based on analytical studies, physical forms and preconditioning data, numerical fitting based on stress variables ΔT_j , $T_{Pulse\ Gate\ Damage\ \%}$ and E_{sc} is proposed. Accuracy and prediction capabilities of ageing-laws have been evaluated and compared. Resulting in suggesting a new ageing-law based on ΔT_{Al_Top} metal-source. This one gives the best fitting accuracy. Finally, the ageing-law based directly on the short-circuit energy E_{sc} appears to have the best in prediction capability.

1. Introduction

SiC MOSFETs increase the power converter efficiency [1]. Today, it is mandatory to guarantee operational level of reliability and robustness capabilities in accidental extreme operation. However, due to a higher current density and shorter channels in planar structure, the short-circuit (SC) withstanding time ($T_{SCWT} @ 2/3 \times V_{DSmax}$) of SiC MOSFETs is lower than silicon devices one, within $t_{SCWT} = 2\mu s$ instead of $t_{SCWT} = 10\mu s$ for Si IGBTs. Many efforts have been recently addressed to study dedicated SiC MOSFETs failure mechanisms under short circuit tests [2,3]. High temperature variations lead to have cumulated thermo-mechanical stresses around the gate-region and Al source-metal. Those often lead for the SiC MOSFET not being able to exceed the threshold of 1000 repeated short-circuit cycles, derived from the silicon standard. The prediction of the number of short-circuit cycles allowed by the SiC MOSFET, before its gate is damaged, is a fact that is not well known today and yet it is of prime concern in the operational phase. In [4], a Weibull distribution and a direct ΔT_j Coffin-Manson ageing-law were proposed but under reduced drain-source voltage bias 200V and using a gate-trench device. In [5], authors experimentally confirm the gate-ageing dependence with ΔT_j stress but the Coffin-Manson parameters were not fitted and the prediction capability was not proposed.

In this paper, repetitive SC study has been led in order to model and to propose a set of predictive analytical gate-ageing laws on a SiC MOSFET

device. Proposed fitted laws have been evaluated in terms of accuracy, practicality and prediction capability for a shorter SC stress than ones used in the fitting operation. The paper is organized as follow: in §2. SC test bench and methodology are presented; in §3. dedicated thermal simulations, modelling and prediction tests are analyzed; finally, in the conclusion, best accurate and predictive laws are highlighted.

2. Repetitive short-circuit stress

2.1. DUT and test bench used

This study is a continuous analysis of the second-generation ST MicroelectronicsTM device 1200V, 75m Ω , 33A @ $T_{Case} = 25^\circ C$ planar-gate type device, in an automotive-grade 3-lead TO247 case [6, 7]. The device was placed under extreme short-circuit mode, which is known as Hard Switch Fault HSF. The DUT (Device Under Test) was placed on the low side of a phase-leg power test bench presented in Fig. 1. A copper clip is used at the high-side socket to replicate the SC behavior. A 10 μF -720V decoupling capacitor is soldered closest the phase-leg including a 2nH coaxial shunt. The total stray inductance of the equivalent power loop is 15nH. With less than 2 joules stored, there is no risk of case explosion, allowing relevant failure analysis to be performed on the chips. Tank capacitors are used upstream to provide instantaneous short-circuit power for 100 μs max. (200J). To secure this stage, a fast IGBT electronic breaker (800ns) and two fast CMS fuse-bars are used. Low voltage signals (as

V_{Drv} and V_{GS}) are measured with self-compensated voltage probes (Tektronix TPP1000 - 300V, 1GHz bandwidth). High voltages (as V_{DS}) are typically measured with a probe (Tektronix TPP0850 - 1000V, 800MHz bandwidth). The current (I_{DS}) is measured through a 2GHz coaxial shunt. I_{GS} waveform is traced on the scope by the operation : $(V_{Drv} - V_{GS}) / R_{Gate}$.

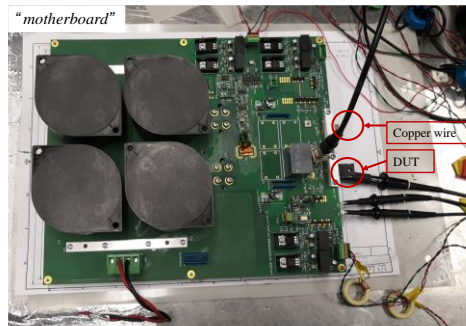


Fig. 1. Secure SC test-bench: max 600V, 400A, 100 μ s, 125°C.

2.2. Set-up, methodology and experimental results

Previous work [6] have shown for the same device, under the same power bench and under the same condition ($V_{DS} = 600V$, $V_{Drv} = -5V/18V$ and $T_{Case} = 25^\circ C$), that average $T_{Pulse\ Gate\ Damage} = 4.9\mu s$ with a safe gate damage-mode. In this paper, a repetitive short-circuit test is applied including a turn-off of 5s between each pulse. Different percentages of $T_{Pulse\ GD}$ have been used, giving $T_{Pulse\ GD\ \%}$: 50%, 60%, 70%, 80% and 90% respectively equal to a pulse width T_{Pulse} : 2.5 μ s, 3 μ s, 3.5 μ s, 4 μ s and 4.5 μ s. Three devices have been chosen for each percentage. Fig. 2 presents for 70% $\times T_{Pulse\ GD}$; a behavior comparison between the first SC cycle and the 593th SC gate-damage cycle. A permanent gate-leakage and a gate-source voltage depolarization by the external gate-resistor clearly appears. In all stresses, drain-source voltage was limited to 600V to avoid possible thermal runaway and then catastrophic drain-source failure-mode.

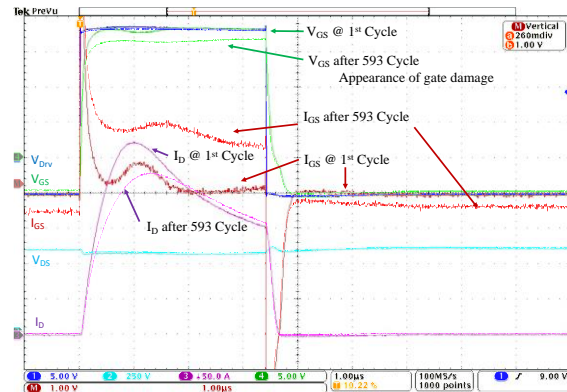


Fig. 2. (V_{GS} , V_{Drv} , I_{GS} , V_{DS} , I_D) Oscilloscope waveforms under repetitive SC @70% of $T_{Pulse\ GD}$, $T_{Pulse\ GD\ 70\%} = 3.5\mu s$. @ $V_{DS} = 600V$, $R_G = 47\Omega$, $V_{Drv} = -5V/18V$.

3. Gate-ageing modelling and prediction

3.1. Transient thermal simulation

In order to prepare the modelling step, all stress points from §2 has been thermally simulated to extract junction temperatures ΔT_j and Al top source-metal $\Delta T_{Al\ Top\ Metal}$ temperature variations on the top of the gate-region, where the damage is developed. A dedicated electro-thermo-metallurgical model developed by authors [8] is re-used. This one considers the temperature dependency of thermal conductivity and mass heat of the SiC from [10] as defined in (1) and (2), as well the solidus-liquidus phase transition of the upper Al layer from [11]. Using Comsol™ software, $I_{DS}(t)$ waveforms from §2.2 is used as input data of the model with $V_{DS} = 600\ V$. Fig. 3 a) presents a thermal simulation under the shortest pulse time $T_{pulse} = 2.5\mu s$ (50%), the figure is supported by its respective $I_D(t)$ waveform. It shows that the Al top source-metal temperature just exceeds the solidus-liquidus phase transition band ($933K \pm 30K$) for 2 μ s. Conversely, Fig. 3 b) presents a thermal simulation under the longest pulse time $T_{pulse} = 4.5\mu s$ (90%). The figure is supported by its respective $I_D(t)$ waveform. In this last extreme stress test, it shows that the Al top source-metal temperature is greatly above the solid-liquid phase transition band for 11 μ s. It can be noted that the ILD-SiO₂ mechanical strength temperature around 600K [9] is clearly exceeded in all these cases. Therefore, all these results confirm the existence of favorable mechanical and metallurgical conditions for the gate-region to be subject to

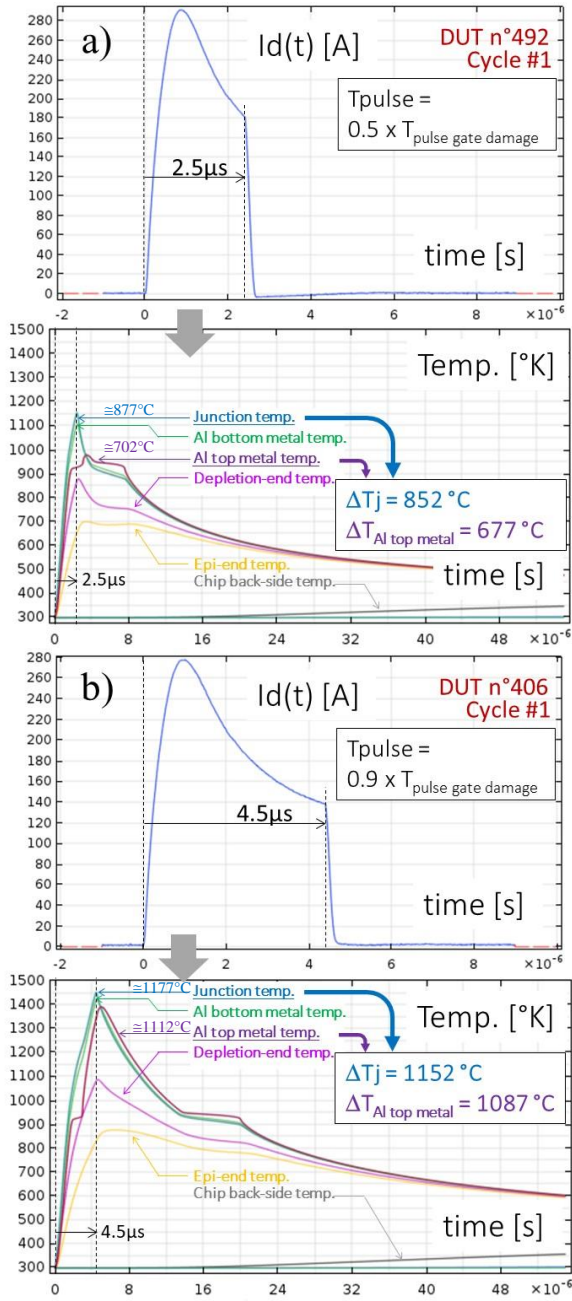


Fig. 3. Transient thermal simulation in short-circuit stress,
 a) Shortest pulse 2.5µs, b) Longest pulse 4.5µs.
 @V_{DS} = 600V, V_{Drv} = -5V/+18V, R_{Gate} = 47Ω,
 T_{Case} = T_{Amb}

thermo-mechanical ageing.

$$\lambda_{SiC} = (-0.0003 + 1.05 \cdot 10^{-5} T)^{-1} \quad (1)$$

$$Cp_{SiC} = 925.65 + 0.3772 T - 7.9259 \cdot 10^{-5} T^2 - 3.946 \cdot 10^7 T^{-2} \quad (2)$$

With [10]: λ_{SiC} , SiC thermal conductivity; Cp_{SiC} , SiC heat capacity. Note that Al layer solidus – liquidus phase transition thermal laws ($T_{s \rightarrow l}$) are much more non-linear and complex in form and are described in [11] for $\lambda_{Al}(T_{s \rightarrow l})$ and $Cp_{Al}(T_{s \rightarrow l})$. A latent heat of melting $L_{fAl} = 397 \text{ kJ/kg}$ over a $\Delta T_{s \rightarrow l}$ range of 30K is considered to allow the convergence of the model.

3.2. Distribution $Nb_{cycles}(\Delta T_j)$ results

Fig. 4 shows an overview of the cycling results distribution from §2.2, versus the temperature variation ΔT_j simulated by the transient thermal model in §3.1. Temperature variation is defined by: $\Delta T_j = T_{jmax} - T_{amb}$. The general shape of the scattered points reveals a non-linear behavior specific to ageing effect. However, three of the four stress points @T_{Pulse GD 90%} are too far apart to be considered in the fitting. Indeed, this high level of thermo-mechanical stress can cause early damage in a very small number of cycles on weak components. Only one point [$\Delta T_j = 1152^\circ\text{C}$, $Nb_{cycles} = 180$]; which is not off-trend; is retained as it greatly improves the global quality of the next fitting operation.

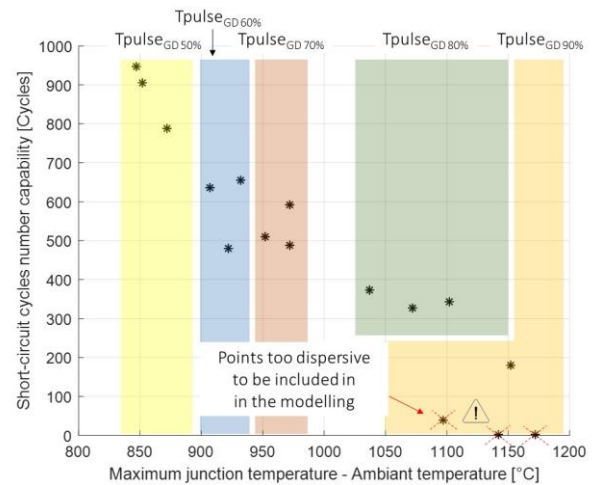


Fig. 4. Scatter plotting of §2. results versus ΔT_j @V_{DS} = 600V, V_{Drv} = -5V/+18V, R_{Gate} = 47Ω.

3.3. $Nb_{cycles}(\Delta T_j)$ fitting law

Two general ageing-laws have been numerically fitted from the scatter plotting in Fig. 4; a power law (1) as a Coffin-Manson form and an exponential law (2). These two laws are based on offset parameters (A_{pj} and A_{ej}) and shape factor parameters (B_{pj} and B_{ej}). These coefficients have been adjusted using a Levenberg-Marquardt optimization algorithm in Matlab™. This algorithm is known and used for its robustness and ability to find a global minimum even with spread initial conditions. The quality of the fitting will be given by the coefficient of determination R-square.

$$Nb_{cycles\ pj} = A_{pj} \Delta T_j^{-B_{pj}} \quad (3)$$

$$Nb_{cycles\ ej} = A_{ej} e^{-B_{ej} \Delta T_j} \quad (4)$$

Results of the fitting using stress variable ΔT_j are given in Fig. 5. Both laws fit very well and are very close, respectively $R_{pj\text{-square}} = 0.9293$ for the power law and $R_{ej\text{-square}} = 0.9248$ for the exponential law. It can be observed that the power law fits slightly better around stress point @ $T_{Pulse\ GD\ 50\%}$, whereas the exponential law fits slightly better when approaching stress point @ $T_{Pulse\ GD\ 90\%}$. The power law is therefore more interesting to keep for predicting the cycles number @ $T_{Pulse\ GD\ X\%} < @T_{Pulse\ GD\ 50\%}$.

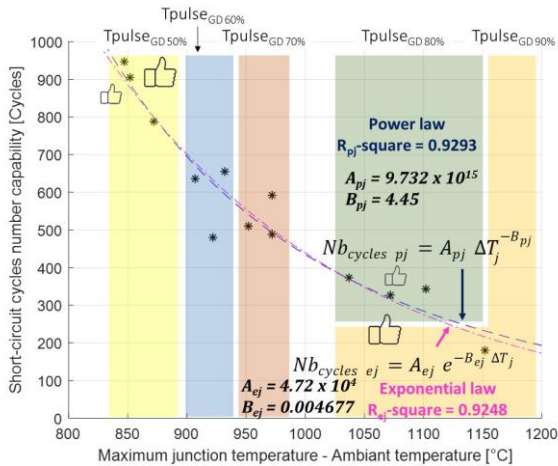


Fig. 5. $Nb_{cycles}(\Delta T_j)$ fitting laws and parameters @ $V_{DS} = 600V$, $V_{Driv} = -5V/+18V$, $R_{Gate} = 47\Omega$.

3.4. $Nb_{cycles}(T_{Pulse})$; $Nb_{cycles}(E_{sc})$;

$Nb_{cycles}(\Delta T_{Al\ Top\ Metal})$ fitting laws and synthesis

Three others ageing-laws, based on power and exponential forms, have been evaluated in terms of accuracy, using variables pulse time $T_{Pulse\ GD\ \%}$, SC energy E_{sc} and $\Delta T_{Al\ Top\ Metal}$ in place of variable ΔT_j in (1) and (2).

Stress variable $T_{Pulse\ GD\ \%}$ is simply and directly based on the gate-pulse signal. Scatter plotting versus $T_{Pulse\ GD\ \%}$ and results of the fitting are illustrated in Fig. 6. With $R_{pT\text{-square}} = 0.8936$ for the power law and $R_{eT\text{-square}} = 0.8912$ for the exponential law, the average fitting quality is 4% slightly lower than the fitting quality with variable ΔT_j . In addition, with $B_{pT} \cong B_{pTj}/2$ we verify physically that thermal diffusion follows a law close to the square root of time.

SC energy variable E_{sc} can be "quite easily measured" from the scope or post-processed from the recorded $I_{DS}(t)$ and $V_{DS}(t)$ waveforms, without use of complex transient thermal simulation. Scatter plotting versus E_{sc} and results of the fitting are illustrated in Fig. 7. With $R_{pE\text{-square}} = 0.9193$ for the power law and $R_{eE\text{-square}} = 0.9255$ for the exponential law, the average fitting quality is only 0.5% lower than the fitting quality with variable ΔT_j . Thus, these gate ageing-laws promise to be a good compromise between precision and "easy to use".

In contrast we suggest introducing in this study a new stress variable $\Delta T_{Al\ Top\ Metal}$ calculated from the transient thermal simulation described in §3.1: indeed, as illustrated in Fig. 3 a) and b), the gate-damage mode seems to be correlated to the existence of a solidus - liquidus phase transition of the Al top source-metal layer combined with a mechanical strength of the ILD around the gate fingers. The scatter plotting versus $\Delta T_{Al\ Top\ Metal}$ and results of the fitting are illustrated in Fig. 8. With $R_{pAl\ square} = 0.9209$ for the power law and $R_{eAl\ square} = 0.9303$ for the exponential law, the average fitting quality is only 0.15% lower than the fitting quality with variable ΔT_j . However, note specifically that $R_{eAl\ square}$ value is the best of all others R-square values, showing that the variable $\Delta T_{Al\ Top\ Metal}$ combined with an classical exponential law provide the best fitting at the expense of greater complexity of use because such variable requires a transient thermal simulation.

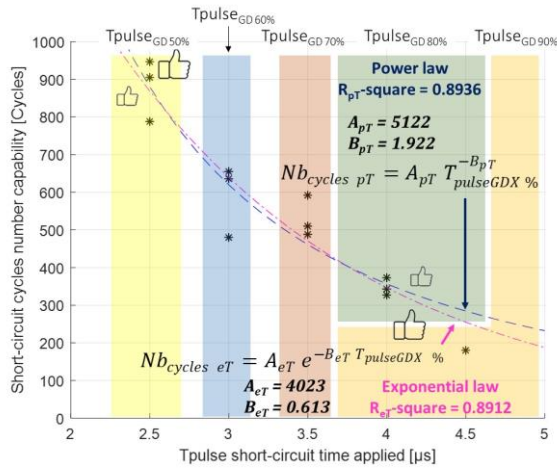


Fig. 6. $Nb_{cycles}(T_{pulse\ GD\ \%})$ fitting laws and parameters @ $V_{DS} = 600V$, $V_{Drv} = -5V/+18V$, $R_{Gate} = 47\Omega$.

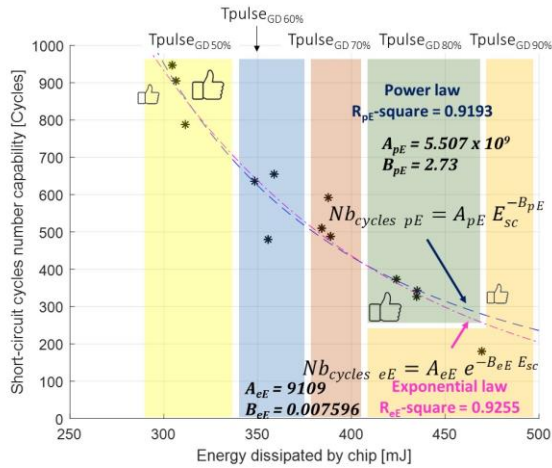


Fig. 7. $Nb_{cycles}(E_{sc})$ fitting laws and parameters @ $V_{DS} = 600V$, $V_{Drv} = -5V/+18V$, $R_{Gate} = 47\Omega$.

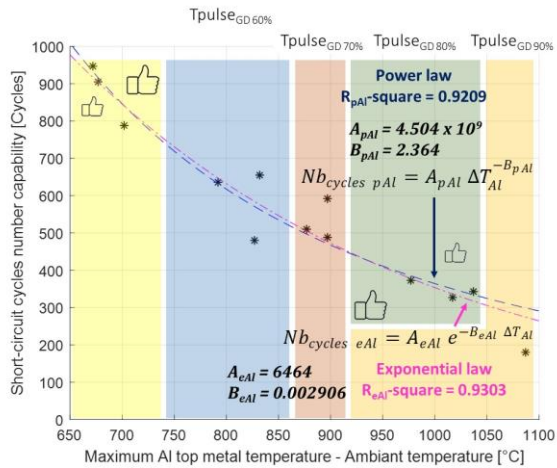


Fig. 8. $Nb_{cycles}(\Delta T_{Al_Top_Metal})$ fitting laws and parameters @ $V_{DS} = 600V$, $V_{Drv} = -5V/+18V$, $R_{Gate} = 47\Omega$.

In summary, Table 1 gives the ranking fitting performance considering the impact of all described variables. As previously analyzed, $\Delta T_{Al_Top_Metal}$ variable with exponential law provides the best fitting. This result can be explained by considering the temperature variation closest to the gate-damage region. However, the use of this variable requires a transient thermal simulation of the chip. Conversely, the $\Delta T_{pulse\ GD\ X\ \%}$ variable gives the worst results but does not require simulation.

Table 1 Quality of the gate-ageing laws fitting based on R-square performance.

Ranking	R-square and law type	Ranking	R-square and law type
1 (best)	0.9303 exp. $\Delta T_{Al\ Top}$	5	0.9209 pow. $\Delta T_{Al\ Top}$
2	0.9293 pow. ΔT_j	6	0.9193 pow. E_{sc}
3	0.9255 exp. E_{sc}	7	0.8936 pow. $\Delta T_{pulse\ GD\ \%}$
4	0.9248 exp. ΔT_j	8 (worst)	0.8912 exp. $\Delta T_{pulse\ GD\ \%}$

3.5. Prediction capability test

All previous laws are now subject to a prediction test with $\Delta T_{pulse\ GD\ X\ \%} < 2.5\mu s$. Indeed, under low pulse duration, the cycling capability becomes high, which makes experimentation complicated and expensive. The prediction capability then becomes useful. A first test considering $\Delta T_{pulse\ GD\ 40\ \%} = 2\mu s$ did not allow to yield experimentally a gate-damage in less than 3000 cycles. Indeed, on this low stress level the temperature variation does not reach the onset of the solidus-liquidus phase transition. Hence, a change in the damage-mode and ageing-laws are to be expected such as the Al grain boundaries reconstruction. In order to keep the initial damage-mode on the gate-region as the basis for the proposed modelling, $\Delta T_{pulse\ GD\ 45\ \%} = 2.25\mu s$ is retained. This stress level leads experimentally to $Nb_{cycles} = 1270$. On this stress point, all new variables ΔT_j , E_{sc} and $\Delta T_{Al\ Top\ Metal}$ are calculated or simulated in Comsol™ and injected in all the proposed ageing-laws in §3.3 and §3.4 to compare their prediction capability with experience. Results and ranking are given in Table 2.

Table 2 Prediction performance of the fitted gate ageing-laws.

T_{Pulse GD 45%} - Prediction performance		
Nb cycles target (experimentation) = 1270		
Ranking	Law type and variable	[Min, Max]* prediction Nb cycles
1 (best)	pow. E_{sc}	[1043, 1391]
2	exp. E _{sc}	[1006, 1254]
3	pow. ΔT _j	[986, 1228]
4	exp. ΔT _j	[964, 1163]
5	pow. ΔT _{Al Top}	[1050, 1090]
6	exp. ΔT _{Al Top}	[1009, 1039]
7	pow. ΔT _{Pulse GD %}	1077
8 (worst)	exp. ΔT _{Pulse GD %}	1012

* : considering I_{Dmax} at 1st cycle and I_{Dmin} at last cycle due to V_{GSth} slight drift during cycling test.

- The $T_{Pulse GD X\%}$ based law gives a confirmation of the worst estimation, as was found in the fitting ranking based on R-square.

- The power form based on E_{sc} is the best in prediction @T_{Pulse GD 45%} although it is slightly less good in global fitting quality for T_{Pulse GD %} > 45%.

- Temperature laws (ΔT_j , and $\Delta T_{Al Top Metal}$) are acceptable and can be clearly used. They allow cycles prediction with less than 20% deviation compared to the experimental result.

4. Conclusion

SiC MOSFET planar gate-ageing laws in repetitive short-circuit stress are proposed. Stress variables ΔT_j , $T_{Pulse Gate Damage \%}$ and E_{sc} are considered. Based on analytical physical forms, preconditioning data and numerical fitting, accuracy and prediction capability have been evaluated and compared. A new ageing-law based on stress variable $\Delta T_{Al Top metal}$ -source is suggested. This one gives the best fitting accuracy but requires a transient thermal simulation in addition of the experimental test. Finally, the ageing-law based directly on the practical short-circuit energy E_{sc} appears the best suited in prediction capability without requiring a post-simulation process.

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