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12 kV 1 kA Breaking Capable Modular Power Electronic Interrupter with Staged Turn-off Strategy for Medium Voltage DC Hybrid Circuit Breaker

Jian Liu, *Student Member, IEEE*, Lakshmi Ravi, *Student Member, IEEE*, Cyril Buttay, *Senior Member, IEEE*, Rolando Burgos, *Senior Member, IEEE*, Steve Schmalz, Andy Schroedermeier, Z. John Shen, *Fellow, IEEE* and Dong Dong, *Senior Member, IEEE*

Abstract- The dc circuit breaker (DCCB) plays an important protection role in the dc distribution systems. Hybrid dc circuit breaker (HCB) offers low conduction losses and reasonably fast response times. In this paper, a high power density, modular and scalable power electronic interrupter (PEI) design is introduced for medium voltage (MV) HCB platforms. Following this concept, the single low-voltage (LV) module is first investigated in terms of the high pulse current ratio and the voltage clamping circuit. After the comparison and test among different devices, a compact module with 1.7 kV discrete IGBTs are selected as main switches. While the voltage clamping circuit is carefully designed to guarantee no tail current bump and sufficient turn-off voltage margin. Next the whole system with series modules is optimized on the aspects of the turn-off strategy, power supply structure and layout of modules. An improved staged turn-off scheme is proposed, which can not only reduce the peak current and total metal oxide varistor (MOV) energy, but also help balance the MOV energy distribution. A 12 kV and 1 kV breaking capable PEI was demonstrated based on the proposed PEI design, achieving a peak power density of 7.4 kW/cm³, much higher than the IGBT module-based solution. The breaking capability and effectiveness of the modular PEI is demonstrated in a 6 kV MVDC HCB device.

Index Terms- Hybrid DC circuit breaker, power electronic interrupter, high power density, staged turn-off, integration.

I. INTRODUCTION

Dc circuit breaker (DCCB) is a key enabler for the development of the medium-voltage direct-current (MVDC) distribution systems [1-3]. However, the lack of natural current zero crossings and the faster rise speed of DC fault currents are some of the challenges for DCCB [4]. Therefore, the fast reaction time, low conduction loss and reliable breaking capability are the desired features for DCCB.

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Conventional mechanical circuit breaker (MCB) employed in the ac system require 4-5 cycles to interrupt the fault current, but will cause arc erosions in the dc system. If a passive or

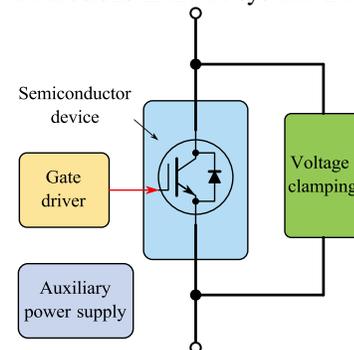


Fig. 1 The typical structure and major components of PEI.

active resonant circuit is added to create the required current zero crossing, MCB can be effectively adopted for the dc applications [5]. The solid-state circuit breaker (SSCB) based on semiconductor devices could interrupt the fault current quickly without any arc issue, but it suffers from the high conduction loss during the normal operation [6], [7]. On the contrary, the hybrid circuit breaker (HCB) combines the low loss advantages of mechanical switches with the fast response times offered by power electronic interrupter (PEI) [8], [9].

Numerous HCB schemes have been proposed in the past as comprehensively surveyed in [10], among which the HCB concept invented by ABB has achieved considerable success in HVDC applications [11] and is well poised to proliferate into the MVDC space. The ABB topology, like other HCB solutions, utilizes a mechanical branch to conduct the nominal load current, and an electronic branch in parallel to commutate and interrupt the fault current. Its mechanical branch includes a distinct design of a load commutation switch (LCS) in series with the ultrafast mechanical switch. The fault current can be forced to commutate from the mechanical branch to the electronic branch by turning off the LCS, thus allowing the arcless opening of the mechanical contacts under a zero-current condition. However, LCS introduces more conduction loss in the main branch and the cooling system may increase complexity and maintenance cost. Another solution to HCB with no conduction loss was proposed in [12], which adopts a current commutation drive circuit (CCDC) to commutate the current reliably and quickly. This structure has been used in

multiple 500kV/25kA 3ms HCBs, which are being equipped in Zhangbei Flexible DC power grid [13].

Currently most HCBs are used for the HVDC grid, which focuses on the conduction loss, manufacturing cost, current interruption capability and maintenance convenience [14]. However, the power density is also an important factor to shrink the size and volume for the shipboard [15] and aircraft applications [16]. Therefore, this paper focuses on the high power density design of HCB, especially the PEI part. The major components of PEI are shown in Fig. 1 [17], including the semiconductor devices, voltage clamping circuit, gate driver and the auxiliary power supply. The main switch of semiconductor devices are the most important components. The standard bulky and expensive power modules are designed for the repetitive switching converters, where devices confront the electrical and thermal stress. On the contrary, the short pulse of surge current and only a few fault events during the whole lifetime post the different requirements for PEI [18]. Therefore, the PEI design is quite different from the normal PWM converters. The contribution of this paper could be summarized as below.

- 1) The modular concept is used to build a compact PEI.
- 2) The trade-off analysis and limiting factors of different components in single module are discussed in detail.
- 3) An improved staged turn-off strategy is proposed to balance MOV energy.
- 4) The auxiliary power supply with high insulation capability is employed to support the whole system, and the cascaded power supply structure is utilized for the gate driver inside PEI.

This paper is organized as follows. In section II, the modular PEI concept and the design procedure is explained. The single module is discussed first, including the surge current conduction and interruption capability of solid-state devices, and the trade-off of the voltage clamping circuit. Two parts together determine the structure and parameters of each PEI module. Next in section III, the staged turn-off strategy is introduced and two methods are proposed to balance the MOV

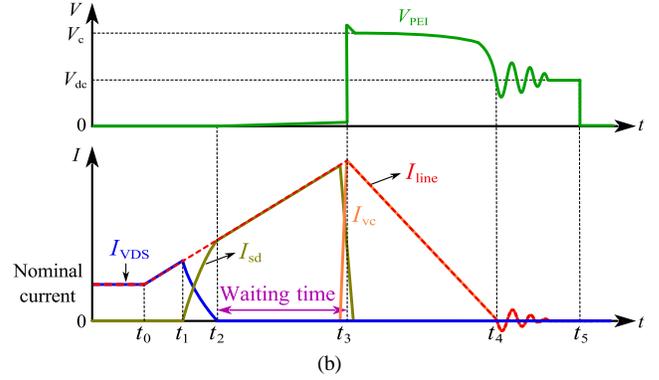
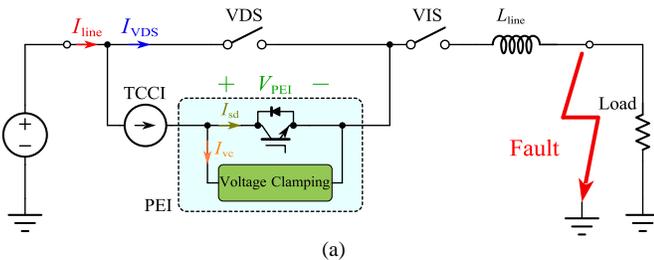


Fig. 2 (a) Structure of a HCB, (b) the operation sequence and waveforms of HCB.

energy. A LCCL-LC resonant power supply based on the current link is designed to supply power to PEI and TCCI as well as provide enough isolation voltage. The PEI modules are integrated into a compact package and verified using the electric-field (E-field) simulation models and partial discharge (PD) results. In section VI, a 6 kV surge current platform is established to test the functionality of PEI alone and the entire packaged HCB. The obtained experimental results validate their effectiveness. Finally, section V draws the conclusion.

II. MODULAR PEI AND SINGLE MODULE DESIGN

A. HCB Structure and Modular PEI

Fig. 2(a) depicts the topology of developed HCB [19], which consists of four parts: the ultrafast vacuum disconnect switch (VDS), vacuum isolation switch (VIS), the transient commutation current injector (TCCI) and PEI. The VDS and VIS have favorable characteristic of arc extinguishing at zero current, and uses the Thomson coil actuators to realize the fast opening of vacuum interrupter (VI) [20]. The TCCI could be regarded as a controllable current source based on the buck converter [19], which can track the line current and inject a current with the opposite direction to create the zero current condition for VDS. As for the PEI, it is responsible for conducting and cutting the pulse surge current and is the focus of this paper.

A simple turn-off sequence and waveform is shown in Fig. 2(b). At the normal state, the current flows through the closed VDS, so the loss is very low. After a fault occurs at t_0 , and the fault current threshold is reached at t_1 , the TCCI works to transfer the current from the VDS to the PEI branch. When I_{VDS} reaches zero at t_2 , a trip command is issued to the VDS and once a sufficient contact separation is achieved at t_3 , the solid-state switch is gated off. The current then commutates to the voltage clamping circuit, which generates a clamping voltage V_c higher than dc bus voltage V_{dc} to clear the fault current. After current is reduced to zero at t_4 , the snubber circuit of PEI resonates with L_{line} , causing voltage and current oscillations. Finally, the VIS is opened at t_5 with a small leakage current and the voltage across the PEI drops to zero.

In this 6 kV HCB, the PEI is designed to generate a peak clamping voltage V_c of 12 kV to clear the fault current of 1 kA. Although some high voltage devices have been designed,

such as the 15 kV silicon carbide (SiC) emitter turn-off thyristor (ETO) [21], SiC MOSFET [22] and SiC insulated gate bipolar transistor (IGBT) [23], more devices should be connected in parallel for the conduction and interruption of 1 kA surge current. Besides, these devices are not commercial products and the long-term reliability is still unknown.

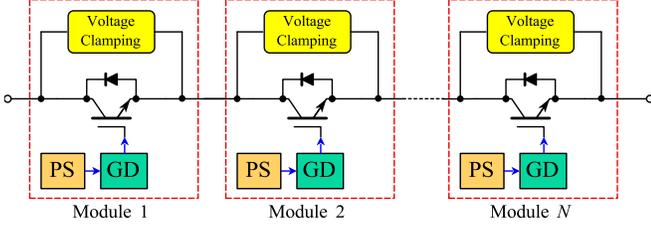


Fig. 3 Modular PEI with distributed voltage clamping circuit.

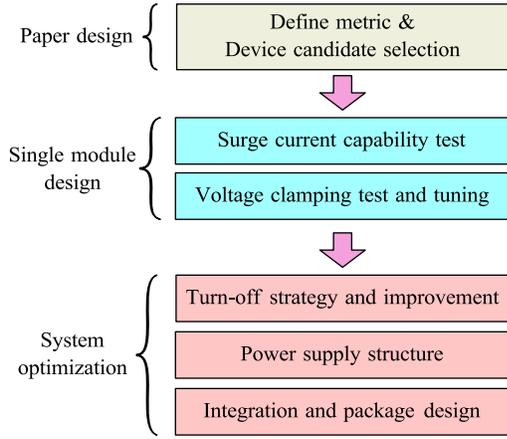


Fig. 4 Design procedure for PEI.

Another solution to reach high voltage is series connection of low voltage devices, and the main challenge is the voltage sharing [24], [25]. Therefore, the modular structure as shown in Fig. 3 has been adopted in most PEI topologies [26]. For example, the Zhangbei 500 kV HCB uses 320 series modules [13]. The distributed voltage clamping circuit paralleled with low voltage device could be regarded as one module, whose maximum voltage is thereby limited and the voltage sharing is realized naturally. Besides, the consistency and parameter tolerance requirement for the devices becomes lower, and the good scalability implies that this solution could be applied to the higher voltage cases. Another advantage of this concept is that the cascading damage can be avoided even one of the series modules is damaged.

Following the modular concept, the design procedure of a high power density PEI is given in Fig. 4. In this first step of ‘paper design’, the commercial devices are collected and compared in terms of the current density according to the value of datasheet. Then in the second step, the surge current conduction and interruption tests are performed for the selected candidates. Two types of voltage clamping circuit, the single module design could be determined. Next the whole system is optimized including turn-off strategy, power supply structure and integration based on the series modules.

B. Selection of Solid-state Devices

Since a modular structure could handle the 12 kV clamping voltage, the challenge is how to achieve conduction and safe interruption of 1kA surge current. According to I_{PEI} in Fig. 2(b), the requirements for the devices should be, 1) conduction of over-current without desaturation between t_2 and t_3 , 2) cut-off of peak current at t_3 , and 3) the junction temperature $T_{j,max}$ should not be exceeded during the whole process. Based on the investigation from [16], the IGBT shows superior performance in terms of the much higher surge capability for single switching applications. Therefore, it is selected for use in this work.

High power density is the design target for the PEI, and the IGBT package plays an important role. Several commercially available IGBT packages (including discretely and modules) are surveyed and summarized. The most important metric for this comparison is the current density as calculated by (1).

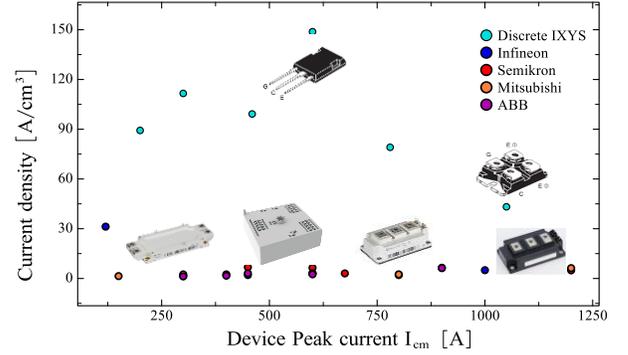


Fig. 5 Peak current density of commercial 1.7 kV IGBT.

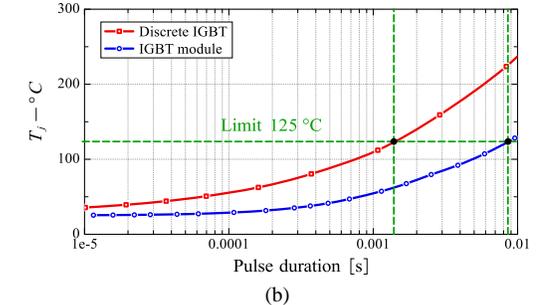
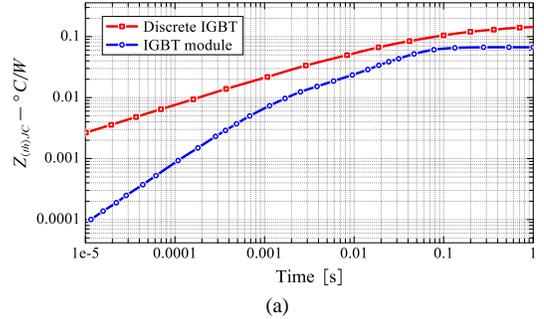


Fig. 6 (a) Thermal resistance from junction to case for discrete IGBT and IGBT module, (b) relationship between T_j and duration of 1 kA pulse current.

$$I_{density} = 1000 / (A_{device} * N_{parallel}) \quad (1)$$

$$N_{parallel} = 1000 / I_{cm}$$

where A_{device} is the package volume, N_{parallel} is the parallel number and I_{cm} is the peak current from the datasheet [27-29]. It can be seen that the discrete package has the highest current density. The discrete device also offers more integration flexibility and has good current sharing for parallel devices.

Apart from the peak current density, the current conduction ability is also compared between discrete IGBT and IGBT module. During the short pulse, the heat produced by die will not reach the case, so the case temperature T_c could be considered same as the ambient temperature. In this way, the variance of T_j under 1kA peak current could be calculated through (2) and depicted in Fig. 6(b).

$$T_j = I_c \cdot v_{\text{on}} \cdot Z_{(\text{th})JC} + T_c \quad (2)$$

where I_c is the peak current through each device (assuming current sharing is good if parallel connection is adopted), v_{on}

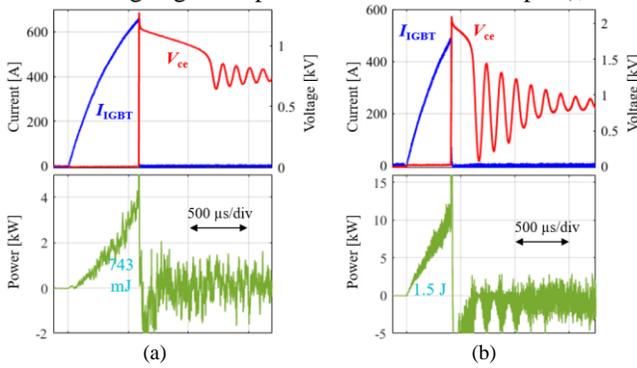


Fig. 7 Surge current test of (a) 1.7 kV IGBT, and (b) 3.3 kV IGBT.

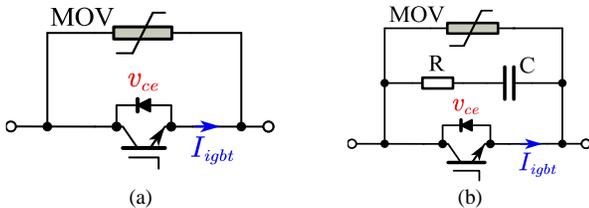


Fig. 8 Two types of voltage clamping circuits, (a) only MOV, (b) MOV paralleled with RC snubber.

represents the on-state voltage, and $Z_{(\text{th})JC}$ denotes the device transient thermal impedance from junction to case as shown in Fig. 6(a) [27-29]. The junction temperature limitation is set as 125 °C to allow margin for the turn-off energy. According to Fig. 6(b), IGBT module has higher thermal capacitance to sustain peak currents for longer pulse durations (> 1 ms) while discrete IGBTs can handle peak currents without thermal concerns for pulses < 1 ms. Since the specially designed ultrafast VDS can open within 500 μs, the discrete package is a better option than the module from the point of current density. Then the discrete device candidate from IXYS should be determined in terms of the voltage rating (1.7 kV, 3.3 kV), technology (non-punch through, Bimosfet), and package (TO247, i5-PAC).

The surge current test was first conducted for verification with the 1.7 kV (IXGK100N170) and 3.3 kV IGBT (IXBF55N300) as shown in Fig. 7. In this test, the device under test (DUT) is turned on to create a surge current and

TCCI is neglected for simplification. It can be seen that both devices are able to conduct at least 500 A current within 500 μs, which means two parallel discrete IGBTs can achieve the target of 1 kA. This result matches the previous calculation in Fig. 6. However, it should be noted that a surge current conduction ability does not necessarily imply the same capability to cut this current. Especially for the high voltage device, the voltage clamping circuit is involved in the turn-off process and can influence the interruption performance.

Voltage clamping circuit can help suppress the overvoltage across the device and absorb the energy stored in line inductor. Various voltage clamping components have been discussed in [6] and [30], including the metal oxide varistor (MOV), transient voltage suppression (TVS) diode, resistor-capacitor (RC) snubber, etc. The design of voltage clamping circuit is typically driven by the peak clamping voltage, the leakage

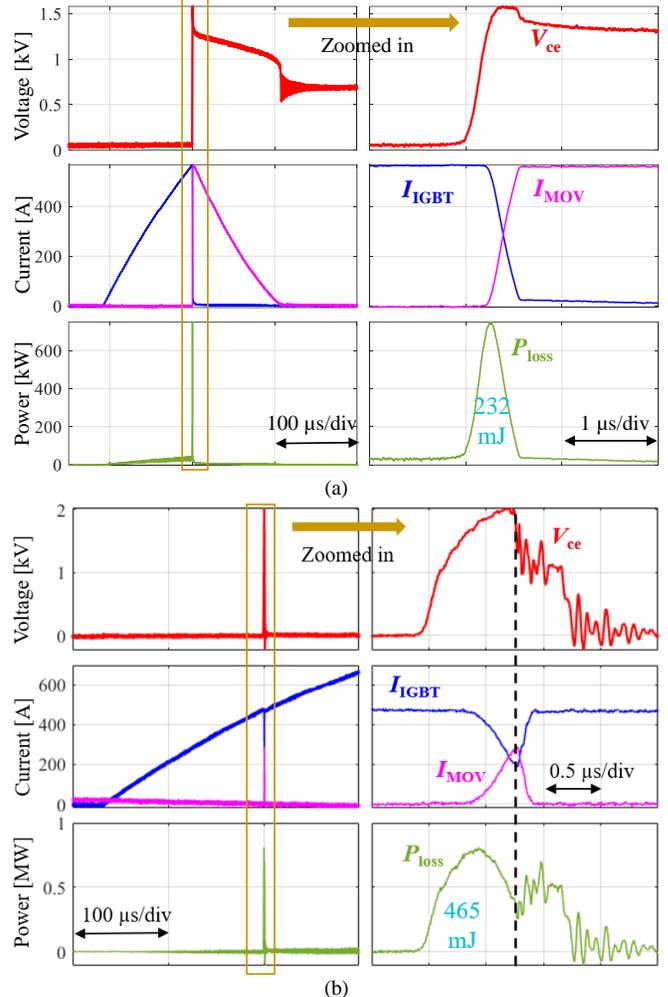


Fig. 9 Surge current turn-off waveforms for only MOV voltage clamping circuit, (a) 1.7 kV IGBT turn-off at 600 A (232 mJ energy), (b) 3.3 kV IGBT failure turn-off at 432 A (477 mJ energy).

current at nominal voltage and the total absorption energy. Since a TVS diode has lower energy capacity than a MOV, it is not considered here. In this design, it was found that the tail-current bump of IGBT also influences the clamping circuit selection. This phenomenon manifests when the MOV plus RC snubber is used, and may become a fatal issue, resulting in

destroyed devices. Overall, two main options as shown in Fig. 8 are investigated and compared.

A MOV is a nonlinear resistor with a dependency on applied voltage [31]. When low voltage is applied, it has very high resistance. Whereas it has the lowest resistance with the clamping voltage applied, so that the fault current will flow through it. Besides, there is a steep front effect to affect the peak voltage, which is proportional to di/dt [32].

In the single MOV configuration, the IGBT operates in a hard-switching condition where it is exposed to simultaneous high current and high voltage and huge switching loss. The gate resistor of IGBT offers a degree of freedom for losses trade-off. A smaller gate resistor will cause smaller switching loss, but causes a higher peak voltage across the MOV due to higher di/dt . Fig. 9 shows the test results of 1.7 kV and 3.3 kV IGBTs, the former one survives the turn-off current of 600 A, but the later fails with a

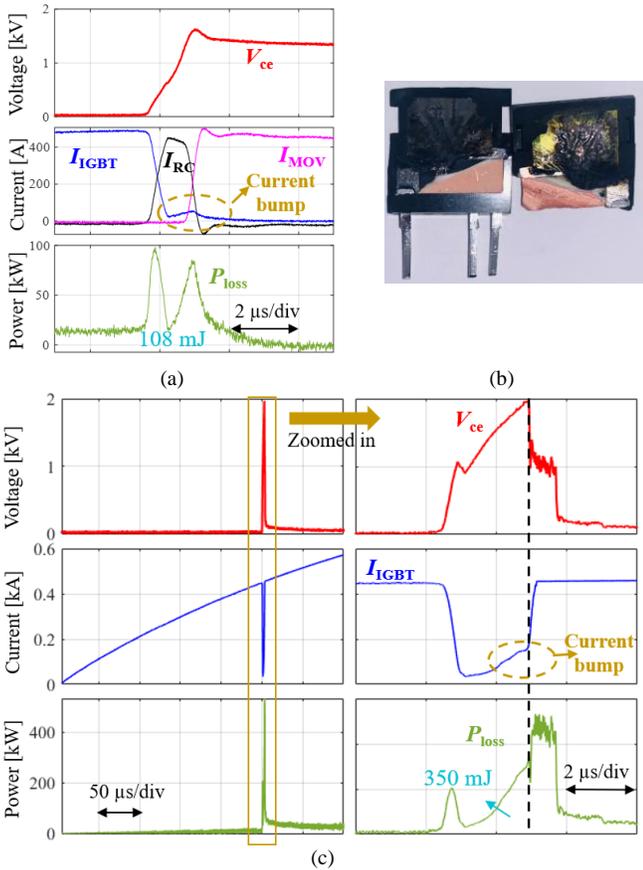


Fig. 10 Surge current turn-off waveforms for MOV plus RC snubber voltage clamping circuit, (a) 1.7 kV IGBT successful turn-off of 330A (108 mJ energy), (b) picture of damaged 3.3 kV IGBT, (c) 3.3 kV IGBT failure turn-off at 450 A (870 mJ energy).

turn-off current of 432 A. In this case, loss reaches 465 mJ which proves to be too high for the device to handle as it resulted in device failure. Considering the risk of device damage or degradation at turn-off from high peak current, this snubberless type voltage clamping circuit is not used here.

Another type of voltage clamping circuit is RC snubber paralleled with MOV, and the IGBT works in soft switching mode. The RC snubber could help lower the turn-off power

loss and limit MOV voltage overshoot [26]. However, there is a unique phenomenon of current bump when the current transfers from the IGBT to the snubber branch as shown in Fig. 10(a). This phenomenon has been reported in many papers about the soft-switching IGBT, which operates at nominal current [33]. Compared to the snubberless case, the turn-off energy becomes smaller, and the current bump only introduces some additional loss but does not damage device.

However, the 3.3 kV IGBT was damaged when cutting current of 450 A with the clamping voltage of 2 kV as shown in Fig. 10(b) and Fig. 10(c). It can be seen that at the peak of current bump, the IGBT fails short so that the voltage drops to zero. Since this test has much higher peak current than the normal operation, the current bump magnitude is higher and the bump energy (350 mJ) could not be neglected. Higher ‘‘bump’’ magnitudes in the presence of high dv/dt may lead to dynamic avalanche, which can create the filamentary currents.

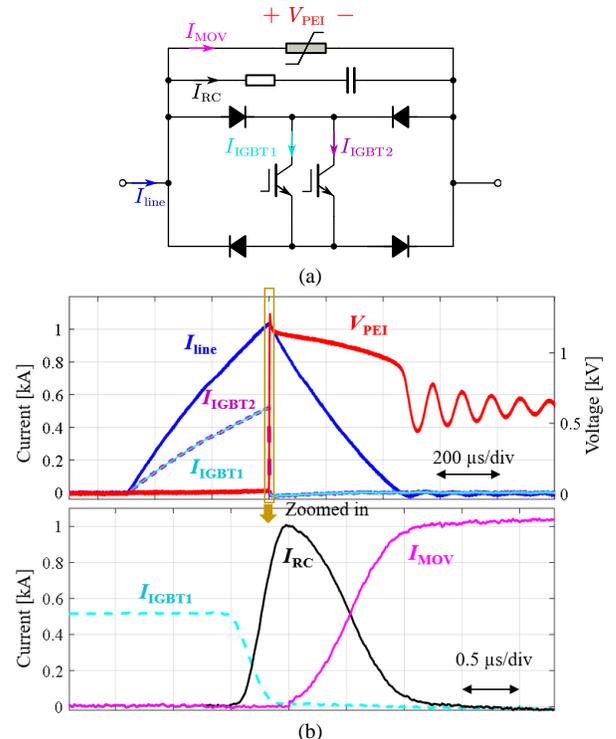


Fig. 11 (a) Configuration of single bidirectional module, (b) experimental waveforms of single module to conduct and interrupt 1 kA pulse current.

TABLE I Parameters of Single Module

Description	Part number	Value	Quantity
IGBT	IXGK100 N170	1.7 kV / 170 A	2
Diode	VS-90EPS16L-M3	1.6 kV / 90 A	4
Snubber R	W22-1R0JI	1 Ω / 7 W	1
Snubber C	C4540H683KG GWC T050	0.68 μ F / 2 kV	8
MOV	V25S510P	1.3 kV (200 A)	1

Such filamentation gives rise to a large increase of local temperature, causing the device failure. The detailed physical mechanism is still being investigated and simulated with TCAD. According to [34], the bump magnitude can be suppressed to acceptable levels by reducing the peak current

and clamping voltage or increasing snubber capacitor. Many discrete IGBTs with different voltage classes, packages and techniques, have been tested and summarized. For the 2.5 kV or 3.3 kV IGBT, a relatively large capacitor should be added to suppress the current bump and the lowered clamping voltage wastes the utilization ratio of the device. Therefore, 1.7 kV non-punch-through IGBT IXGK100N170 is selected in this work.

According to the tuning result, 0.54 μF C0G capacitor and 1 Ω resistor paralleled with MOV V25S510P are selected as the voltage clamping circuit. The snubber capacitor should be C0G material while resistor should be wire-wound type to guarantee enough surge current capability. The topology of single module is shown in Fig. 11(a) and the parameters are listed in Table I. In each module, two IGBTs are parallel connected to achieve a higher current capability, and four diodes form a bridge structure for bidirectional function. The RC snubber and MOV

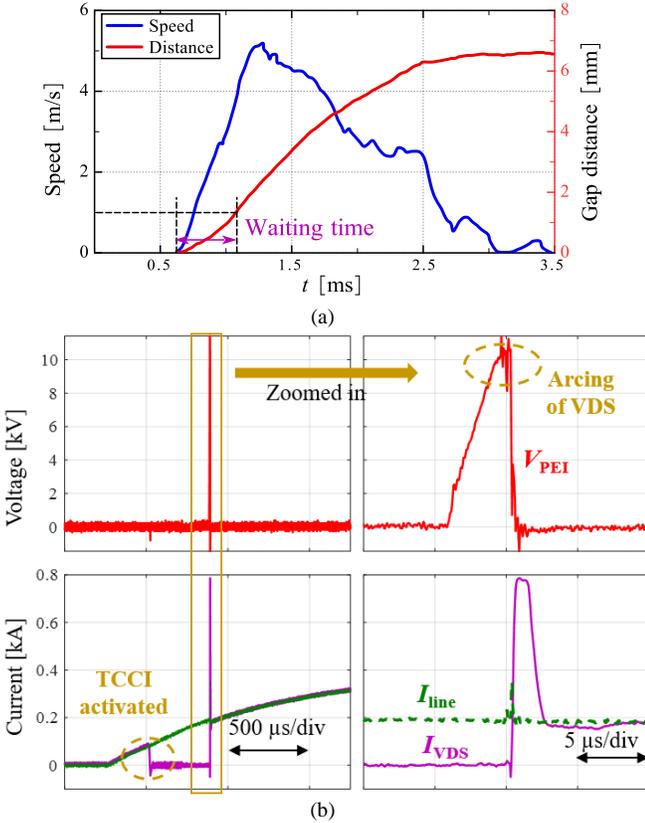


Fig. 12 (a) Waveform of the gap distance and contactor opening speed of mechanical contacts, (b) waveforms of HCB failure with VDS arcing due to the higher clamping voltage than the dielectric strength.

are placed outside the diode bridge to avoid the oscillations related with the reverse recovery of the diode [35]. The test waveforms of such a module is provided in Fig. 11 (b), which can verify the capability to conduct and interrupt 1 kA pulse current. Besides, no obvious current bump is observed in the tail current stage. Since the clamping voltage is set as 1.34 kV in each module, there should be 9 modules in total to generate the 12 kV clamping voltage for the whole PEI.

III. SYSTEM OPTIMIZATION OF MODULAR PEI

A. Turn-off Strategy and Improvement

The interruption time of HCB is predominantly limited by the opening speed of the mechanical contacts, which is greatly slower than that of SSCB. A typical waveform of gap distance and contactor opening speed of VDS is depicted in Fig. 12 (a). It can be observed that the 1 mm gap distance, which corresponds a dielectric strength of 10 kV, is reached after around 400 μs for the PEI turn-off. Only after enough dielectric strength has been established across contacts of VDS, will PEI be allowed to be turned-off as shown in Fig. 2(b). Otherwise, arcing will occur across VDS, allowing the current back to the VDS branch and causing the failure of HCB as shown in Fig. 12(b). It should be noted that the overshoot of I_{VDS} is caused by the discharging of snubber capacitor in PEI. A long waiting time for PEI means the peak current could be very high and the total HCB interrupting time is accordingly long.

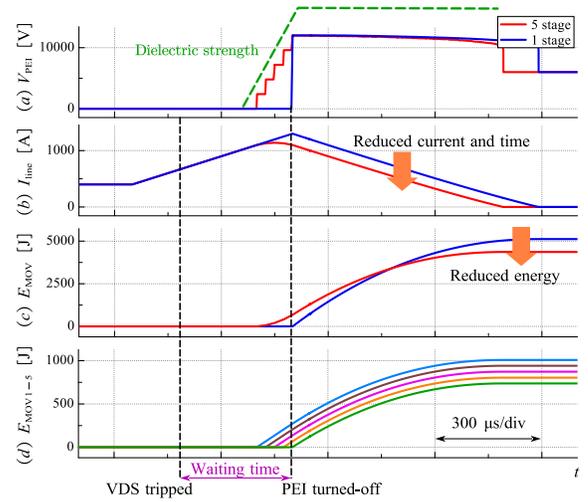


Fig. 13 Comparison between single stage and five stage turn-off schemes.

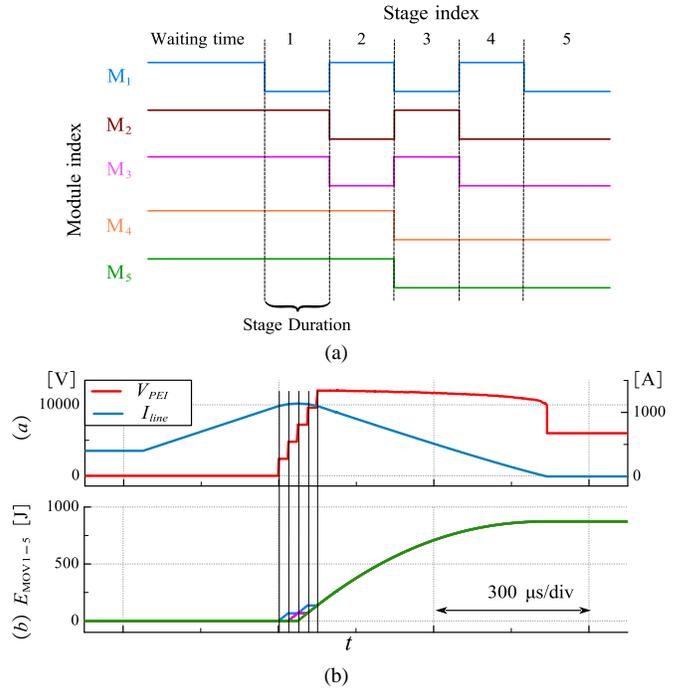


Fig. 14 (a) Illustration of proposed per-cycle balancing staged turn-off scheme, (b) waveforms of PEI with proposed turn-off scheme.

In order to reduce the waiting time for PEI, a staged turn-off strategy was introduced in [36] to make full use of the gap distance curve. Since PEI consists of series of identical modules, they can be turned off sequentially to create a staged clamping voltage waveform as shown in Fig. 13. The coordination of PEI turn-off sequence and opening of VDS contacts is very important to make sure that the arcing will not occur. It can be seen that the peak fault current, total absorption energy and clearing time will be reduced after applying this staged turn-off strategy. However, it should also be noted that the MOV in the first module to turn-off will absorb the maximum energy, while the last one will absorb the least energy. This unbalanced energy distribution will result in asymmetric degradation of the MOVs and in a way mitigate the benefit of staged turn-off scheme.

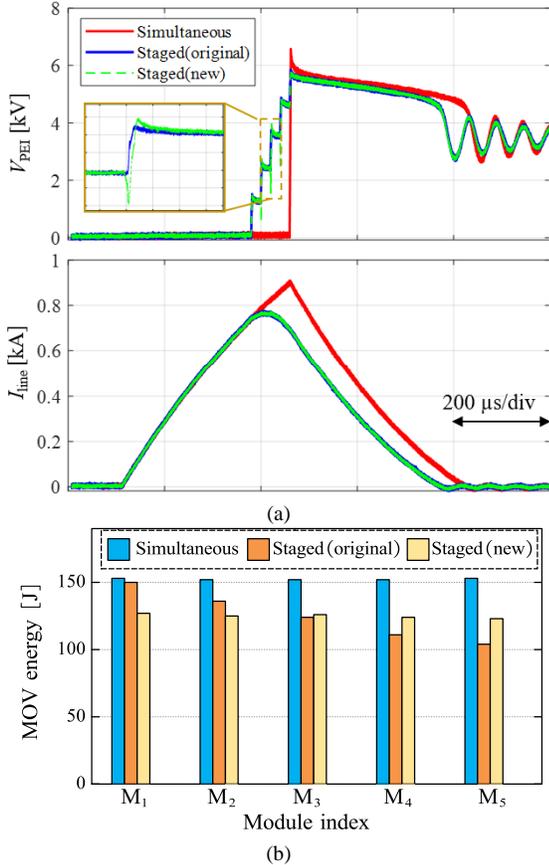


Fig. 15 (a) Waveforms of PEI voltage and line current with three turn-off strategies, (b) comparison of MOV energy with three turn-off strategies.

In this paper, two methods are proposed to improve the traditional staged turn-off strategy. In the first method, the turn-off order is rotated among different modules over the lifetime of the HCB. For example, the first module to turn-off in the n^{th} fault event will be the last one to turn-off in $(n+1)^{th}$ fault event. In this way, over a long period, the average energy absorption of MOV in each module will balance out.

The second method tries to balance the MOV energy during each event, which is called the per-cycle balancing scheme. The key point is allocating the module insertion time to

coordinate the MOV absorption energy. Assuming the fault current keeps constant during the whole turn-off process, if the total insertion time of each module is close, their MOV energy will be balanced as a result. Besides, the number of total inserted modules should be maintained the same as the original staged turn-off scheme. An example of the per-cycle balancing scheme turn-off sequence with five modules is shown in Fig. 14 (a). By turning-on or off different modules, the total insertion time of each module becomes the same. It is to be noted that this concept could be applied to any number of modules. The corresponding waveforms in Fig. 14 (b) are also given to show the effectiveness of MOV energy balancing.

The simultaneous, original staged and per-cycle staged turn-off schemes are verified with 5 modules, and the experimental results are given in Fig. 15(a). A stage duration of 20 μ s is designed to follow the increase of dielectric strength. It can be

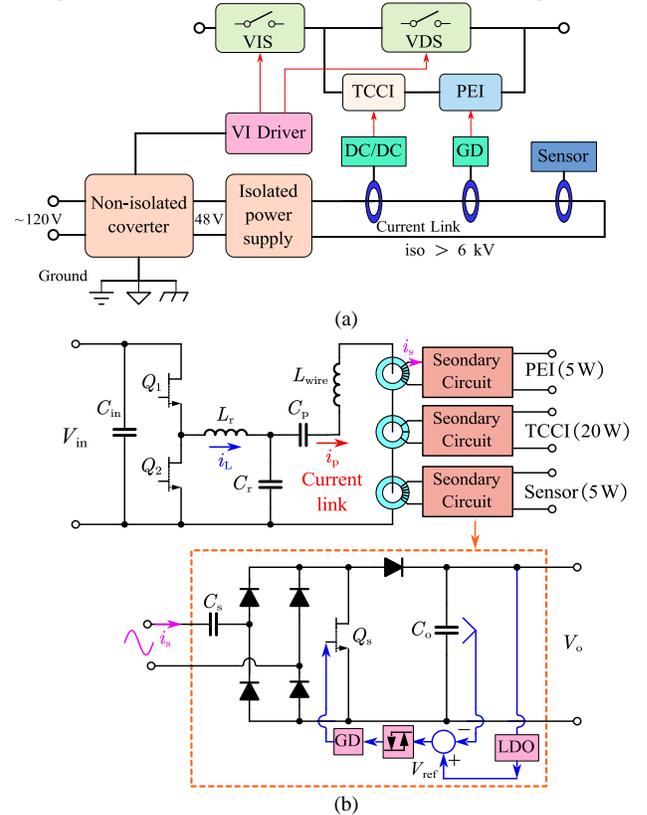


Fig. 16 (a) Power supply architecture for the whole system, (b) LCCL-LC resonant converter for PEI, TCCI and sensor based on current link.

seen that the two staged strategies produce almost identical voltage and current waveforms, which shows a smaller peak current and clearing time compared to the simultaneous strategy. A small voltage dip occurs at the stage transient with the new per-cycle staged method, due to the delay of gate command for different modules. Furthermore, the MOV energy of 5 modules are calculated and summarized in Fig. 15(b), which matches previous analysis. Simultaneous turn-off scheme has the highest energy, while the traditional staged turn-off scheme has the unbalanced energy distribution. The proposed per-cycle balancing method can not only reduce the total energy, but also balance the MOV energy.

B. Power Supply Architecture

In the whole system, the auxiliary power supply comes from the 120 V ac grid. The drive circuit for the Thomson coil of VDS and VIS does not need isolation, because the insulation layer is inserted between the coil and the VI [20], [37]. However, an isolated power supply with enough insulation capability is necessary to drive the TCCI, PEI and some sensors as shown in Fig. 16 (a). Considering the different location and power rating of multiple loads, an LCCL-LC resonant converter based on a current link is adopted in this paper [38].

As presented in Fig. 16(b), the primary circuit is able to provide a constant sinusoidal current i_p . While the secondary side uses a diode bridge and a boost converter to regulate the output voltage. By changing the turn number of secondary winding, the output power rating is changed accordingly. The

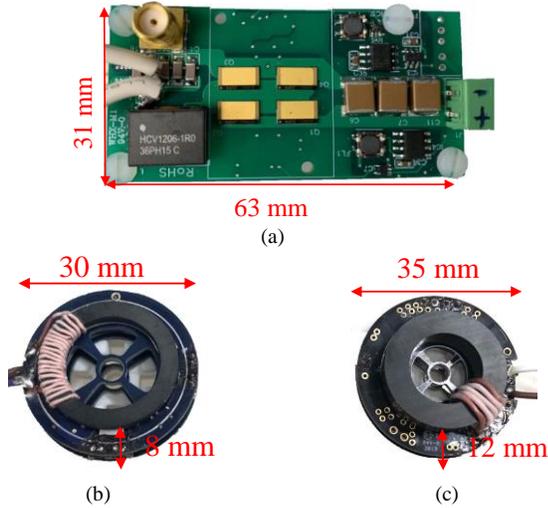


Fig. 17 Prototype picture of (a) primary circuit, (b) 5 W secondary circuit and (c) 20 W secondary circuit.

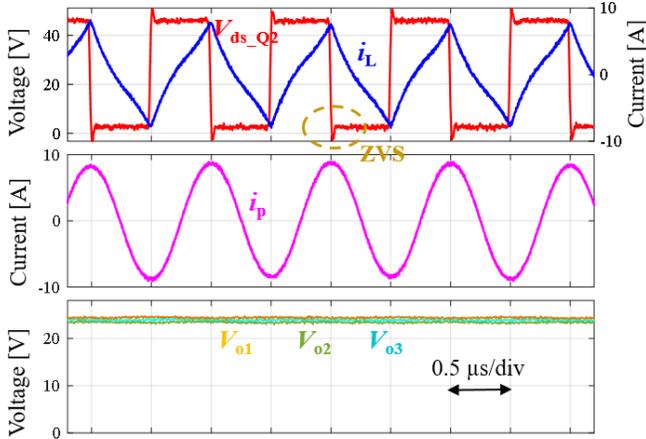


Fig. 18 Waveforms of critical variables in LCCL-LC resonant converter.

multi-load driving ability could be achieved because all receiving circuits are connected in series from one sending circuit. Besides, the single primary turn transformer could reduce the coupling capacitor significantly. The detailed working principle and circuit parameter design are described in [38], [39] and will not be discussed here.

In order to shrink the overall converter size, especially the magnetic component size, the switching frequency is designed as 1 MHz. Gallium Nitride (GaN) devices are selected as the power switch due to their small size and low loss at high frequency. Fig. 17 shows the hardware of the primary board, 5 W and 2 W secondary boards, which are quite small and compact for the higher power density. The single-turn primary wire passes through an aperture in three secondary boards and then returns back to the primary board. And the corresponding experimental waveforms at full load are presented in Fig. 18. It can be seen that the ZVS turn-on of Q_2 is achieved at the frequency of 1 MHz and the output voltage ripple is pretty low. In order to evaluate the thermal performance of this power supply, one hour continuous test was conducted and the thermal camera results are presented in Fig. 19. It can be seen that the design can handle the thermal stress without any issue.

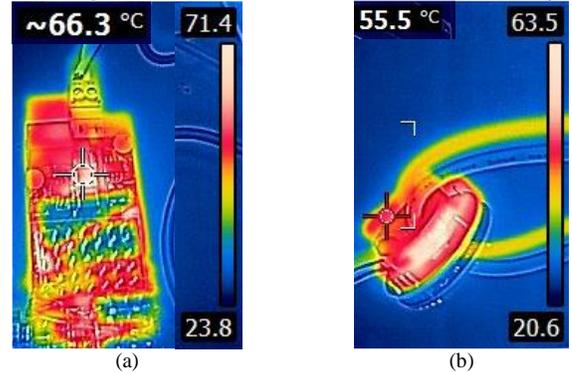


Fig. 19 Thermal test results of (a) primary board and (b) 20 W secondary circuit.

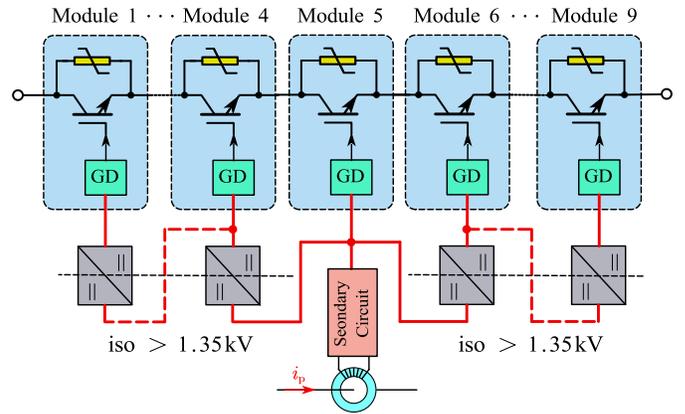


Fig. 20 Cascaded gate driver power supply inside PEI.

Partial discharge (PD) free design is also desired for the power supply system to guarantee the long-term operation with a steady-state voltage of 6 kV. Therefore a silicone encapsulant is selected to pot the whole secondary circuit as well as a part of primary wire. The high voltage PD test result demonstrate that the partial discharge inception voltage (PDIV) of the potted version could reach 16.4 kV, with a breakdown voltage above 20 kV [36]. Considering the high resonant frequency of the current source (1 MHz), the EMI radiation noises caused by the HV cable will influence the operation of other sensitive parts, such as the TCCI and the central controller. Therefore, a coaxial cable with grounded

shield layer is selected for the primary wire and the RF terminal is adopted for the interconnection. An adapter board with two RF terminals is designed to interface the potted secondary board. Since the shield layer could be regarded as the return path, the single cable connection makes the assembly of power supply much easier.

On another aspect, the gate driver power supply for IGBT in each module should be isolated with each other, too. The extreme case is gate driver voltage potential difference between the first module and last module will be 6 kV and the transient voltage will reach the total clamping voltage of 12 kV. Applying individual 5 W secondary circuits for each module is feasible but will occupy a large space. And as mentioned earlier, the voltage potential difference between two nearby modules will not exceed the clamping voltage of selected MOV. Therefore, a cascade power supply architecture

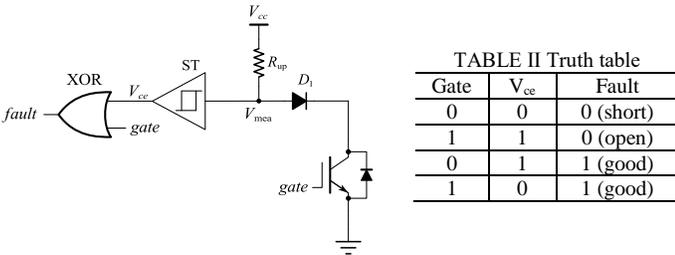


Fig. 21 Schematic of fault detection circuit in each module.

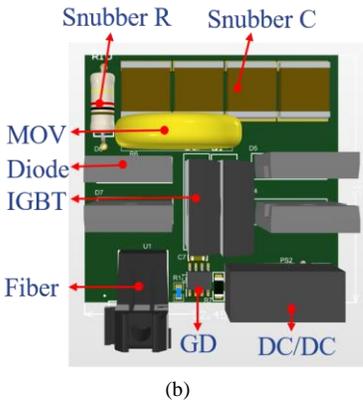
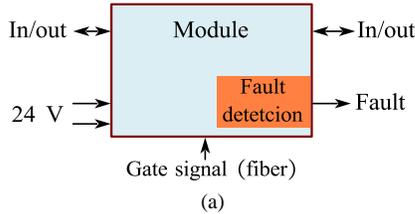


Fig. 22 (a) Interface of single module, (b) PCB layout of single module.

is adopted inside PEI to reduce the isolation voltage requirement for the small dc/dc power supply. As shown in Fig. 20, the output of 5 W secondary circuit is connected to the middle module and then the power is delivered to series modules one by one. In this way, the commercial compact dc/dc power supply is sufficient to meet this isolation voltage requirement of 1.35 kV.

C. Fault Detection and Integration

Another important function of the PEI is the fault indication, which focuses on the open- or short- circuit detection of the IGBT in each module. A simple test circuit is integrated to each module as shown in Fig. 21. R_{up} is a pull-up resistor and can limit the current once the device fails short. While D_1 is a high-voltage diode to block the clamping voltage from the detection circuit during the fault event. A non-inverting Schmitt trigger can transfer the measured device voltage to the binary output V_{ce} , and the XOR logic with gate signal could generate the fault signal according to Table II. The AND logic of total nine modules fault signal will give the final fault signal.

Therefore, the interface of each module is defined as shown in Fig. 22(a). The three-dimension (3D) illustration is given in Fig. 22(b), and the fault detection circuit is placed on the bottom layer. The integration of PEI needs to connect nine

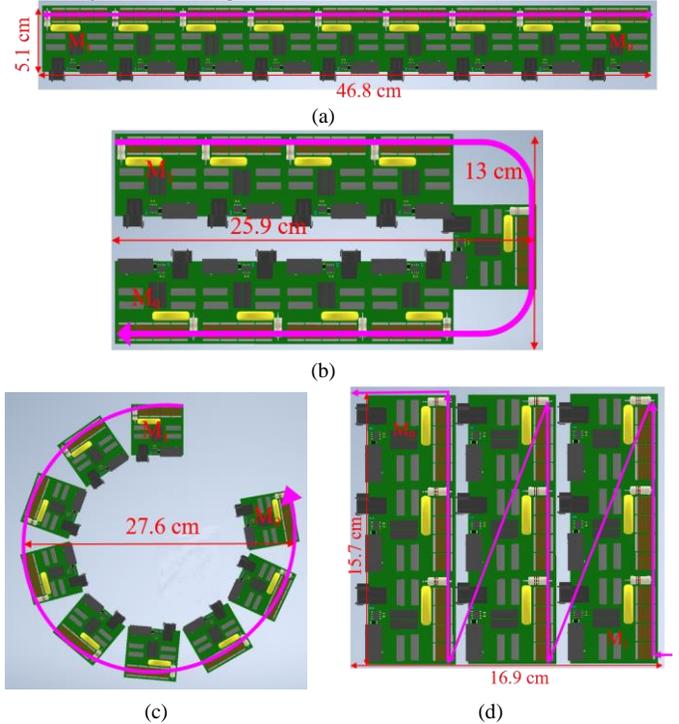
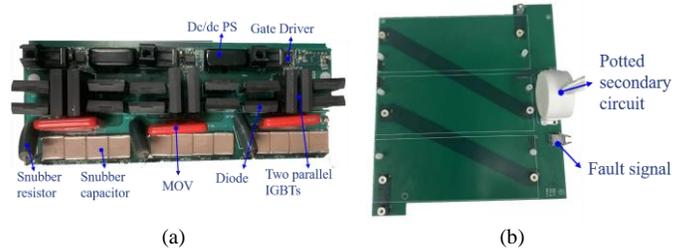


Fig. 23 Four kinds of layouts, (a) straight, (b) U-shape, (c) circular, (d) zigzag shape.



(a) (b)

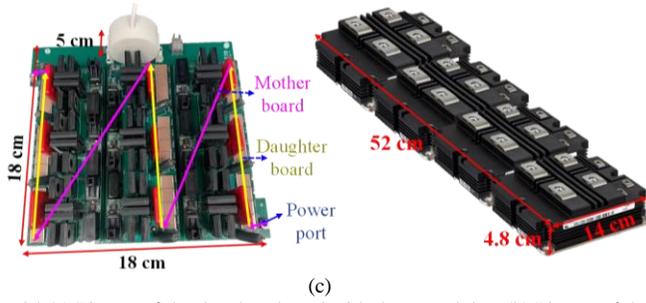
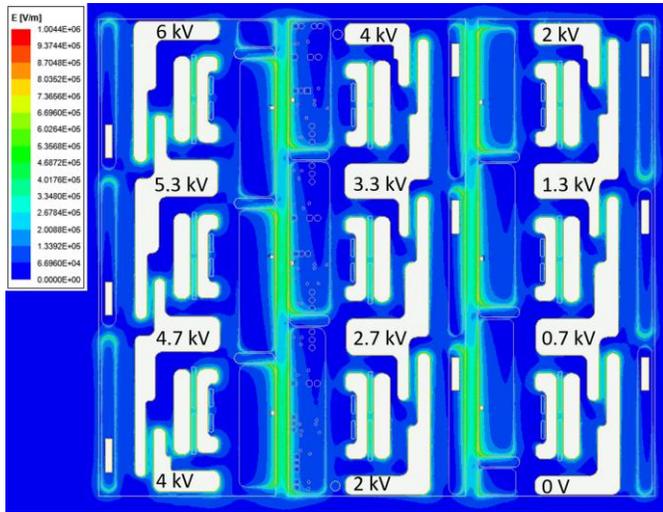
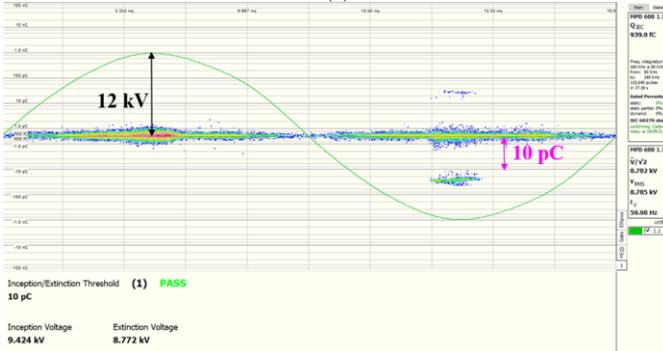


Fig. 24 (a) Picture of the daughter board with three modules, (b) Picture of the mother board, (c) picture of whole PEI and comparison with a 12 kV bidirectional switch based on 6.5 kV IGBT module.

modules in series to reach 12 kV, and there are a lot of possible ways to arrange their positions. According to the shape of main-power path, four typical layouts of nine modules are listed in Fig. 23, including the straight line, U-shape, circular shape, and zigzag shape. Obviously, the straight line has the smallest volume and highest power density, but is relatively hard to match the dimension of TCCI and assemble with VDS. Therefore, the zigzag structure is adopted here due to higher power density compared to U-shape and circular shape.



(b)



(c)

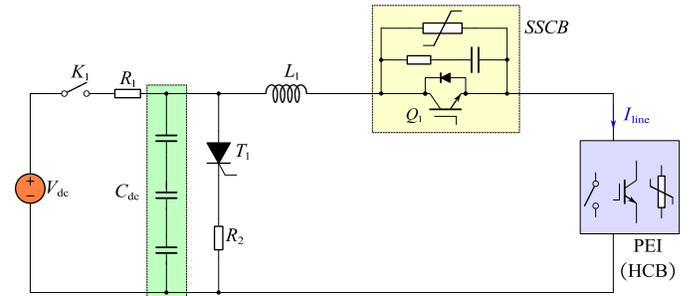
Fig. 25. (a) Zigzag main power path of second version PEI, (b) E-field simulation results for three parallel placed daughter boards, (c) experimental PD test results.

As shown in Fig. 24(c), a mother-daughter board configuration is employed to implement the zig-zag main power path. Each daughter board in Fig. 24(a) contains three modules, and the total fault signal is passed to the first module through the digital isolator. While the mother board shown in Fig. 24(b) integrates the interface for the auxiliary power supply and final fault signal. It can be calculated that the proposed design reaches a peak power density of 7.4 kW/cm^3 . Compared to the 12 kV bidirectional switch based on four 6.5 kV IGBT modules ($52 \times 14 \times 4.8 \text{ cm}^3$), our proposed design achieves around 2.5 times better power density. And it should be noted that extra MOV and gate driver units should be added to build a PEI besides the IGBT modules.

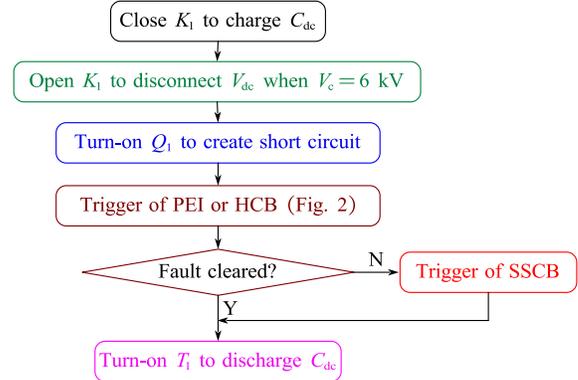
The E-field control is also very important for the insulation and PD free operation, and the upper limitation of E-field in the air is set as 2 kV/mm here. Assuming the equal voltage distribution of 9 modules, the E-field simulation result through ANSYS is presented in Fig. 25(a) with the daughter board distance of 4.5 mm, and the PD test result is given in Fig. 25 (b). It can be seen that the maximum E-field in the air gap between two daughter boards is 1 kV/mm, only half of the limitation. In addition, the PD experimental results also indicate the PDIV is 9.4 kV, higher than the DC bus voltage 6 kV.

TABLE III Parameters of test setup.

Symbol	Description	Value
V_{dc}	Dc source voltage	6 kV
C_{dc}	Dc capacitance	2.25 mF
L_1	Air core line inductance	0.5 ~ 2.5 mH
R_1	Charging resistor	500 Ω
R_2	Discharging resistor	1 k Ω



(a)



(b)

Fig. 26. (a) 6 kV 1 kA test platform circuit for PEI and HCB, (b) operation sequence and test process.

VI. EXPERIMENTAL TEST RESULTS

A. Full Voltage Test for PEI and Power Supply

A 6 kV 1 kA short circuit experimental platform as shown in Fig. 26(a) is established to test PEI and then HCB the parameters are listed in Table III. This platform consists of a high voltage dc source, a charging relay K_1 , charging resistor R_1 , dc capacitor bank C_{dc} , discharging thyristor T_1 , discharging resistor R_2 , air core inductor L_1 and a high capacity protection SSCB. The PEI and HCB under test is inserted on the return path.

The operation process of the experimental platform is shown in Fig. 26(b). The PEI or HCB is initially closed, and the capacitor bank C_{dc} is charged after closing K_1 . After its voltage reaches 6 kV, K_1 is opened to disconnect the capacitor from the source. Then Q_1 in the SSCB is turned-on to create a short-circuit fault manually; the line current then rises with a di/dt controlled by changing the value of L_1 . When testing PEI, the turn-off command is delayed by certain time from the on command of Q_1 . When testing HCB, the operation follows the time diagram in Fig. 2(b). If the PEI or HCB fails to clear the fault current, the protection SSCB could help to interrupt it and avoid catastrophic damage of the test platform.

In the first test, the PEI, one primary secondary circuit and three secondary circuits are connected as in Fig. 27 to verify

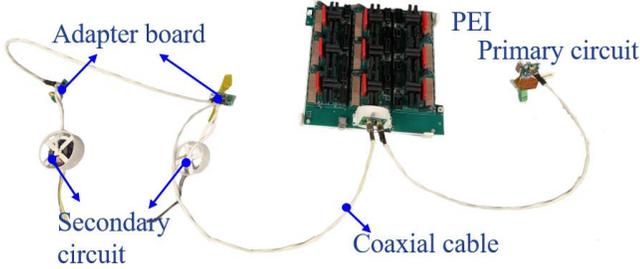


Fig. 27. Picture of PEI and connected power supply under test.

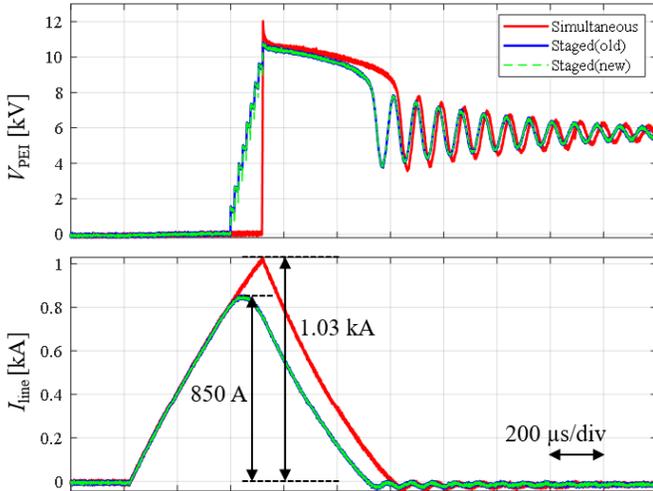


Fig. 28. Waveforms of full voltage PEI with three turn-off strategies.

the functionality of PEI and designed power supply. Following the operation in Fig. 26 (b), three kinds of turn-off strategies are implemented and at 12 kV and 1 kA are plotted as shown in Fig. 28. It can be seen the fault current of 1 kA and the

clamping voltage of 12 kV is realized successfully with the simultaneous turn-off strategy. After using the staged turn-off scheme with a duration of 15 μ s, the peak current is reduced to 850 A, and the total energy is reduced from 2.24 kJ to 1.89 kJ. Several continuous pulse test was conducted and PEI shows the same performance without any issue. During the whole process, the power supply also works well, which indicates the robustness and stability of designed power supply.

B. Full Voltage Test for HCB

After all of the components have been verified by experiments to achieve the expected performance, the VDS, VIS, TCCI and the PEI are packaged together as shown in Fig. 29 to test the function of the entire HCB. The TCCI and PEI are fixed in a fiber glass box to avoid the breakdown between them and VI. The controller of DSP is responsible for the generation the command signal for all the components based on the results from the LEM current sensor.

In this test, the fault happens at t_0 is detected at t_1 , and TCCI is activated at t_2 to reduce the VDS current to 0. After a waiting time of around 200 μ s, the PEI is turned off at t_3 , the clamping voltage of 12 kV clears the line current successfully at t_4 .

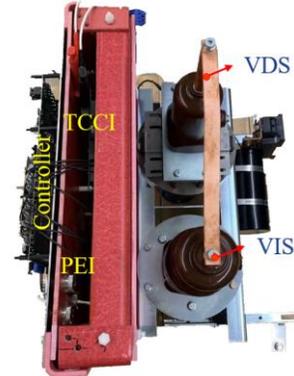


Fig. 29. Picture of a 6 kV HCB equipment.

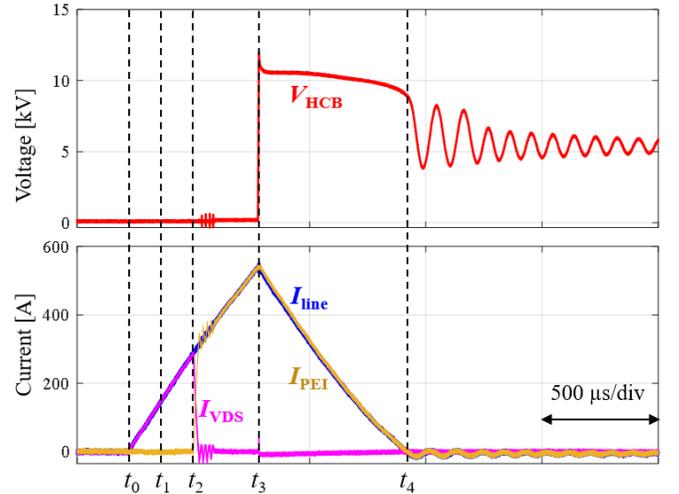


Fig. 30. Waveforms of 6kV HCB operation.

V. CONCLUSIONS

As an important part of HCB, PEI plays an important role of conduction and interruption of surge current. Although it is based on the series semiconductor devices, the design focus is quite different from that of the normal power converters. In this paper, the design procedure based on a 12 kV 1 kA modular PEI concept is introduced. The trade-off of single module shows the device and voltage clamping selection, and the integration of nine modules demonstrates a very high power density of 7.4 kW/cm³. In addition, the proposed staged turn-off strategy can improve the MOV energy balance and thus average their life time. The experimental results validates the current interruption function of deigned PEI and HCB at 6 kV dc bus. With the good scalability and small volume, this PEI concept and the HCB architecture shows great potential in the MV dc system, such as shipboard and aircraft applications.

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