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Gate-damage safe failure-mode deep analysis under short-circuit operation of 1.2kV and 1.7kV power SiC MOSFET using dedicated gate-source / drain-source voltage depolarization and damage-mode optical imaging

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Abstract—Robustness of 1.2kV and 1.7kV Silicon Carbide MOSFETs submitted to short-circuit operations mode is studied. Experimental results confirm two main failure modes: a safe fail-to-open mode and an unsafe fail-to-short mode. A technique based on direct depolarization of gate source voltage is used to increase the short-circuit withstand capability and to partially obtain a fail-to-open mode. Electro-thermo-metallurgical simulations are investigated to deeply explain the fail-to-open mechanisms. Finally, using lock-in-thermography and scanning-electronic-microscopy imaging, a new and spectacular lift-off effect of gate-finger is highlighted to clearly confirm the fail-to-open mode capability such devices.

Keywords—short-circuit, SiC MOSFET, failure-mode.

I. INTRODUCTION

SiC MOSFETs have emerged in large market applications (e.g., railway traction, automotive, energy distribution network, electric vehicles and the “more electric” aircraft) [1], because of their advantages of lower switching losses, higher power density and higher temperature capability. However, the reliability of these devices under single and repetitive harsh operating conditions remains a major concern, especially the lowest ruggedness against short-circuit (SC) [2, 3]. The SC characterization is essential to determine failure-mode types and short-circuit duration capability and to highlight technology improvement requirements. Indeed, the ability of device to withstand SC events at least $10\mu\text{s}$ (T_{scw}) as standard IGBT device could simplify protection circuitry, reduce overall system cost. Various scientific literatures reported that SiC MOSFETs may present, under short circuit operation, different failure modes such as drain-source Fail-To-Short (FTS) and Fail-To-Open (FTO) by means of an interesting and original gate-source short or low ohmic path obtained in low-power density stress conditions [4-6]. However, these references only report results on standard 1.2kV rating while other ratings are introduced today. Indeed, medium voltage SiC MOSFETs (650 V–1700 V) ratings are now commercially available from several major manufacturers for standard motor-drive, automotive on-board charger and photovoltaic inverter. To

address the lack of results on 1.7kV rating, we examine in this paper the SC capability of such components to exhibit the same FTO mode and gate-damage properties that well-known 1.2kV rating devices. To achieve this objective, a large V_{GS} depolarization method is explored combined with a small V_{DS} depolarization to reduce the chip power-density stress applied on 1.2kV and 1.7kV devices. Gate “depolarization” means reduction of the gate voltage bias on the SC sequence. The gate voltage bias is thus reduced from 18V (or 20V nominal rating bias) to a value between 10V and 12V bias. Ruggedness capability and dedicated failure-modes are then presented in depth based on 1D transient thermal simulation and detailed cuts optical imaging. Finally, using Lock-In-Thermography (LIT), Focus-Ion-Beam (FIB) and Scanning-Electronic-Microscopy (SEM) 2D-3D imaging a new and spectacular lift-off effect of a gate-finger is highlighted probably yielded by combination of the strength cracking (from top to bottom direction of the chip) and an Al melting moving (from bottom to top direction of the chip) at the edge and below the gate-damage region. The article is organized as follows: the experimental setup is presented in part II, then results on V_{GS} depolarization, discussion and comparisons are exposed in part III including thermal transient simulations to support analysis, $R_{\text{DS(on)}}$ penalty is depicted in part IV, finally FIB-SEM analysis are presented in part V on 1.2kV and 1.7kV chips.

II. EXPERIMENTAL SET-UP

Short-circuit tests are carried out on two types of 3-pin TO247 1.2kV SiC MOSFETs (respectively A-, B-MOSFET) manufactured by Cree (a small size die 10mm^2 ref. A - C2M0080120D and a large size die 26mm^2 ref. B - C2M0025120D) and a third type of 3-pin TO247 MOSFET (C MOSFET) rated at 1700V from the same manufacturer (large size die 30mm^2 ref. C - C2M0045170D). Such devices are examined under standard type 1 hard-switching fault. The experiments are achieved on the bench described in Fig. 1 [7]. This bench offers for the users the possibility to set different SC test conditions such as various V_{DS} , V_{GS} , and incremented T_{SC} values. The tests are

TABLE 1. SUMMARY OF SHORT CIRCUIT TESTS PERFORMED ON THREE TYPES OF DEVICES

Device	A-MOSFET (C2M0080120D)			B-MOSFET (C2M0025120D)			C-MOSFET (C2M0045170D)		
V_{DS} (V)	500	550	600	500	550	600	500	550	600
V_{GS} (V) depolarization	13	12	10	13	12	10	13	12	10
T_{sc} (μ s)	21	18	24	21	29	28	26	29	28
Critical energy E_c (J)	0.82	0.64	0.85	2.4	2.49	2.45	3.09	2.95	2.53
Total chip Surface (mm^2)	10.4	10.4	10.4	26	26	26	30	30	30
Critical energy density (mJ/cm^2)	7.8	6.2	8.2	9.6	9.6	9.4	10.3	9.8	8.4
Power density (W/mm^2)	3756	3418	3440	4192	3294	3363	3560	3390	3007
Failure mode	FTO	FTO	FTO	FTO	FTS	FTO	FTO	FTO	FTS

performed at room temperature ($T_{CASE} = 25^\circ C$) with a gate resistance (R_G) fixed to 47Ω which allows a slow turn-off to avoid overvoltage without the use of a Soft Shut Down (SSD) function included in the gate-driver circuit. Such a value also allows an easy on-line ohmic measurement of the dynamic gate leakage $I_{GS}(t)$ with a good accuracy. The pulse duration time of the SC test (T_{SC}) is progressively increased with a step of $1 \mu s$ until FTO and / or FTS failure mode occurs. Note that to facilitate comparisons the maximum voltage applied across all devices will be 600V. Considering that $2/3 \times$ Voltage rate is a standard voltage stress to define short-circuit capability by manufacturers, the drain-source derating applied in our test is equal to $600V / (2/3 \times 1200V) \rightarrow 75\%$ for 1.2kV devices and a derating to $600V / (2/3 \times 1700V) \rightarrow 53\%$ for 1.7kV device. Note that a great voltage derating is often considered in critical on-board applications such as aeronautics, where 1.7kV rating is expected to replace 1.2kV one, to withstand critical voltage transients or to reduce cosmic radiation failure rate. In [8, 9], a FIT reduction at least of two decades is expected on neutron radiation by using a 1.7kV SiC module instead of a 1.2kV one, at the same DC-bus voltage.

III. RESULTS AND DISCUSSION

The short-circuit test methodology is performed with a three values of bus voltage (V_{DC}) (500, 550 and 600V) and $10V < V_{GS} < 13V$ to identify the maximum power density yielding a FTO mode [10] at $T_{CASE} = 25^\circ C$.

Table 1 summarizes the results of short-circuit. Tests were performed on the three references at different V_{GS} and V_{DS} bias. For the test, at least 3 DUTs of each reference were analyzed in order to verify the low dispersion and the consistency of the behavior.

For 1.2kV devices, there are very few articles on the topic of a strong reduction of the gate voltage to obtain a SiC MOSFET very robust in short-circuit operation. Scientific literature on 1.7kV devices is poor because such a rating is still not widely available and clearly more expensive than 1.2kV device. The only relevant reference is [11] on the C2M0080120D device: under $V_{DS} = 600V$, $V_{GS} = 11V$, the authors measured a $T_{SC} = 15\mu s$ and an $E_{SC} = 0.8J$. These values are quite consistent with our measurements since under the same drain voltage but $V_{GS} = 10V$ device is more robust with $T_{SC} = 24\mu s$ and $E_{SC} = 0.85J$ due to the increase in T_{SC} .

Fig. 2 reports waveforms (V_{GS} , I_G and I_{DS}) recorded during failure under short-circuit tests for three SiC MOSFET references. It can be highlighted that:

- a delayed FTO appears on all devices between $4\mu s$ and $7\mu s$, this delay could be explained by a minimal thermal diffusion time or by the time taken by the temperature in the oxide region to cross the liquidus-solidus transition band, at the turn-off, in the cooling-down phase,

- from Table 1, it can be noticed that the two 1.2kV devices (A- and B-MOSFET) perfectly comply with initial requirement which is to maintain a secure FTO failure mode at V_{DS} voltage closer to 600V with a $T_{SC} > 10\mu s$. On the other hand, although the C-MOSFET 1.7kV devices presents a FTO at $V_{DS} = 550V$ but not at $V_{DS} = 600V$, it shows a better robustness to short-circuit operation with, in average, an increase of 23% of the T_{SC} compared to 1.2kV devices,

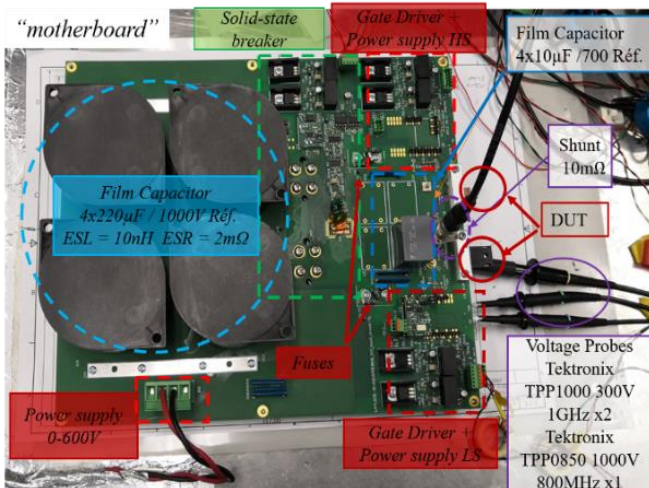


Fig. 1. Bench of type 1 short-circuit test.

- the study also points out that if the gate depolarization gets too close to the threshold voltage, which is difficult to estimate because the chip temperature reaches a very high value, the failure mode reverses from FTO to FTS. In this case, often approaching $V_{GS} = 10V$, the gate voltage must be raised to recover the FTO. It may be explained by the thermal instability that appears on SiC MOSFET chips when the gate voltage approaches the threshold voltage, the saturation current increases with temperature. In practice, the weakest MOSFET cell, i.e. with the highest local threshold voltage, should logically go into thermal runaway first,

consider that power density is a good criterion for short-circuit robustness management.

This last property also shows that the failure mode involved is based on reduced thermal rate and that sufficient delay time is required for the metallurgical and thermo-mechanical mechanisms to develop fully between the Al source electrode and the gate-polysilicon fingers [12]. Therefore the V_{GS} depolarization is applied with a quasi-constant reduced V_{DS} bias. A 1D transient electro-thermo-metallurgical simulation is performed in Fig. 3 to explain the origin of FTO mode (explanation will be more detailed in the final paper submission) on A, B and C-MOSFET.

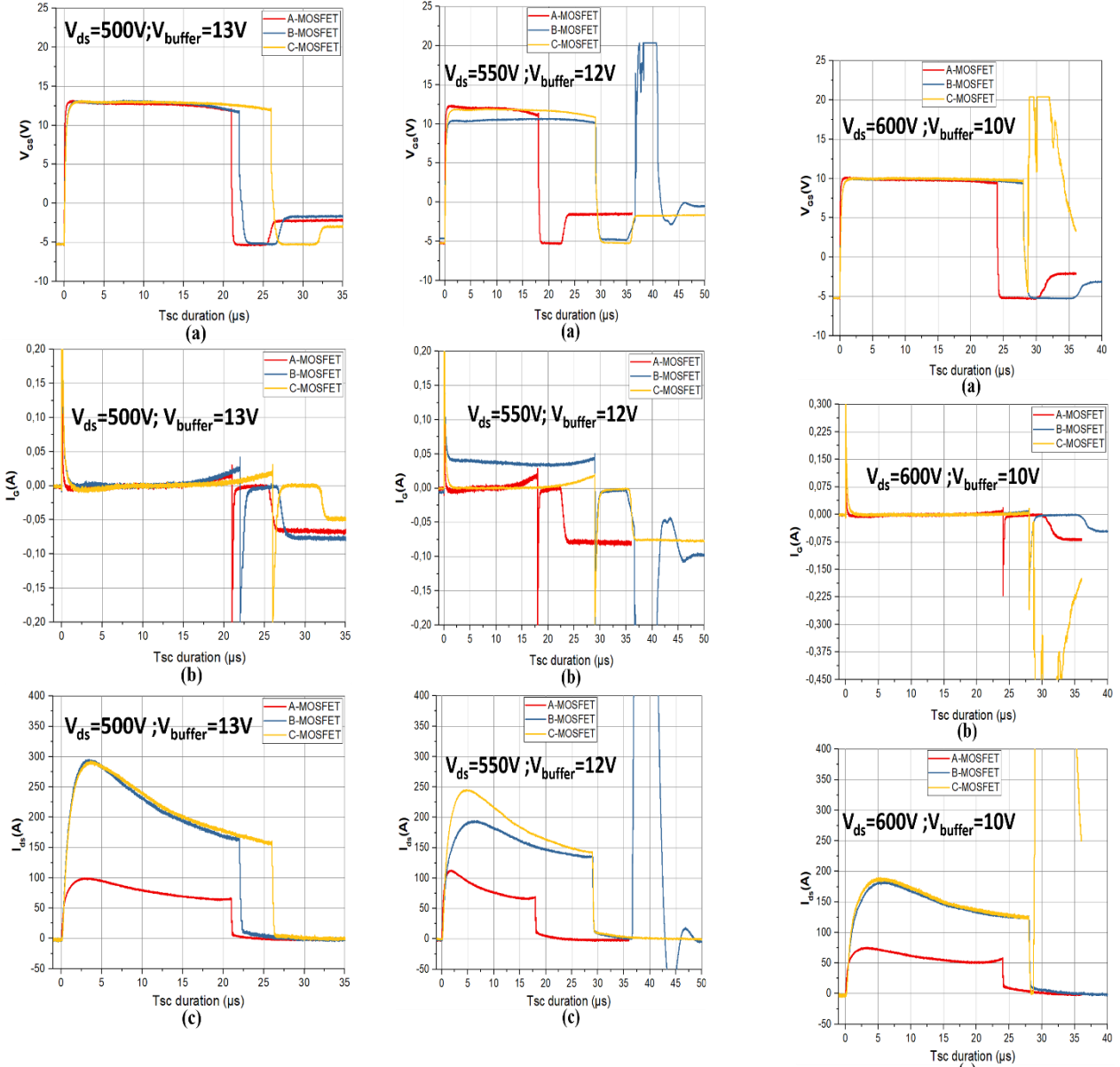


Fig. 2. Experimental waveforms during short circuit of the three MOSFET SiC DUT 1.2kV and 1.7kV (T_{CASE} = 25°C, R_G = 47Ω): (a) $V_{GS}(t)$, (b) $I_G(t)$ and (c) $I_{DS}(t)$.

- the critical power density or FTO/FTS boundary is a relatively constant quantity considering all devices, ranging only from $3.4kW.mm^{-2}$ to $4.2kW.mm^{-2}$ despite a significant difference in chip size and voltage rating. We can therefore

This model, developed by the authors in Comsol Multiphysics™ includes the fusion enthalpy of the Al layer at the top of the chip to take into-account its solidus – liquidus

phase transition. In Fig. 3a), melting is partial while in Fig. 3b) and c) melting is full. Note that the effect of the solidus – liquidus phase transition of the Al layer is clearly visible by the quasi-plateau shape of the transient temperature at the top layer.

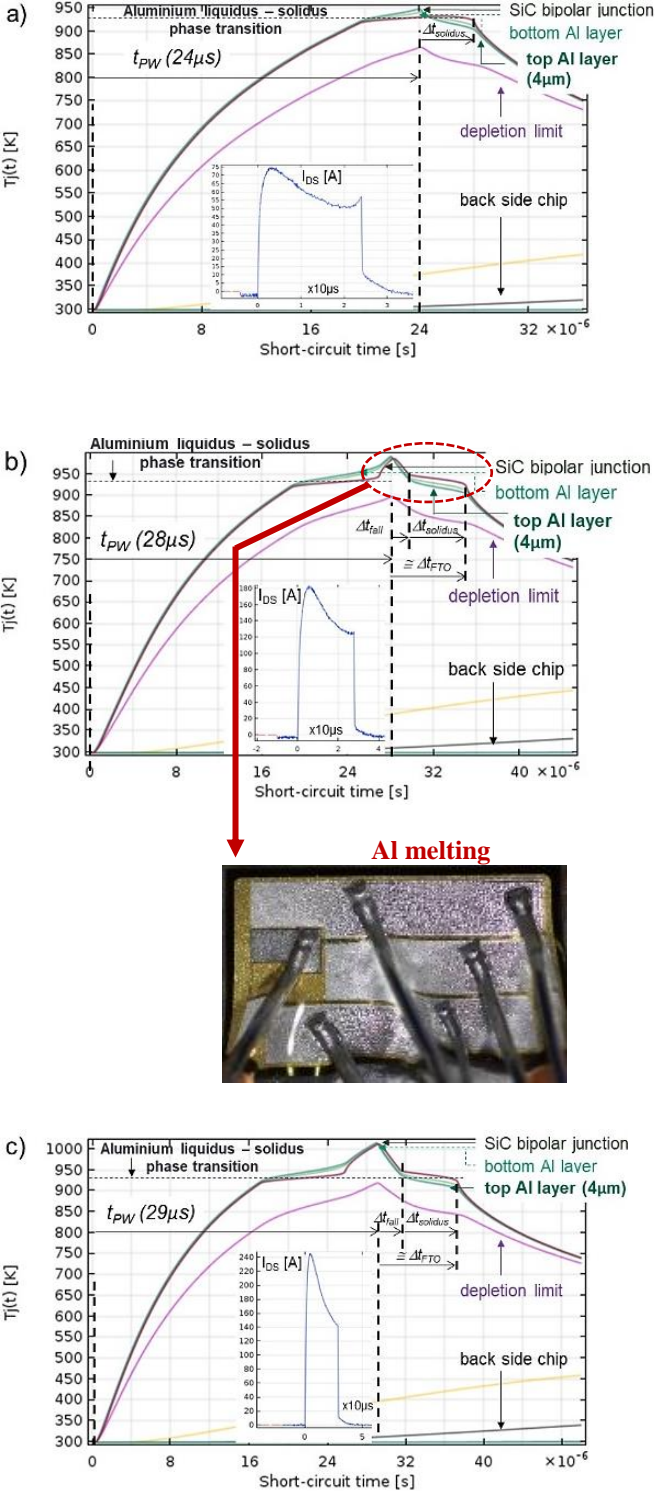


Fig. 3. SC transient thermal simulation, for all results @ $R_{gate\ ext.} = 47\Omega$, $T_{case} = 25^\circ\text{C}$; a) A-MOSFET 1.2kV, $t_{PW} = 24\mu\text{s}$, @ $V_{DS} = 600\text{V}$, $V_{buffer} = 10\text{V}$; b) B-MOSFET 1.2kV, $t_{PW} = 28\mu\text{s}$, @ $V_{DS} = 600\text{V}$, $V_{buffer} = 10\text{V}$; c) C-MOSFET 1.7kV, $t_{PW} = 29\mu\text{s}$, @ $V_{DS} = 550\text{V}$, $V_{buffer} = 12\text{V}$.

Indeed, during this sequence, the Al layer acts as a quasi-perfect local heat sink. The thermal energy taken from the chip allows the layer to change state, which slows down the temperature rise. Conversely, on cooling, this energy is released and the temperature decrease is slowed down. From simulation, in Fig. 3b), thanks to removable prototype case using silicone-gel, it can also be clearly observed and proved by the inset photo the melting and solidification of the Al top metal in coherence with the proposed simulation. Note that in all cases, gate-region temperature is greatly higher than the strength SiO_2 temperature $\approx 600\text{K}$ suggested by authors in [13] yielding to a possible path before Al melting. Finally, it can be noted that the delayed FTO mode observed in Fig. 2, fits quite well with the liquidus – solidus delay time of the Al top metal layer, from heat operation to cool-down operation, which enables to fix a permanent failure mode.

IV. R_{DSON} PENALTY

A strong reduction in gate voltage V_{GS} clearly has a direct impact on R_{DSON} and the on-state voltage drop. Indeed, by reducing the gate voltage closer to the threshold voltage, the channel resistance is directly and strongly increased. Fig. 4 shows the comparative behavior of the normalized R_{DSON} (V_{GS} , T_{CASE}) for A-, B- and C-MOSFET devices. At $T_{CASE} = 25^\circ\text{C}$ the penalty can be prohibitive, it is not the same at 150°C operating temperature. Indeed, the Coulomb scattering mobility component increasing with the temperature within $[25^\circ\text{C} - 150^\circ\text{C}]$ which comes to partially compensate the classical acoustic phonon mobility component which always decreases with the temperature. Furthermore, at this temperature, the 1.7kV device shows a better behavior because the relative channel resistance compared to the total resistance is lower, which makes it less sensitive than 1.2kV devices to the V_{GS} reduction with a penalty of 50% compared to $V_{GS} = 20\text{V}$. The acceptability of this penalty is related to the switching frequency used. For a high frequency application where the conduction losses would only represent 1/3 of the total losses, for example, a 17% increase in total losses is to be expected if a V_{GS} reduction is permanently applied.

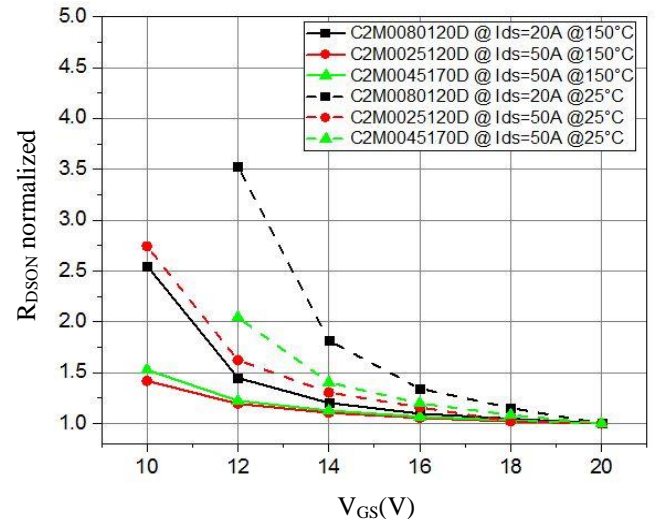
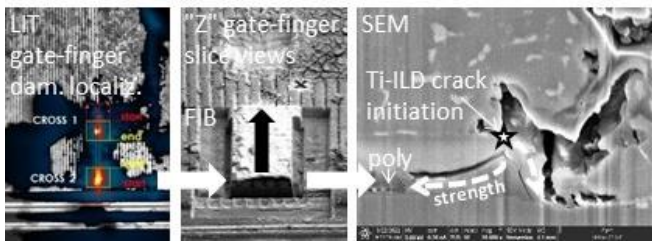


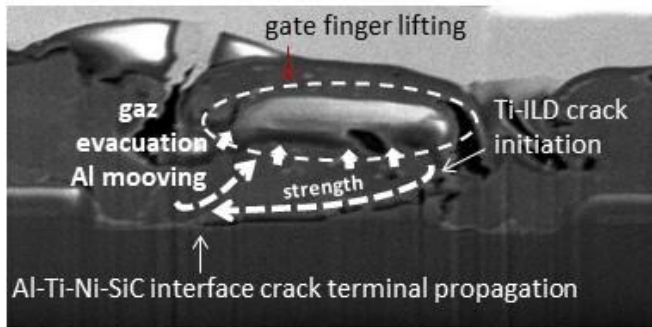
Fig. 4. Effect of V_{GS} depolarization on RD_{SON} as a function of T_{CASE} for A, B and C-MOSFET devices.

V. OPTICAL DAMAGE-MODE ANALYSIS

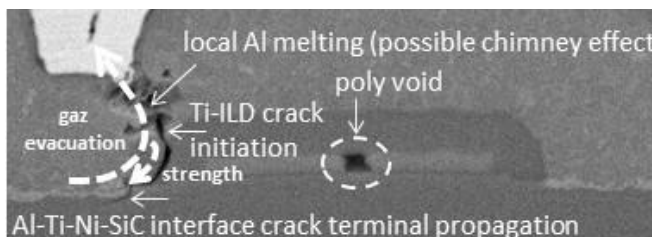
Lock-In Thermography for gate-damages localization (10Hz – 26Hz range, 16mW – 50mW self-heating), Focused Ion Beam (2 μ m) and Scanning Electron Microscopy have been realized on A-MOSFET 1.2kV and C-MOSFET 1.7kV. In Fig. 5 a) thanks to a LIT, gate-damage is fixed around a gate-finger near the gate-ring chip-edge. A FIB cutting and SEM analysis confirm a Ti-Internal Layer Dielectric (ILD) gate-crack form ILD corner to Si poly which probably proves the low-ohmic quasi-short path between gate and source as previously named FTO mode on A type. In Fig. 5 b) a spectacular lift-off effect of a gate-finger can be highlighted probably yielded by combination of the strength cracking (from top to bottom direction) and an Al melting moving (from bottom to top direction) at the edge and below the gate-damage region on A-MOSFET type. Finally, in Fig. 5 c) the same behavior as in b) can be observed on C-MOSFET type but with less melting and thermo-mechanical damage than A-MOSFET type, probably explained by a lower current density in the channels regions before the failure-mode of C type.



a) A-MOSFET 1.2kV Ti-ILD gate-crack from corner to Si poly.



b) A-MOSFET 1.2kV gate finger lift-off highlighting moving by strength crack and Al melting – gas.



c) C-MOSFET 1.7kV Ti-ILD corner – border crack initiation – propagation giving gas evacuation path.

Fig. 5. LIT, FIB slice views and SEM imaging on A-MOSFET 1.2kV and C-MOSFET 1.7kV.

VI. CONCLUSION

1.2kV and 1.7kV SiC MOSFETs robustness has been evaluated under short circuit operation. Two failure modes (FTO and FTS) are investigated using experimental results showing a power density boundary between 3kW.mm⁻² and 4kW.mm⁻². V_{GS} depolarization method is used to maintain a secure delayed failure-mode FTO. The results show promising enhancement in terms of short circuit time (T_{SCW}) that exceeds 10 μ s, and the appearance of FTO for both voltage rating. 1.7kV SiC MOSFET has the additional advantage of being 2-decade more robust on cosmic radiation. Using LIT and SEM imaging on 1.2kV and 1.7kV devices, a new and spectacular lift-off effect of the gate-finger region is highlighted, confirming gate-damage and FTO mode.

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