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► **To cite this version:**

Maxime Darnon, Mathieu de Lafontaine, Pierre Albert, Corentin Jouanneau, Thomas Bidaud, et al.. Sub-millimeter-scale multijunction solar cells for concentrator photovoltaics (CPV). SPIE OPTO 2022 - Physics, Simulation, and Photonic Engineering of Photovoltaic, SPIE, Feb 2022, San Francisco, United States. 10.1117/12.2613441 . hal-03781347

HAL Id: hal-03781347

<https://hal.science/hal-03781347>

Submitted on 11 Oct 2023

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Sub-millimeter-scale multijunction solar cells for concentrator photovoltaics (CPV)

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ABSTRACT

Concentrator photovoltaic (CPV) technologies provide the highest photovoltaic conversion efficiency but remain too expensive for very large scale development. Reduction of the dimension (micro-CPV) is a promising approach towards cost reduction but necessitates sub-millimeter-scale high efficiency solar cells. In this paper, we review the challenges faced by sub-millimeter-scale solar cells for application in micro-CPV. We show that plasma etching processes are necessary to fabricate sub-millimeter-scale high-efficiency solar cells to avoid a waste of material in the isolation and dicing lines. We also show that despite the cell performance is known to degrade when the dimension of the cell is downscaled, this degradation can be negligible when optimized etching and passivation processes are used and when the cell operates under high concentration ($>500x$). The through-cell via contact architecture is a promising approach to avoid bus bars on the front side and therefore optimize the wafer usage and minimize dark current. Combining all these solutions, we claim that sub-millimeter-scale high efficiency solar cells as small as 0.01 mm^2 can be fabricated with more than 90% of wafer material used for photovoltaic conversion and without performance degradation when operating under $1,000x$ concentration compared to 1 mm^2 solar cells operating under $500x$ concentration. Challenges on characterization and in-line metrology remain to be solved and manufacturing lines need now to be adapted to provide commercial solutions for micro-CPV.

Keywords: CPV, micro-CPV, high efficiency solar cells, multi-junctions, III-V materials, plasma etching, though cell via contacts

1. INTRODUCTION AND CONTEXT

Concentrator photovoltaics (CPV) is a technology that uses lenses or mirrors to concentrate the sunlight onto high-efficiency solar cells. Contrary to flat panel photovoltaics (PV) technologies that are dominated by silicon-based solar cells with theoretical efficiency limit of approximately 29%[1], concentrator photovoltaics uses multijunction solar cells based on III-V materials and germanium to increase the efficiency. In addition, sunlight concentration increases the flux density on the solar cells, and therefore increases the solar cells efficiency up to $>40\%$, until Joule losses induced by high current start to counter this effect [2]. For these reasons, concentrator photovoltaic systems have reached an efficiency of 38.9% in test conditions[3]. Commercial CPV systems manufactured by STACE have an efficiency of 33% which makes them the most efficient commercial technology for sunlight conversion into electricity. They use $>10\text{cm}^2$ silicone-on-glass lenses to concentrate the sunlight on few mm^2 solar cells placed near the focal point of the lens, $\sim 10 \text{ cm}$ away of the lens.[4]

Despite record efficiencies, CPV systems suffer from several challenges. First, the cost of CPV systems remains higher than the cost of flat panel PV technologies, except in regions with very high direct normal irradiance (DNI)[5]. This cost is partly due to the cost of the expensive multijunction solar cells, but also to the balance of system that includes 2-axis trackers and bulky panels shipping and handling. Indeed, commercial CPV modules are several centimeter-thick and need to be perfectly aligned with the sun so that the image of the sun lies on the smaller surface solar cells.

To overcome this limit, several groups are investigating submillimeter-scale concentrator photovoltaics (micro-CPV)[6][7][8][9][10]. This concept consists in downscaling the surface of the lenses and the solar cells. This reduction of the dimension leads to lighter and easier-to-handle modules that have the potential of reducing the cost of the balance-of-system [6]. In addition, smaller surface solar cells generate lower current per cell, and therefore less Joule losses, which opens the way to higher concentration ratios[11]. Other losses such as temperature-induced losses or top electrode shading losses can also be reduced when the cell dimensions are reduced to few hundreds of micrometers. Finally, micro-CPV can also embed micro-tracking technologies, for which the lenses are fixed but the cell panel is tracked to follow the course of the sunlight, which enables to fix CPV panels like flat panel PV and avoid the costly 2-axis trackers[11].

Ritou *et al.* [8] and Dominguez *et al.* [6] have reviewed the state of the art of micro-CPV modules. Both reviews show that micro-CPV modules can be fabricated with module efficiencies larger than 36%. They show also that the cell active area (aperture area) is in the range of 0.36 mm². Dominguez *et al.* claim that the cells dimension should remain above 0.25 mm² so that serial assembly remains feasible[6] while Wiesenfarth *et al.* mention a limit of 0.09 mm² to avoid too high performance reductions[12]. However, these limits depend on hypotheses on assembly cost and performance degradation due to area downscaling. In practice, no micro-CPV module has been fabricated with cell active area below 0.36 mm² due to the unavailability of commercial smaller dimension solar cells.

As a matter of fact, the future of micro-CPV technologies is hampered by the capacity to fabricate in high volume high efficiency sub-millimeter scale solar cells enabling modules below 0.5 \$/W. Assuming that solar cells correspond to 15% of the cost of the modules[2], have an efficiency of 44%, and that the concentration is 1,000x with optical efficiency of 95%, this means that the cost of the cell should not exceed ~3 \$/cm². Solar cells fabrication being performed by processes on full-size wafers (4- or 6-inch diameter), the cost of the processed wafers is independent on the surface of cells used for photovoltaic conversion (*i.e.* sum of the active area of all cells fabricated on the wafer). Therefore, it is necessary to have as much active area as possible per wafer to reduce the cost per cm².

For micro-CPV modules demonstrations mentioned by Ritou *et al.*[8], the aperture area (*i.e.* active area) was 0.36 mm² but the actual cell dimensions were closer to 1 mm², meaning that a large share of the wafer surface would be wasted. Schmieder *et al.* have fabricated multi-junction solar cells with an active area of 0.029 mm², but these cells remained on their native substrate (*i.e.* were not diced).[13] Wiesenfarth *et al.* have fabricated 0.166 mm² solar cells that were diced, but there is no indication of the actual size of the diced solar cells.[14] Albert *et al.* have demonstrated triple junction solar cells with an active area of 0.068 mm² using mainstream materials (InGaP/(In)GaAs/Ge).[9] These cells were diced into individual cells of 0.089 mm². These demonstrations showed that fabrication of sub-millimeter-scale multijunction solar cells is possible but requires specific process development. They also showed that perimeter recombination reduces the cell efficiency[9] and that the relative contribution of dark current on the photogenerated current due to increased relative surface of busbars leads to open circuit voltage reduction[14].

In this paper, we will review the challenges associated with sub-millimeter-scale multijunction solar cells, and we will propose solutions to mitigate these challenges. After discussing fabrication-related issues, we will focus on perimeter recombination and the impact of the bus bars on the dark current and wafer utilization. The challenges associated with characterization are then addressed before discussing the future of sub-millimeter-scale triple junction solar cells.

2. SOLAR CELLS FABRICATION

2.1 Challenges associated with sub-millimeter-scale multijunction solar cells fabrication

Fabricating a multijunction solar cell requires few microfabrication processes. An electrode is deposited and patterned by lift-off process on the front side and deposited on the back side. The front side electrode is made of few micron-wide lines of metal (fingers) linked to contact pads used for assembling the cells on receiver (bus bars). Wire bonding is the dominant assembly method and requires contact pads with a typical surface of 0.15x0.15 mm². [14] With most advanced wirebonding tools, the bond pad could be reduced down to 0.1x0.1 mm², but this would come with increased cost,

reduced reliability and reduced assembly throughput. Wet etching processes are used to etch the highly-doped III-V material between the fingers necessary for having an ohmic contact between the semiconductor and the metallic fingers. An antireflective coating is deposited on the front side and openings on the contact pads are formed by wet etching. The devices are isolated one from the other either by wet chemical etching or by partial saw dicing. The devices are finally separated from one another (singulated) by saw dicing.

Among these fabrication steps, we can identify two steps that cannot be used for submillimeter-scale solar cells fabrication: the isolation process and the singulation process. Indeed, in both cases, a diamond saw induces harsh mechanical stress that makes difficult the dicing of devices with a surface below 1 mm^2 . More importantly, the width of the dicing line (kerf) is larger than $75 \text{ }\mu\text{m}$ and damages the sidewall of devices.[15] This leads to a large waste of high-value material when more dicing lines are required per wafer, *i.e.* when the dimension of the solar cells is reduced.[9] Using wet chemical etching process would not help since it is not applicable for singulation (too long process) and isotropic etching leads to wide isolation lines that would also waste material at the sub-millimeter scale.

2.2 Proposed solutions for sub-millimeter-scale multijunction solar cells fabrication

It is necessary to replace saw dicing by alternative processes for cells isolation and cells singulation. For mainstream cell structures (InGaP/(In)GaAs/Ge), the device is $\sim 170 \text{ }\mu\text{m}$ -thick. To cut such a thickness, it is possible to use laser-based singulation processes. Conventional laser dicing methods are expected to enable the cut of $40 \text{ }\mu\text{m}$ -wide trenches through the germanium substrate.[9] However, local high temperature at the trench sidewall during the process deteriorates the device properties and leads to residues deposition. Figure 1a shows a cross section scanning electron microscopy (SEM) picture of a germanium substrate after partial laser dicing. It is clear that the device sidewalls are strongly damaged by the laser process and many residues are redeposited. The residues can partially be cleaned by an additional dipping in H_2O_2 as visible fig. 1b. However, to avoid device degradation, an initial isolation process is required to etch trenches that are large enough (typically $20 \text{ }\mu\text{m}$ wider than the width of the trench) to avoid exposing the III-V materials sidewalls to the high temperature process. Such large isolation trenches lead to a relatively large waste of surface that is not compatible with sub-millimeter-scale solar cells fabrication. Recent progresses in stealth dicing eventually combined with back-side grinding can enable dicing lines as narrow as $2 \text{ }\mu\text{m}$.[16] Such a process could avoid the need for isolation process since the sidewall of the device active region would be mechanically cleaved, and therefore are expected to have minimal damage. However, there has been no demonstration of stealth dicing processes on germanium substrate, and the effect of the process on the device properties is therefore not known.

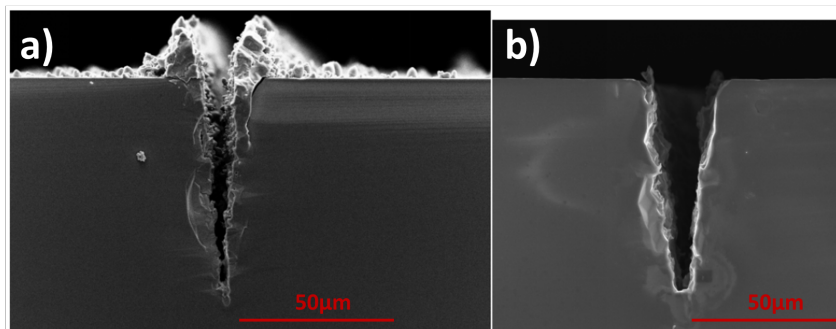


Figure 1. Cross section scanning electron microscopy image of a partial dicing in a germanium substrate before (a) and after (b) cleaning in H_2O_2 . Picture P. O. Downey.

Another option for cells isolation and singulation is to use plasma etching processes.[9][17] Indeed, our team has shown that $10 \text{ }\mu\text{m}$ -wide trenches can be etched through a $170 \text{ }\mu\text{m}$ -thick germanium substrate.[18] We also developed plasma etching processes to etch through the complex heterostructure of III-V materials that compose triple junction solar cells.[19] Combining those two steps, one can fabricate solar cells that are separated by $10 \text{ }\mu\text{m}$ -wide dicing lines.[17] The reduction of the width is limited by aspect ratio-dependent etching that slows down the etching process when the aspect ratio increases.[18] For thin cells architectures (*e.g.* inverted metamorphic cells), or by using back side grinding, the thickness of the devices can be reduced down to few tens of microns. In such case, we can anticipate that $1 \text{ }\mu\text{m}$ -wide dicing lines could be etched considering an aspect ratio of 17 being achievable by plasma etching.

Using plasma etching processes, we have fabricated sub-millimeter-scale triple junction solar cells presented figure 2. The smallest cell has an active area of 0.068 mm^2 and a total area of 0.089 mm^2 , demonstrating the feasibility of sub-

millimeter-scale triple junction solar cells fabrication.[9] We can see on this figure that plasma etching also enables the fabrication of versatile shapes of solar cells defined by lithography.

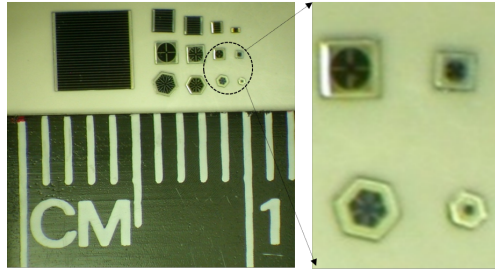


Figure 2. Optical picture of triple junction solar cells fabricated using plasma etching for isolation and dicing.

3. PERIMETER EFFECTS IN SUB-MILLIMETER-SCALE MULTIJUNCTION SOLAR CELLS

3.1 Challenges associated with sub-millimeter-scale multijunction solar cells

When the dimension of the solar cells is reduced, the relative impact of the perimeter on the cell performance is increased.[9][14][20] Indeed, charge carrier recombination is favored at the cell perimeter where defects provide recombination centers. These defects can be dangling bonds, impurities or surface oxides.[20] Increased recombination at the cell perimeter leads to a degraded ideality coefficient of the diodes, and therefore a reduced open circuit voltage (V_{oc}) for the cells.[21] Figure 3a presents the V_{oc} as a function of the perimeter/mesa area ratio (P/A) of the solar cells that were fabricated by Albert *et al.* [9]. The mesa area corresponds to the area delimited by the isolation process. We can clearly see that the open circuit decreases with the logarithm of the P/A ratio. Extrapolating this curve to larger P/A ratio, we estimate that The V_{oc} of 0.01 mm² solar cells is 7.8% lower than the V_{oc} of the 1 mm² solar cell. Downscaling the solar cells dimension will therefore lead to a decreased output voltage of the solar cells, and therefore a decrease of its efficiency if this degradation is not counterbalanced by positive effects of downscaling.

3.2 Mitigating perimeter effects in sub-millimeter-scale multijunction

The degradation of the V_{oc} is mostly linked to charge carrier's recombination at the perimeter of the cells. To mitigate this effect, it is therefore necessary to minimize the relative effect of these recombination on the cell's performance.

First, one can play on the isolation process to minimize the density of recombination centers at the cell perimeter. Using plasma processes for cells isolation offers indeed the opportunity to optimize the etching process for minimal surface damage.[17][22] Plasma etching processes rely on a synergetic effect between reactive radicals and ions coming from the plasma. Radicals can adsorb and eventually diffuse at any surface, while ion bombardment can break bonds and amorphize horizontal surfaces. By wisely choosing the plasma gas and process condition, one can use plasma processes to passivate defects that would result from discontinuing the semiconductor crystals at the cell perimeter.[17] We have demonstrated that using an hydrogen-rich plasma etching process, combined with an adequate cleaning process, the surface non-radiative recombination at the middle cell perimeter ((In)GaAs) could be similar to the ones of a mechanically cleaved sample. In addition, non-radiative recombination at the top cell perimeter (InGaP) could be significantly reduced compared to a cleaved semiconductor surface. Compared to other isolation methods such as wet chemical etching or partial saw dicing, this process improves the V_{oc} by 1 % for ~30 mm² solar cells.[15] When the P/A ratio increases, the optimized etch process keeps its superiority as illustrated figure 3a, with a V_{oc} improvement of 10 mV compared to sub-optimal plasma etching process for a P/A of 40 cm⁻¹ (1x1 mm² solar cell). Extrapolating the trend, we can anticipate a V_{oc} of 2.365 V for 0.01 mm² solar cell (P/A of 400 cm⁻¹) under one sun illumination.

A second measure that can be implemented after the isolation process is the passivation of the sidewall perimeter using a passivation process[22] or the deposition of a passivation layer[9]. Surface passivation of semiconductors can be induced by chemical passivation or field-effect passivation. Since the sidewall materials are complex with n-type and p-type regions of different materials, field passivation would require different materials along the height of the cells which is hardly feasible. Chemical passivation can be achieved using species that saturate dangling bonds or that inhibit non-

radiative combination centers.[22] Semiconductor surface passivation can be achieved by depositing hydrogen-rich $\text{SiN}_x\text{:H}$ layers by PECVD.[23] Such a material can also be used as an antireflective coating to maximize light collection.[24] When an optimized $\text{SiN}_x\text{:H}$ layer is deposited on solar cells, we can see figure 3b that the open-circuit voltage is increased and that the slope of the V_{oc} Vs P/A is reduced, indicating a lower surface recombination velocity. Extrapolating this trend, we can estimate that the V_{oc} of passivated 0.01 mm^2 solar cells is degraded by only 12.6% compared to passivated 1 mm^2 solar cells, and that the passivation process improves by 6.2% the V_{oc} of 0.01 mm^2 solar cells.

Surface recombination effect is also mitigated by operation of solar cells under concentrated sunlight. Indeed, under high concentration, the recombination centers get saturated, and their impact does not increase when the charge carriers' density increases.[21] For this reason, the relative impact of charge carriers' recombination at the perimeter decreases when the concentration factor increases. This effect is evidenced figure 3c, where the open circuit voltage of millimeter-scale and sub-millimeter-scale triple junction solar cells is plotted with respect to the sunlight concentration.[9] As expected, we see a logarithmic increase of V_{oc} when sunlight concentration is increased. Even if the slope is hardly changed, the relative degradation of the V_{oc} goes from 3.8 % at 1 sun down to <1.5% at ~250x for a 0.25 mm^2 solar cell compared to a 1 mm^2 solar cell. Extrapolating the trend of figure 3c and assuming no impact of series resistance on the V_{oc} at high concentration, one can assume an increase of the V_{oc} by 750 and 850 mV when the concentration factor is increased from 1x to 500x and 1,000x, respectively, leading to lower relative impact of the V_{oc} degradation.

By combining optimized isolation process and surface passivation methods, and operating under high concentration, the relative effect of perimeter recombination will therefore be minimized. Extrapolating our results and using the V_{oc} of solar cells isolated with optimized plasma etching process, we can anticipate that 0.01 mm^2 solar cells passivated with $\text{SiN}_x\text{:H}$ passivation and operating under 1,000x would have a V_{oc} of 3.36 V (see table 1). This is 0.3 % lower than the V_{oc} of a passivated 1 mm^2 solar cells under 1,000x concentration but 3.3 % higher than the V_{oc} of a passivated 1 mm^2 solar cells operating under 500x concentration. These estimations assume that the passivation process leads to the same absolute V_{oc} improvement whatever the plasma etching process used for the cell's isolation. It also does not take into account the effect of temperature on the V_{oc} that is expected to depend on the dimension of the cells and on the concentration factor. Even though these estimations are oversimplifying, they indicate that appropriate isolation and passivation processes would enable the fabrication of sub-millimeter-scale solar cells with no significant impact of the perimeter recombination on the cells performance.

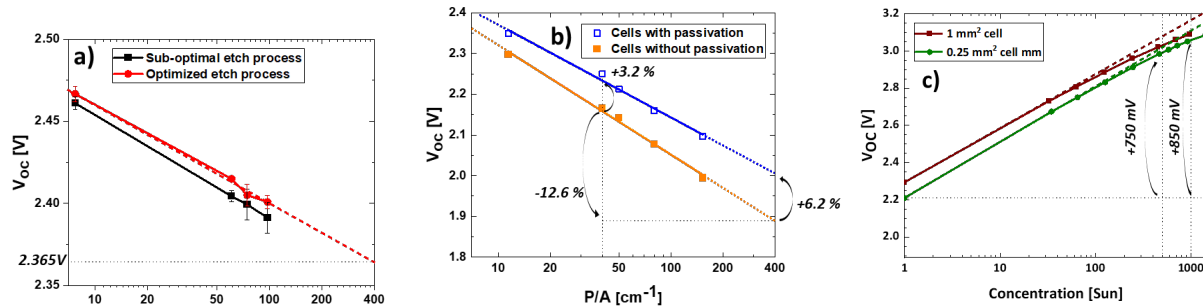


Figure 3.a. Evolution of the V_{oc} measured at one sun as a function of the perimeter / mesa area ratio (P/A) for triple junction solar cells fabricated with optimal and sub-optimal plasma etching process. b. Evolution of the V_{oc} measured at one sun as a function of P/A for triple junction solar cells fabricated with or without passivating anti reflective coating. c. Evolution of the V_{oc} of 1 mm^2 and 0.25 mm^2 triple junction solar cells as a function of sunlight concentration.

Table 1. Extrapolated open circuit voltage for 1 mm² and 0.01 mm² solar cells with or without surface passivation, and operating under 1, 500 or 1,000x sun illumination.

Concentration	<i>V_{oc}</i> of 1 mm ² solar cell		<i>V_{oc}</i> of 0.01 mm ² solar cell	
	w/o passivation	w/ passivation	w/o passivation	w/ passivation
1x	2.42V	2.50V	2.365V	2.51V
500x	3.17V	3.25V	3.115V	3.26V
1,000x	3.27V	3.35V	3.215V	3.36V

4. IMPACT OF BUSBARS ON SUB-MILLIMETER-SCALE MULTIJUNCTION SOLAR CELLS

4.1 Limitations associated to bus bars

To integrate solar cells into concentrator photovoltaic modules, it is necessary to interconnect each solar cell one to the other. The conventional method for triple junction solar cells contacting is to use gold wire bonding. Such a method necessitates bonding pads on the solar cells with a typical surface of 0.0225 mm². These pads (also called bus bars) have negative effects for the solar cells.[14] Indeed, the area under the bus bars is shaded and is therefore not used for converting sunlight into electricity. Their surface is generally not counted in the active area of the cell and can be considered as wasted area, which reduces the amount of energy that can be produced per wafer.[25] In addition, this shaded area contributes to the dark current of the solar cell. The ratio between the dark current and the photogenerated current determining the open-circuit voltage, the presence of bus bars leads to a loss of *V_{oc}*. [14]

When the area of the solar cells is downscaled, the effect of the busbars becomes relatively more important. Indeed, the bond pads for wire bonding cannot be below 0.01 mm² to enable wire bonding. For solar cells with an active area of 0.01 mm², the busbars correspond to 50% of total surface of the solar cells (~0.02 mm²), which would lead to dramatic open circuit degradation and unacceptable materials loss.

4.2 Suppressing bus bars

The need for bus bars is intimately related to the use of wire bonding processes for solar cells interconnections. To solve the issues related to the bus bars, it is therefore compulsory to modify the cells interconnection methods to avoid wire bonding processes.

There are few alternatives to wire bonding technologies. In the semiconductor industry, flip-chip technologies are the main alternative to wire bonding. This approach has been proposed for CPV applications by Panasonic which has demonstrated the fabrication of micro-CPV modules using flip chip interconnects.[26] The concept is to fabricate redistribution layers using microfabrication methods (*i.e.* lift-off deposition and patterning of metal lines) to transfer the front contact to a semi isolating substrate. Even though this approach reduces the shading due to bonding pads, the surface of one solder bump for flip chip technology remains in the order of 0.005 mm² and cannot be scaled down.[27] Assuming two solder bumps per cell, the surface required for flip-chip packaging is similar to the one needed for wire bonding. Therefore, the surface wasted for cells contacting would be prohibitive for sub-millimeter scale solar cells.

Panasonic have also proposed to transfer the contact pads from the front side of the cell towards its back side by using vias in the semi insulating substrate.[28] Even if this approach is efficient to avoid the bus bar on the cell front side—and therefore limits the impact of the shading on the *V_{oc}*—it still requires real-estate on the substrate to transfer the contact. As an example, the cells used by Panasonic [28] used 0.855 mm² of surface for an active area of 0.25 mm², meaning that ~70% of the surface of the cell was not active and therefore wasted in terms of photovoltaic conversion. The issue of material waste remains therefore unsolved by microfabricated interconnects.

The most efficient solution to bus bar suppression is to transfer the top electrode contact towards the back side of the cell using vias embedded into the solar cells. The “through-cell via contact” (TCVC) architecture proposed by Richard *et al.*[25][29][30] consists in using insulated metallic vias through the cell to transfer the busbars towards its back side. Using this approach, no more busbar is required on the front side, and the two contacts are on the back side. The cell can

eventually be assembled using surface mount technologies. Two groups have reported multijunction TCVC solar cells.[31][32] In both cases the contact surface on the front side was negligible compared to bus bars (23 μm -diameter and 14 μm -diameter disks for Oliva *et al.* and de Lafontaine *et al.*, respectively). Figure 4 presents a 0.18x0.18 mm² triple junction TCVC cell with one single via. This cell has a shaded area of 907 μm^2 , which corresponds to 2.8% of the cell area. Through-cell vias contact avoids therefore both the reduction of the V_{oc} and the waste of material associated to the bus bar, while enabling the assembling and interconnection of sub-millimeter-scale multijunction solar cells.

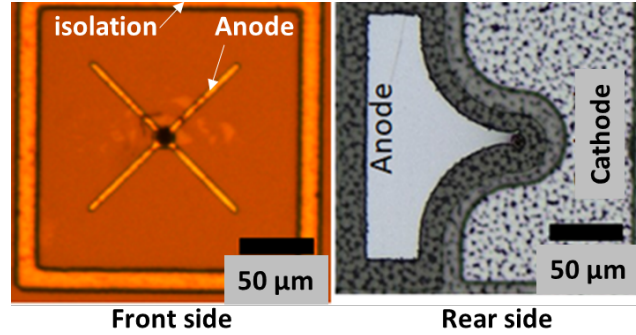


Figure 4. Optical picture of a 0.18x0.18 mm² triple junction TCVC solar cell.

5. CHARACTERIZING SUB-MILLIMETER-SCALE MULTIJUNCTION SOLAR CELLS

A final challenge associated with sub-millimeter-scale triple junction solar cells is their characterization. Indeed, conventional methods for solar cells characterization are not straightforward to be applied to sub-millimeter-scale solar cells. For multi-millimeter-scale solar cells, it is well known that sun simulators (either for 1 sun or for concentration measurements) must present an excellent uniformity and spectral content for accurate cells characterization.[2] Triple A+ simulators have a spectral match of 0.875 to 1.125 for all intervals, a uniformity of irradiance better than 1% and temporal instabilities below 1%. Even if these characteristics are guaranteed at the millimeter scale, our experience is that it is not necessarily verified at the sub-millimeter scale. In addition, the surface being very small, the current produced per cells is in the range of few hundred micro Amps (*e.g.* ~150 μA for 0.01 mm² cells). Any stray light or reflection on the probes has therefore a larger relative contribution on the measured current which can be difficult to discriminate. External quantum efficiency is also difficult to assess for sub-millimeter-scale solar cells. Indeed, conventional methods [2] use a spot size of ~1 mm². This spot size and precise position depend on the wavelength because of achromatism in the measurement system. These systems are therefore not usable for solar cells with a surface below 1 mm².

The problem of solar cells characterization becomes even more stringent when one considers high volume manufacturing of sub-millimeter-scale solar cells. Indeed, each cell must be characterized individually so that cells are binned into batches of cells with identical characteristics, and out-of-specification cells are identified before being assembled. Conventional methods with probe cards would need to be adapted for fast characterization of hundreds of thousands of cells. The eventual reduction of the busbar dimension or their transfer to the back side of the cells (TCVC approach) would make this even more difficult.

6. DISCUSSIONS AND PERSPECTIVES

Micro-CPV technologies are an interesting pathway towards more competitive concentrator photovoltaics technologies that require high-efficiency sub-millimeter-scale solar cells. To date, there is no established supply chain for such small cells, and methods used to fabricate and interconnect current multi-millimeter-scale high-efficiency solar cells must be revisited. When the dimension of the solar cells is downscaled, the relative impact of the isolation and dicing lines, as well as of the bus bar become more and more important. We have seen that plasma dicing technologies can be used for cells isolation and dicing with dicing lines of 10 μm width, and that this width could be reduced to ~1 μm if thin cells such as inverted metamorphic cells are fabricated. Using optimized plasma etching, cleaning, and surface passivation processes, the recombination at the cell perimeter can be reduced, so that they lead to no significant V_{oc} loss when the cells are operating under high concentration factors—other benefit from micro-CPV approach (lower temperature, lower series resistance) not being considered. The TCVC approach that suppresses the need for bus bars on the front side of the

cell is a key enabler of micro-CPV technologies, since it avoids waste of material and V_{oc} losses due to relatively high saturation current.

The impact of these various implementations depends on the targeted cells dimensions. We have discussed in part 3 the impact of perimeter recombination as a function of the P/A ratio. From the material utilization standpoint, the benefit of plasma-based isolation/singulation processes and the impact of the TCVC architecture is plotted figure 5. To build this figure, we calculated the percentage of the wafer used for the active area, the bus bars, and the isolation/singulation lines, as a function of the cell active area. We considered solar cells with square active area, one 100 μm -wide bus bar on one side of the cell (aggressive assumption for wire bonding), and 75 μm -wide isolation/dicing lines (aggressive assumption for saw dicing), as schematized on figure 5. We also plotted the surface wasted by the isolation/dicing lines assuming 5 μm -wide lines (conservative assumption for plasma dicing) and no bus bar (TCVC architecture). We can see on this figure that even if the bus bars represent $\sim 8\%$ of the wafer surface for 1 mm^2 solar cells, this surface strongly increases for solar cells smaller than 1 mm^2 and reaches more than 20% of the wafer's surface for 0.01 mm^2 cells. With the TCVC architecture, all this material would be usable for more solar cells fabrication per wafers. The isolation/dicing lines have an even larger impact on material utilization. They represent 13% of the surface of the wafer for 1 mm^2 solar cells and close to 60% of the wafer for 0.01 mm^2 solar cells. Transitioning from a saw dicing process to a plasma etching process would therefore have a tremendous impact. Combining the TCVC architecture with plasma-based isolation/dicing process, and assuming 5 μm -wide isolation/dicing lines, the wafer utilization would be $>90\%$ for solar cells with active area as small as 0.01 mm^2 . Such a large wafer surface utilization is very promising for minimizing the cost of high-efficiency triple junction solar cells for micro-CPV applications.

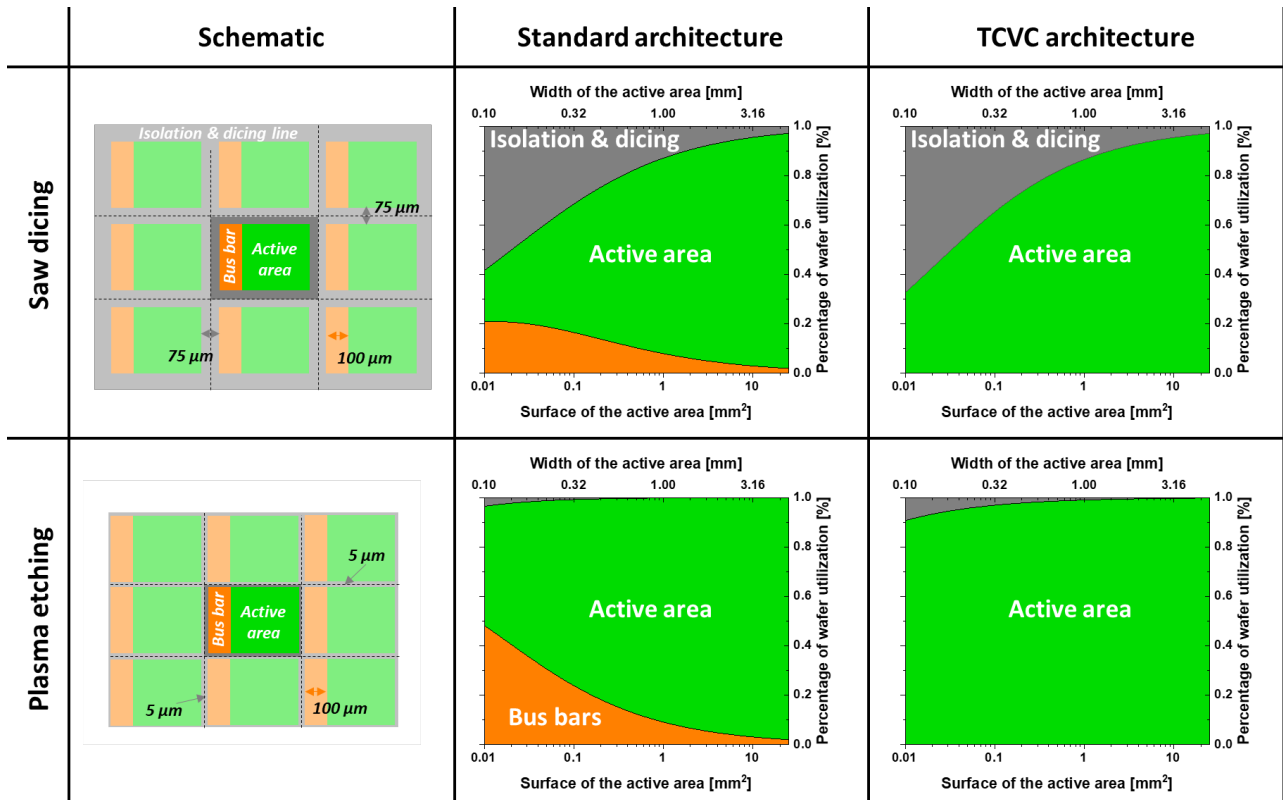


Figure 5. Representation of the wafer surface utilization as a function of the cell active area surface for standard or TCVC architectures, and considering saw (partial) dicing or plasma etching for isolation and dicing. The schematic on the left-hand side presents the dimension and shape of solar cell chosen to build the figures.

There are therefore technological solutions to fabricate sub-millimeter solar cells with no significant open circuit losses, and very efficient wafer utilization. Solar cells suppliers must now implement these methods in production lines to enable the development of a micro-CPV technologies. All the methods proposed here are based on micro fabrication methods that are conventional for the semiconductor industry, but much less common for companies specialized in high-efficiency solar cells fabrication. Developing manufacturing lines with plasma etching processes, and toolset

necessary for TCVC cells fabrication will therefore require strong efforts from the solar cells' suppliers. In addition, challenges remain to be solved on in-line metrology for sub-millimeter solar cells characterization. CPV systems developers will also have to adapt their manufacturing methods not only to handle sub-millimeter-scale solar cells, but also to assemble the cells without wire bonding, using for instance surface mount technologies. All these efforts necessitate significant investment but are compulsory if one wants to envision high volume manufacturing of micro-CPV modules.

ACKNOWLEDGEMENTS

LN2 is a joint International Research Laboratory (IRL3463) funded and co-operated in Canada by Université de Sherbrooke and in France by CNRS as well as INSA Lyon, Ecole Centrale Lyon and Université Grenoble Alpes. It is also supported by the Fonds de Recherche du Québec Nature et Technologie (FRQNT). Pierre Olivier Downey is acknowledged for laser dicing pictures. The support of NSERC, Prompt and STACE in the framework of the MARS-CPV project is acknowledged.

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