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Electromagnetic analysis of switching cells with dies embedded in printed circuit boards: Application to TAPIR (compact and modular Power modules with Integrated cooling) technology

W-F. Bikinga, Y. Avenas^{*}, K. Alkama, B. Mezrag, J-M. Guichon, J-L. Schanen

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ABSTRACT

The TAPIR technology (compact and modular Power modules with Integrated cooling) requires a multiphysics analysis to prove its interest compared to current power module solutions. To contribute to this objective, this paper focuses on magnetic aspects and, more specifically, on stray inductance evaluation. Through simulation and experimental studies, it is shown that stray inductances close to 1nH can be obtained. Several design aspects are also studied: the presence of inner layers in the PCB and the decoupling capacitors arrangement. Furthermore, the magnetic interactions between switching cells is studied by simulations and experiments. It is shown that the presence of an adjacent cell reduces slightly the stray inductance (max 20%). In the case of paralleled switching cells, it is also demonstrated that an alternated position of DC link heat sinks can induce a 30% reduction of the stray inductance.

1. Introduction

With their higher switching speeds compared to silicon devices, wide band gap devices allow increasing the efficiency of static converters and/or improving their compacity. Particularly, in the field of high-power converters, the superior behavior of SiC devices is proven by many works in the literature. For example, Soltau et al. (Soltau et al., 2020) compare the losses of a railway traction inverter using 3.3 kV SiC MOSFETs and Si IGBTs having the same current ratings, and the same package. The results exhibit 59% loss reduction in favor of SiC devices. With such loss reduction, very high efficiency levels can be reached as shown by Li et al. (2020) who present a 500 kW three-phase inverter made with SiC MOSFETs that achieves an efficiency of 98.74%. Haihong et al. (2016) compare a 1 kW permanent magnet synchronous drive inverter made with Si IGBTs and another one made with SiC MOSFETs. The results show an efficiency improvement of 1 % for the prototype using SiC MOSFETs. Rujas et al. (2017) demonstrate a 30% volume reduction when using SiC MOSFETs in the case of a 25 kW DC/DC railway converter.

However, to actually benefit from the superior performances of SiC devices, their packaging must be adapted. Indeed, the increase of the switching speed as well as the decrease of the die surface require new packaging techniques with suitable parasitics (stray inductances and capacitances) and low thermal resistance. Several literature surveys are available regarding these topics (Lee, Smet, and Tummala, 2020; Hou

et al., 2020; Chen, Luo, and Kang, 2017; Alizadeh and Alan Mantooh, 2021). To summarize, the design of a power module results from the trade-off between parasitics and thermal management, also considering reliability and voltage withstand issues. Performances can be improved by new architectures (double side cooling (Ding et al., 2021), chip-on-chip (Regnat et al., 2018)...) or new processes or materials (die attaches (Zhang, Damian, and Zijl, 2021), substrates (Rajagopal et al., 2021),...). Also, PCB (printed circuit board) embedding technology is currently under the focus of intense researches (Caillaud et al., 2019; Hou et al., 2019; Knoll et al., 2021; Yang and Emadi, 2020; Pascal et al., 2018; Tablati et al., 2020) due to its versatility and the possibility of obtaining designs with very low stray inductances.

In previous work from the authors (Bikinga et al., 2020, 2021), an assembly called TAPIR (compact and modular Power modules with Integrated cooling) was proposed to optimize the weight and volume of power converters with air cooling systems. This technology is based on a modular arrangement of 3D switching cells which is able to distribute the heat in the whole heat sink volume and to limit the number of thermal interfaces. An example of one switching cell is presented in Fig. 1: the electrical connections are done by the heat sinks and the power devices are embedded in a PCB between them. Thus, there is no insulating material between the heat sinks and the devices which are cooled on their both sides. As a consequence, the thermal resistance can be quite low and reach values comparable to thermal resistances obtained with water cooling as shown in (Bikinga et al., 2020). Also,

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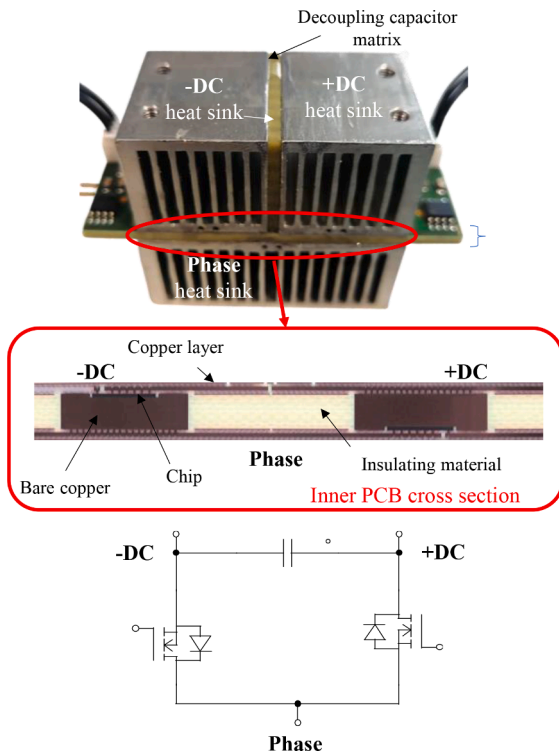


Fig. 1. TAPIR switching cell including an inner PCB fabricated with p²Pack Embedding Technology © (cross cut) - Courtesy of Schweizer Electronic AG.

capacitive elements can be integrated between +DC and -DC heat sinks to act as decoupling capacitors. It was demonstrated in Bikinga et al. (2020) by an experimental setup that the stray inductance of this switching cell could be close to 2 nH which makes it compatible with the use of fast switching devices.

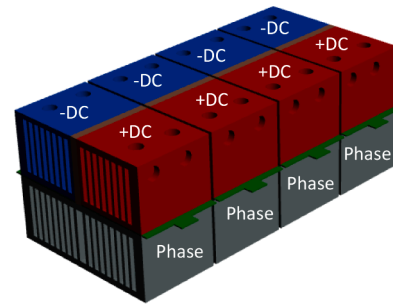
To build a power electronics converter, the switching cells are assembled in a complete 3D architecture. For instance, Fig. 2 presents different possible assemblies for paralleling 4 switching cells. In Fig. 2a, the switching cells are positioned one in front of the other. In this configuration, the airflow crosses successively each element. Their temperature is therefore not homogeneous. Fig. 2b proposes another configuration where 2 × 2 switching cells are crossed by the same airflow. The temperature is therefore more homogeneous and the shape factor of the system is modified. Finally, Fig. 2c presents another configuration where all switching cells are crossed by the same airflow but the position of the DC link is alternated for each successive cell. The interest of this configuration will be studied later in this paper.

The implementation of this technology is not simple and must face a lot of challenges. They are detailed in (Bikinga et al., 2021) and concern principally the design of the elementary switching cell itself (thermal, electromagnetic, voltage withstand, reliability issues) but also the global assembly (mechatronic integration, thermal and magnetic coupling between cells, EMI mitigation, reliability...).

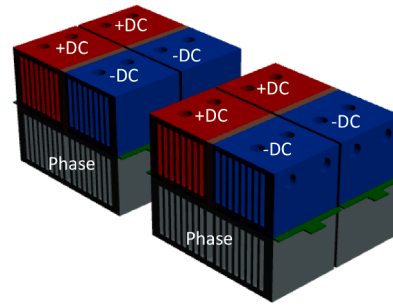
The present paper will focus on electromagnetic aspects. The main goals of this research work are the following:

- Propose simulation and experimental strategies to estimate the achievable switching cell stray inductance when using this technology,
- Compare different switching cell architectures to help the designer,
- Evaluate the impact of magnetic coupling between nearby switching cells and propose an experimental and simulation methodology to carry out this evaluation.

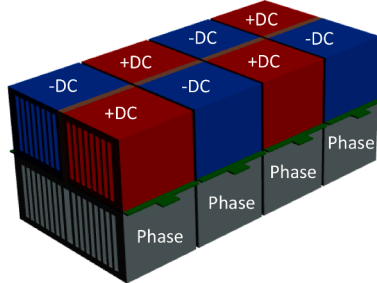
The following section is dedicated to the presentation of tools used



(a) 4 successive switching cells



(b) 2×2 successive switching cells



(c) Four successive switching cells with alternated positions

Fig. 2. Different configurations for paralleling 4 switching cells.

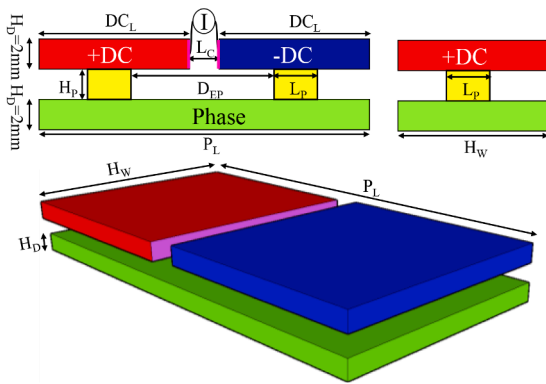
for stray inductance evaluations. A software is chosen and an experimental device is described. This device is based on the PCB presented in Fig. 1 and includes 80 V – 0.9 mΩ – 360 A Si MOSFET chips. Then Section 3 compares different switching cell architectures: with internal layers in the PCB and with different decoupling capacitor arrangements. Section 4 is dedicated to the study of magnetic interactions between adjacent switching cells. Finally, Section 5 proposes discussions about the results.

2. Methods and materials for stray inductance evaluation

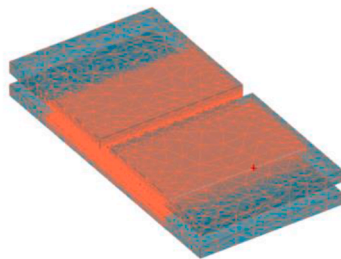
2.1. Simulation strategy

2.1.1. Choice of the simulation software

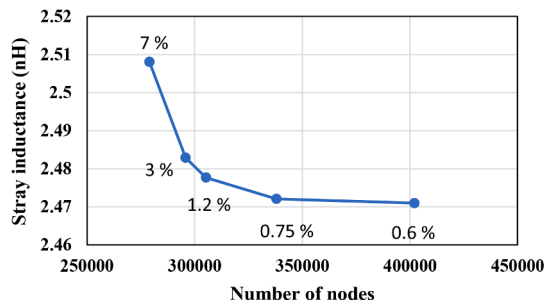
Several solving methods can be used to model eddy currents in power electronics systems. The PEEC (Partial Element Equivalent Circuits) method (Ruehli, 1974; Schanen and Roudet, 2008) is well suited for modeling thin wire-like conductive regions. However, the standard PEEC method is not adapted to the modeling of massive conductors (3D currents) and therefore to this work which uses massive heat sinks as power connectors. The finite element method (FEM) is known as an effective tool for the calculation of 3D electromagnetic fields and eddy currents. However, this method is very sensitive to the meshing which determines the accuracy of the solution and is also time consuming. As a consequence, the homemade MIPSE software (Modeling of Inter-connected Power SystEms) is chosen to perform the electromagnetic study of the TAPIR technology. It is based on integral methods



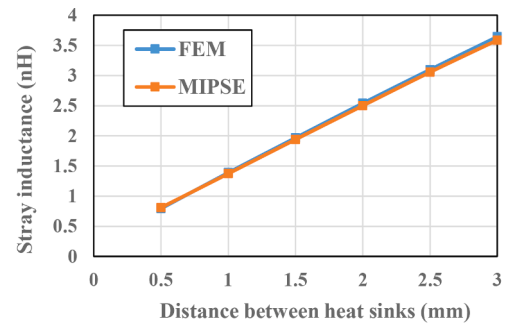
(a) Geometry and parameters: side view (top) and global view (bottom)



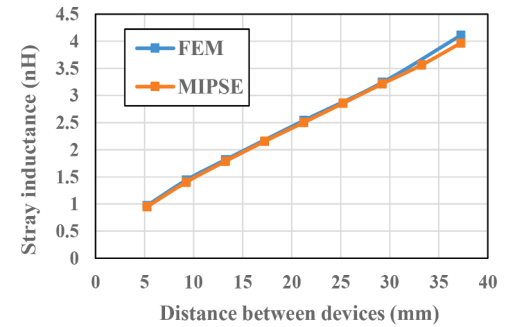
(b) Meshing of the geometry (FEM simulation)



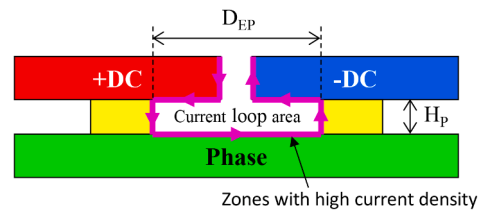
(c) Meshing sensitivity study – the number in % is the ratio of poor-quality elements



(a) Impact of the distance between DC and phase heat sinks H_F



(b) Impact of the distance between devices D_{EP}



(c) Schematic of the current loop (cross section)

Fig. 4. Comparison between FEM and MIPSE simulations and parametric study.

study and making a first parametric study.

2.1.2. Validation

The validation is carried out with a simplified geometry (Fig. 3). The thickness H_D of +DC, -DC and Phase heatsinks is 2 mm. The PCB is not represented but the semiconductor chips as well as their electrical connections inside the PCB are represented by two $5\text{ mm} \times 5\text{ mm} \times 2\text{ mm}$ conductive blocks. The other geometrical parameters are represented in Fig. 3 and summarized in Table 1. For the stray inductance calculations, a current is injected between the internal vertical sidewall areas of +DC and -DC blocks. These surfaces are highlighted in purple in Fig. 3a. They are at constant potential; the injected current is therefore non-uniform. The voltage is then measured across these equipotential surfaces to estimate the stray inductance of the switching cell.

A frequency analysis was done and showed that the stray inductance remains constant beyond 1 MHz. Also, the equivalent frequency during switching and oscillation regimes which will be observed later in the paper are typically several tens of MHz. For the calculations, the operation frequency is thus chosen to be 100 MHz.

The meshing of the system is done carefully for FEM simulations: high mesh density at the surfaces of conductors with high current density (Fig. 3b), and adapted size of the infinite box around the switching cell. A meshing sensitivity study was carried out to determine the necessary number of nodes (Fig. 3c). A number close to 400000 was chosen due to the low ratio of poor-quality elements ($< 1\%$) and the convergence of the stray inductance value. The meshing is automatically

Fig. 3. Simplified geometry of a switching cell for electromagnetic simulations and meshing.

Table 1

Geometrical parameters of the simulation study.

Parameter	Name	Value
Heat sink height	H_D	2 mm (§2.1 and 3.1) 20 mm elsewhere
Distance between chips	D_{EP}	20 mm Variable in §2.1.2
Distance between DC link and Phase	H_p	2 mm Variable in §2.1.2
Chip width	L_p	5 mm
Distance between +DC and -DC	L_c	2.5 mm Variable in §3.2
Heat sinks width	H_w	25 mm
DC heat sinks length	DC_L	23.75 mm Variable in §3.2
Phase heat sink length	P_L	50 mm

(unstructured PEEC) (Meunier et al., 2019; Siau et al., 2016) with matrix compression to limit the required computation time and memory space. It also integrates an automatic meshing tool (Alkama et al., 2021).

In the following paragraph, electromagnetic simulations on a simple geometry will be carried out with MIPSE and a commercial FEM software (Altair Flux^{3D}). It will allow validating the use of MIPSE in this

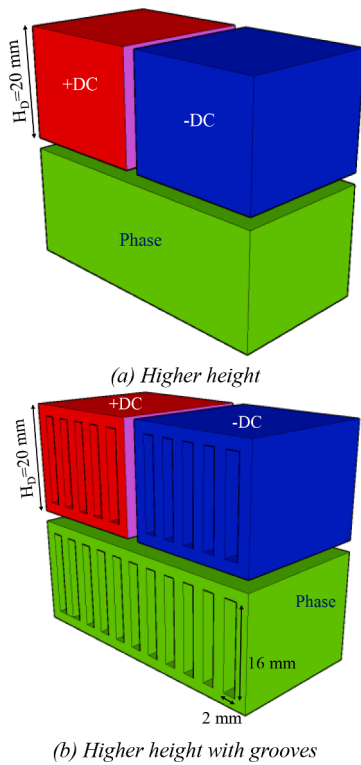


Fig. 5. Different heat sink geometries.

Table 2
Stray inductance for different heat sink configurations.

	Fig. 3	Fig. 5a	Fig. 5b
Stray inductance (nH)	2.47 nH	2.50 nH	2.50 nH

done when using MIPSE.

The influence of two geometrical parameters is presented: the distance between DC link and phase heat sinks (H_D) and the distance between both semiconductor devices of the switching cell (D_{EP}) (as displayed in Fig. 3a). Fig. 4 shows the simulation results. The stray inductance increases logically with H_D and D_{EP} . To explain this variation, Fig. 4c presents the location where the current density is the highest due to skin effect. Thus, when D_{EP} or H_D increases, the area of the current loop increases and, as a consequence, the inductance also increases.

It is observed that very low stray inductances can be obtained. If H_D is 0.5 mm, an inductance lower than 1 nH is estimated. However, to design a TAPIR switching cell, a trade-off must be done between this inductance and the stray capacitance induced by such proximity between heat sinks. Also, the distance between semiconductor chips can be reduced to decrease the stray inductance to 1 nH. In this case, a trade-off between this value and the thermal coupling between chips must be done to fix this parameter.

Finally, a maximum difference of 2% is observed between both simulation tools which shows that MIPSE is able to estimate accurately the stray inductance of TAPIR switching cells. It will therefore be used in the following paragraphs.

2.1.3. Physical description of heat sinks

For simplifying simulations, it is interesting to observe if an accurate description of the heat sinks is necessary or not to obtain good stray inductance estimations. In this objective, 3 heat sink geometries are compared: the one presented in Fig. 3a, the same with heat sinks having an increased thickness $H_D=20$ mm (Fig. 5a) and the same than Fig. 5a

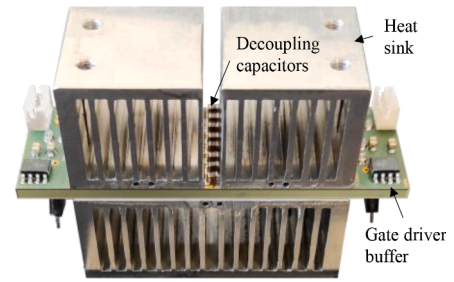


Fig. 6. Switching cell with SMD capacitors soldered on the top of the PCB.

but with cooling grooves (Fig. 5b). The results presented in Table 2 shows that the height has a very low influence on the results (lower than 1% in this example).

The low influence of heat sink height is mainly due to the chosen boundary conditions. Indeed, the current is injected on surfaces at constant potential. The injected current density is therefore not constant on these surfaces. Due to the constant potential, the current along the height of the heat sink is very low and the main injection is thus localized at the bottom part of the heat sink. Note that new boundary conditions will be proposed in § 3.3 to be more representative of capacitor matrixes.

The representation of grooves has a negligible effect because the current density is the highest on the internal surfaces of the geometry and is very low in the bulk (Fig. 5c).

2.2. Experimental device

The switching cells implemented in this study could be used in 48 V automotive applications like Belt Starter Generators (BSG) (Si et al., 2021). They were fabricated based on p²Pack Embedding Technology © (Schweizer Electronic AG) (Gottwald and Roessle, 2019) (Fig. 1). They include bare MOSFET chips dedicated to automotive 48 V applications. As SiC devices, the high switching speed of these devices associated with the low DC link voltage necessitate the fabrication of low inductance switching cells to limit the overvoltage during turn-off. As shown in Fig. 1, both MOSFETs are oriented in opposition in the PCB to respect the construction of TAPIR switching cells. The chips are assembled on bulk copper blocks to improve conduction heat transfers, the connections to external layers of the PCB are done by microvia arrays. The external dimensions of the PCB are 70 mm × 25 mm × 2 mm. Unfortunately, the different layer thicknesses, the size of the copper blocks, the location and size of microvia arrays cannot be presented for confidentiality reasons. This is why direct comparisons between simulation and experiment cannot be proposed with accuracy. However, this experimental device will be used to illustrate the measurement methods and verify the main trends obtained with simulation.

In Fig. 1, the height of each heat sink is $H_D = 20$ mm. The other heat sinks dimensions are given in Table 1 and Fig. 3. The capacitor matrix is composed of 63 SMD capacitors (10 μF) which are uniformly distributed between +DC and -DC heat sinks.

To compare different decoupling capacitor configurations (section 3), other switching cells have been implemented by soldering 8 SMD capacitors (10 μF) on the top of the PCB between +DC and -DC heat sinks as seen in Fig. 6.

The experimental measurement of the stray inductance is quite easy when the waveform of current can be captured. However, since it is not possible to include a current sensor in the present switching cell, another method must be used. Very often, the measurement is done during the V_{DS} ringing after turn-off (Yang et al., 2018). In this case, the oscillation frequency f_0 is linked to the stray inductance L_s by the following relationship:

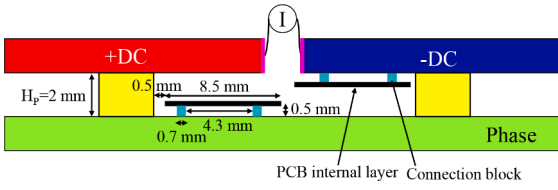


Fig. 7. Geometry with internal layers (cross section).

$$f_o \approx \frac{1}{2\pi\sqrt{L_s C_{oss}}} \quad (1)$$

where C_{oss} is the output capacitance of one MOSFET.

However, the value of C_{oss} is highly nonlinear and can be modified by different parameters as the DC bus voltage, the capacitance of the package... This is why, another method is used in this paper. The principle is to charge the decoupling capacitors with a small voltage (typically several V), then disconnect the voltage source, and finally turn-on both MOSFETs to obtain an oscillating waveform between the decoupling capacitors and the stray inductance. The oscillation frequency can thus be linked to the stray inductance of the switching cell by:

$$f_o = \frac{\sqrt{1 - m^2}}{2\pi\sqrt{L_s C_{dec}}} \quad (2)$$

where C_{dec} is the total capacitance of the decoupling capacitors, and m is the damping factor.

With this experimental configuration, the measurement is independent of C_{oss} . However, the damping factor m of this circuit, given by (3), greatly depends on the total resistance R_{tot} of the circuit and on the C_{dec} value. This value must therefore be adapted to the devices implemented in the switching cell as it will be seen in section 4.

$$m = \frac{R_{tot}}{2} \sqrt{\frac{C_{dec}}{L_s}} \quad (3)$$

Section 2 was dedicated to the presentation of both simulation and experimental tools which are used to estimate the stray inductance. In the following section, they will be implemented to compare different switching cell architectures. The main goal is therefore to provide some design rules for the implementation of TAPIR switching cells.

3. Comparison of different switching cell architectures

3.1. Internal layers of PCB

A PCB with embedded dies is placed between the different heat sinks of the TAPIR switching cell as shown in Fig. 1. Due to the presence of gate and source electrodes, and of the guard ring termination on one side of the chips, the PCB must include several internal layers in its volume. This is the case of the PCB presented in Fig. 1 for instance. A clever use of these internal layers allows modifying the parasitic elements (inductances and capacitances) of the interconnects. To illustrate this possibility with magnetic simulations, Fig. 7 shows a geometry where two internal conductors are present to reduce the distance between DC link and Phase heat sinks potentials. The dimensions of these conductors are 8.5 mm × 25 mm × 0.1 mm. They are connected to the source electrode of each chip through two conductive blocks (0.7 mm × 25 mm × 0.5 mm) which represent a connection by vias between two layers of the PCB.

An inductance of 2.2 nH is obtained for this configuration using internal layers, in comparison with 2.47 nH in the switching cell without them (Table 2). It can be explained by the decrease of the switching cell loop area and therefore the reduction of the magnetic field. The use of internal layers is therefore interesting to reduce the stray inductance of switching cells. However, it has to be done carefully: a trade-off is

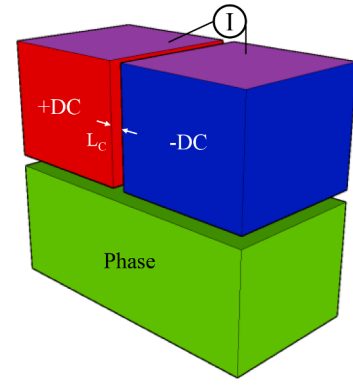


Fig. 8. Current injection on the top of DC link heat sinks.

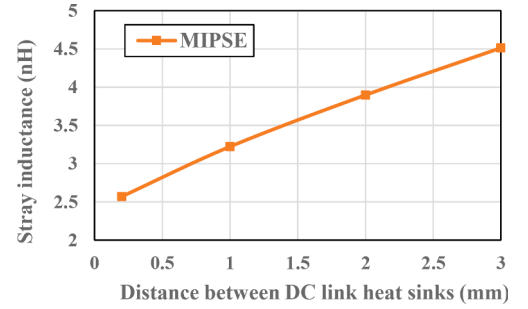


Fig. 9. Stray inductance as a function of L_c – current injection on the top.

necessary between the decrease of the parasitic inductance and the increase of the capacitance between heat sinks. The latter will reduce the switching speed of the devices, especially for SiC MOSFETs which have a very low output capacitance C_{oss} (several hundreds of pF).

Also, a study of the current capability of these internal layers is necessary to limit their self-heating during operation. Indeed, the current repartition between the internal layers and the heat sinks highly depends on the frequency: the current ratio in the internal layers increases with the frequency due to skin effect. It was verified with MIPSE that the current in the internal layers was 93% of the total current at 100 MHz, and 30% at 10 kHz. Hence the switching frequency has a huge impact on the rms current in internal layers.

3.2. Position of the decoupling capacitors

The position of the decoupling capacitors between DC link heat sinks as proposed in Fig. 1 reduces the stray inductance but adds an integration complexity. In addition, in many cases, the small space between heatsinks does not allow obtaining capacitance values sufficient to ensure the necessary energy storage for the operation of the converter. Another possibility is therefore to place the decoupling capacitors on the top of the DC link heatsinks. This position has the advantage of being simpler to implement, decouples the lifetime of the module from that of the capacitors, and allows increasing the global capacitance. Simulations are thus carried out to study the impact of this new position on the stray inductance of the switching cell.

For these simulations, the current injection is done on the top of the heat sinks as shown in Fig. 8. With the position of the decoupling capacitors between DC link heatsinks (Fig. 1), the distance between them depends on the size of the capacitors included in the matrix. By changing the position of the capacitors as shown in Fig. 8, the distance L_c between heatsinks can be modified and has a non-negligible impact on the stray inductance of the switching cell. Fig. 9 shows the evolution of this inductance as a function of L_c . Obviously, this inductance increases with the distance due to the increase of the current loop area. However, the

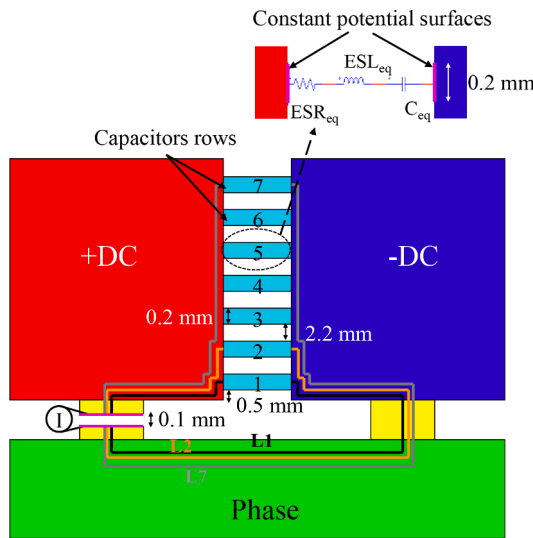


Fig. 10. Geometry and capacitor modeling for studying the current repartition between capacitor rows.

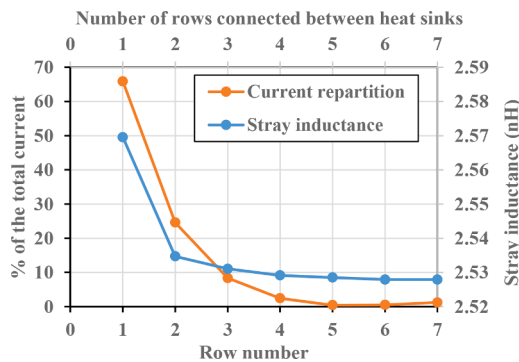


Fig. 11. Current repartition between capacitor rows and variation of the inductance as a function of the number of capacitor rows connected between heat sinks.

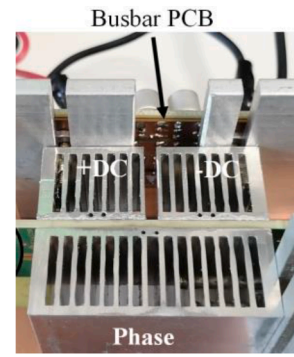
obtained value (<3.5 nH for 1.5mm) remains low enough for SiC devices. Furthermore, if L_C is reduced to 0.2 mm, the stray inductance is very close to the one obtained with the implementation proposed in Fig. 5a (2.6 nH). This capacitor position seems therefore to be interesting and should be studied in future works.

3.3. Study of the decoupling capacitor matrix

As shown in Fig. 1, the spacing between +DC and -DC heat sinks can be used to integrate decoupling capacitors. In this figure, a matrix of 63 SMD capacitors is implemented for this purpose. It contains 7 rows of 9 capacitors (0805 package). The capacitance of each elements is 10 μ F.

For stray inductance estimation, the geometry of the switching cell with the capacitor matrix can be represented schematically by Fig. 10. It can be seen that each capacitor row does not see the same inductance: it is the highest for row 7 and the lowest for row 1. This difference in inductance induces a current imbalance between capacitors rows which must be studied.

To study the impact of the number of capacitor rows, the entire geometry with heatsink is used. The height of each heat sink H_D is 20 mm. For studying the current repartition between capacitor rows, the location of the current injection must be modified. Here, a thin opening is made in the middle of one chip to perform the current injection on equipotential surfaces (current lines perpendicular to the surface). The placement of each capacitor row on each DC link heat sink is represented



(a) Physical implementation

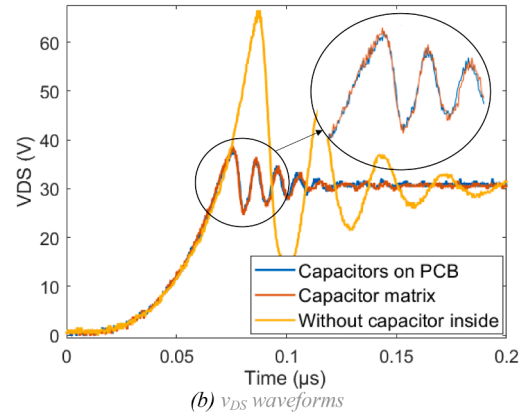


Fig. 12. Switching behavior during turn-off for different decoupling capacitor configurations.

by 7 equipotential surfaces.

With the MIPSE software, it is possible to insert the equivalent model of a capacitor between two equipotential surfaces. This tool is thus used to model the capacitance rows between DC link heat sinks as shown in Fig. 10. The equivalent model of a single capacitor is a capacitance $C=10$ μ F in series with a resistance $ESR=10$ m Ω and an inductance $ESL=1$ nH (values obtained from the datasheet). Since each row is composed by 9 capacitors, a 90 μ F capacitance C_{eq} in series with a resistance $ESR_{eq}=1.1$ m Ω and an inductance $ESL_{eq}=0.11$ nH are implemented. The current is measured in each capacitor row. Note that the inductive model neglects the magnetic couplings between capacitors.

The current distribution in the different capacitor rows is presented in Fig. 11 for a 100 MHz frequency. With the geometry and capacitor values chosen in this example, it can be observed that nearly 66% of the total current circulates in row 1 (see Fig. 10 for the row numbers), against only 24% and 6% respectively in row 2 and row 3. Row 4 is crossed by less than 2% of the total current while less than 1% flows through rows 5, 6 and 7. As a consequence, the stray inductance does not depend a lot on the number of rows that are connected between the DC link heat sinks. Indeed, it is shown in the same figure that the stray inductance is 2.57 nH when only row 1 is connected and decreases slightly to ≈ 2.53 nH when all rows (1 to 7) are connected.

As a conclusion, it seems that the introduction of a capacitor matrix is not useful to decrease the stray inductance in this example. However, the current distribution depends on the geometry of the switching cell as well as the value of SMD capacitances. This study must thus be done for each application.

3.4. Experimental validation

In order to evaluate the impact of the different decoupling capacitor configurations, the switching behavior during turn-off is measured

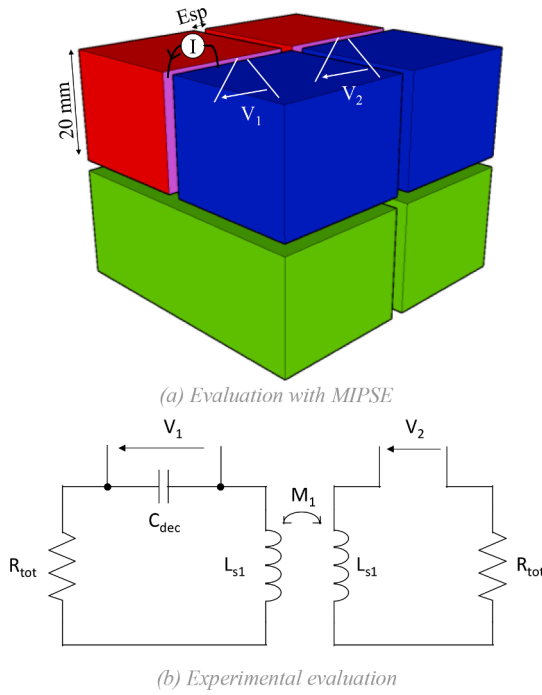


Fig. 13. Evaluation principle of stray inductance and mutual inductance of two adjacent cells.

based on the double pulse test method. A setup with an external PCB busbar is fabricated to characterize the switching cell as shown in Fig. 12a. The drain-source voltage v_{DS} across one MOSFET of the switching cell is measured with care, as close as possible to the chip. Fig. 12b presents v_{DS} waveforms during turn-off for different decoupling configurations:

- with a capacitor matrix (Fig. 1),
- with capacitors soldered on the PCB (Fig. 6)
- without integrated decoupling capacitor.

For these tests, the DC bus voltage is 30 V and the output current is 50 A. As expected, they clearly show the interest of integrating decoupling capacitors inside the switching cell because the overvoltage is much higher when only the external busbar PCB is present. However, it is also shown that the switching behavior of both switching cells with decoupling capacitors are very close to each other. It confirms the analysis presented in the previous paragraph.

This section gave some insights for the design of single switching cells. However, in the global system, they are integrated close to each other (Fig. 2). This proximity induces electromagnetic interactions between cells which modifies the stray inductances. This will be studied in the next section.

4. Evaluation of electromagnetic coupling between switching cells

When a switching cell is close to another one, the creation of eddy currents in the second cell decreases the magnetic flux created by the first one and therefore decreases its stray inductance. Also, a magnetic coupling exists between both switching cells and induces a mutual inductance between them. The goal of this paragraph is to evaluate these magnetic interactions and to determine if they have to be considered during the design of the switching cell.

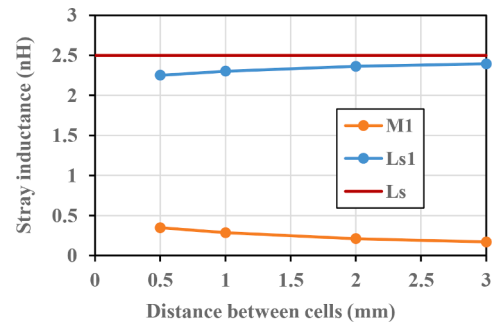


Fig. 14. Stray inductances and mutual inductances of adjacent cells as a function of the distance between them. L_{s1} is the stray inductance when one adjacent cell is present, M_1 the mutual inductance with this cell, L_s the stray inductance of a single cell for comparison.

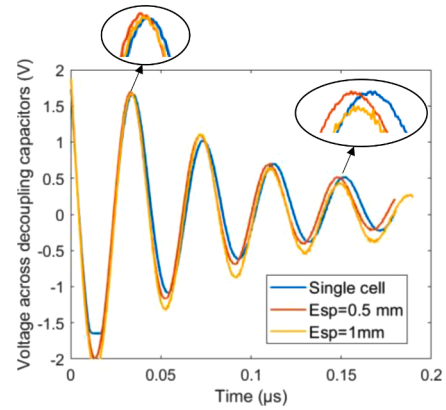


Fig. 15. Voltage across decoupling capacitors for a single cell, and for adjacent cells. E_{sp} is the distance between cells.

4.1. Inductance of adjacent switching cells

The inductance of a switching cell is first estimated as a function of the distance E_{sp} between both cells using the MIPSE software. The modeling principle is presented in Fig. 13a. The current I (frequency $f = 100$ MHz) is injected on the internal faces of the DC link heat sinks of one switching cell. Voltage V_1 is measured across the DC link internal faces of this cell to obtain the stray inductance L_{s1} by:

$$L_{s1} = \frac{V_1}{2\pi f \cdot I} \quad (4)$$

To estimate the mutual inductance M_1 between them, the circuit of the second cell must be open, therefore the decoupling capacitors are not included, and voltage V_2 is measured:

$$M_1 = \frac{V_2}{2\pi f \cdot I} = L_{s1} \frac{V_2}{V_1} \quad (5)$$

For $E_{sp}=0.5$ mm, it can be seen in Fig. 14 that the stray inductance L_{s1} of a switching cell close to another one is 10% lower than the stray inductance L_s of an isolated switching cell ($L_s=2.5$ nH). The influence of the other switching cell is logically lower when the distance E_{sp} increases because of the decrease of eddy currents in the second cell. The decrease is divided by two when $E_{sp}=3$ mm. Regarding the mutual inductance between cells, it is quite low, in the range 5-15% of L_s .

4.2. Experimental evaluation

For this experimental study, switching cells with SMD capacitors soldered on the PCB (Fig. 6) are used because they are simpler to implement. Also, it was shown in the previous section that this

Table 3
Magnetic interaction effects.

	Single cell	Esp 0.5 mm	Esp 1 mm
Stray inductance	1.35 nH	1.25 nH	1.30 nH
Mutual inductance	/	≈ 0.13 nH	≈ 0.10 nH

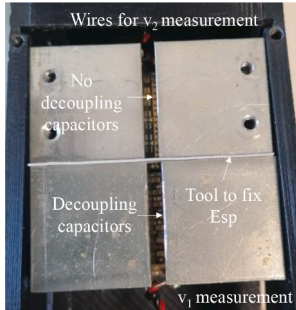
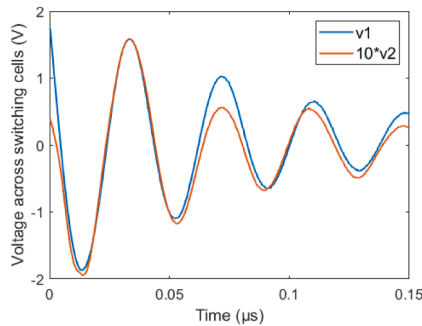


Fig. 16. Setup for estimating electromagnetic interactions between cells (top view) (b) Voltage waveforms for $E_{sp}=0.5$ mm.



(b) Voltage waveforms for $E_{sp}=0.5$ mm

Fig. 17. Setup for estimating electromagnetic interactions between cells and results.

configuration had a negligible impact on the stray inductance.

First, the measurement of the stray inductance of a single switching cell is done with the method presented in paragraph 2.2: the stray inductance is estimated from the oscillation frequency between the decoupling capacitors and the stray inductance (Eq. (2)). For the devices implemented in this switching cell ($R_{dson} \approx 1m\Omega$), the free oscillation regime is not possible with $8 \times 10 \mu F$ SMD capacitors. They are thus replaced by 8 capacitors with lower capacitances ($C_{dec}=30$ nF) to decrease the damping factor as shown in (3). A higher voltage rating (1000 V) is also chosen to limit non-linearities of the capacitance during oscillations. The voltage across the decoupling capacitors is presented in Fig. 15 (“Single cell” curve). With (2) it is then possible to estimate the stray inductance. The obtained value is 1.35 nH as shown in Table 3. This value is lower than the one obtained with MIPSE (Table 2) mainly because the distance between chips D_{EP} is reduced in the experimental device.

The method based on free oscillations can also be used to estimate the electromagnetic coupling between switching cells. Fig. 16 presents the experimental setup to fix the distance E_{sp} between switching cells. Fig. 15 shows that the oscillation frequency is actually higher when another switching cell is placed close to the studied cell due to the reduction of the stray inductance as discussed in section 3. The estimated values of stray inductances are given in Table 3 for two E_{sp} values. It shows that the stray inductance reduction is lower than 10% for $E_{sp}=0.5$ mm. Compared to the simulation study, the distance between chips is reduced in this switching cell which means lower

magnetic interactions.

Also, if the decoupling capacitors are not present in the second cell (Figs. 13b and 16), the measurement of the voltage V_2 across the location of these capacitors can be used to estimate the mutual inductance M_1 between both cells as it was done in the simulation study with (5).

Fig. 17 shows the waveforms of v_1 and v_2 during oscillations for $E_{sp}=0.5$ mm. It can be seen that the ratio between these two voltages as defined by (5) is close to 0.1 which is logically lower than the simulation results presented because of the reduction of H_p . Table 3 gives estimated mutual inductances for different distances E_{sp} between cells. Logically, the mutual inductance decreases with the increase of this distance as shown by simulations.

5. Discussion

5.1. Stray inductance value

The TAPIR technology intends improving the thermal management of air-cooled power converters. The elementary switching cells were designed to obtain a low stray inductance and limit overvoltage during switching. Based on the results obtained in simulation and experimental studies, it is proposed here to benchmark this packaging proposition with other embedded solutions from literature.

With simulations on a simplified geometry, it was observed that the stray inductance of TAPIR switching cells was in the range 0.8 to 4 nH (Fig. 4) depending on geometrical parameters as the distance between chips D_{EP} and the distance between DC and phase heat sinks H_p . With experiments, a 1.35 nH stray inductance (including the ESL of decoupling capacitors) was obtained.

Neeb et al. (2014) presented a PCB embedded package for Si diodes and IGBTs. With simulations, they estimated a stray inductance close to 1 nH. This value can be explained by a low H_p value (≈ 0.22 mm). Hoene, Ostmann, and Marczok (2014) proposed a 20 mm \times 30 mm packaging for JFET devices with a stray inductance lower than 0.6 nH. This very low value is also due to a low thickness of the package ($H_p \approx 0.5$ mm) and a low distance between dies ($D_{EP} \approx 5$ mm). Marczok et al. (2019) studied a package based on a multilayer AMB (active metal brazed) substrate and prepackaged power MOSFETs. They measured a stray inductance lower than 1.6 nH which can be explained by a low distance between chips (≈ 5 mm). Knoll et al. (2021) obtained a 2.3 nH stray inductance with 1200 V SiC MOSFET chips embedded in a PCB. For clearance and thermal requirements, the distance between chips is close to 25 mm which limits the decrease of the inductance.

Thus, both simulation and experimental studies presented in this paper show that the stray inductance of the TAPIR switching cell is close to the ones obtained in the literature. For the experiments, it was chosen to keep a sufficient distance between chips (> 10 mm) for limiting the thermal coupling. However, simulations show that stray inductances lower than 1 nH are easily reachable. A trade-off between stray inductance and thermal behavior is therefore necessary to determine this distance.

It was also shown that the distance between heat sinks D_{EP} and the presence of internal layers could decrease efficiently the stray inductance. However, the choice of this distance must be done by considering the increase of the parasitic capacitance. Indeed, this capacitance can slow down the commutation, and therefore increase switching losses.

5.2. Decoupling capacitors

It was shown in Fig. 1 that the large area between +DC and -DC heat sinks gave the opportunity of integrating a large number of decoupling capacitors. It was a matrix of 63 SMD capacitors in this example.

On a stray inductance point of view, it was demonstrated in paragraph 3.3 that the use of this matrix did not allow decreasing significantly the stray inductance compared with a classical arrangement with decoupling capacitors brazed on the top of the PCB.

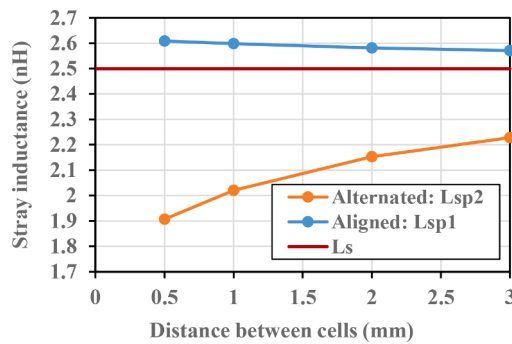


Fig. 18. Stray inductance of two paralleled adjacent switching cells - L_s is the stray inductance of a single cell for comparison.

However, for applications with high switching frequencies and which necessitate relatively low DC link capacitance (like 3 phase inverters for example), this feature could be used to integrate the whole DC link in the switching cell. One possible interest is that the capacitors could be cooled by the heat sinks that could increase their maximum RMS current. However, this feature has to be demonstrated by thermal studies in the future.

5.3. Stray inductance of adjacent paralleled switching cells

In section 4, it was shown that magnetic interactions exist between adjacent switching cells. Therefore, it is interesting to evaluate the impact of this coupling on the stray inductance of paralleled and adjacent switching cells.

For this discussion based on simulation results (paragraph 3.1 – Fig. 13a), the current sharing between both cells is considered to be perfect. In a first configuration, the DC potentials are aligned (Fig. 2a), and, in a second, they are alternated (Fig. 2c). The inductance of each cell is determined as a function of the distance E_{sp} between them for each case as presented in Fig. 18. L_{sp1} is the inductance with aligned heat sinks and L_{sp2} is the one with alternated heat sinks. It is found that L_{sp1} is higher than the inductance of an isolated cell L_s contrarily to L_{sp2} which is always lower than L_s . When $E_{sp}=0.5$ mm, L_{sp2} is 30% lower than L_{sp1} which means that the alternated configuration helps decreasing the stray inductance of switching cells. Also, it is verified with these results that the following relationships are respected:

$$L_{sp1} = L_s + |M_1| \quad (6)$$

$$L_{sp2} = L_s - |M_1| \quad (7)$$

The arrangement of the DC link with multiple paralleled switching cells has therefore a non-negligible impact on the global stray inductance. Future work will have to study if this phenomena worth being used for a global reduction of the stray inductance, in some high current applications.

6. Conclusion

The TAPIR (compact and modular Power modules with Integrated cooling) technology necessitates a multiphysics analysis to prove its interest compared to current power module solutions. To contribute to this objective, this paper focused on magnetic aspects and, more specifically, on stray inductance evaluation.

A stray inductance of 1.35 nH was measured with a device including a PCB with embedded low voltage Si MOSFETs. Also, it was shown by simulations that stray inductances lower than 1 nH could be obtained. However, a trade-off must be made with thermal performances and parasitic capacitance to obtain the best geometrical parameters.

It was also shown that the inclusion of a decoupling capacitor matrix in the switching cell did not allow decreasing significantly the stray

inductance compared with a more classical arrangement.

Finally, it was shown that the magnetic coupling between switching cells has a relatively low impact on the stray inductance (decrease lower than 10%). However, the presence of mutual inductances between adjacent cells is not negligible. The design of the DC link must therefore be considered for the design of topologies with paralleled devices.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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